TMS320C6678 EVM Board for TI

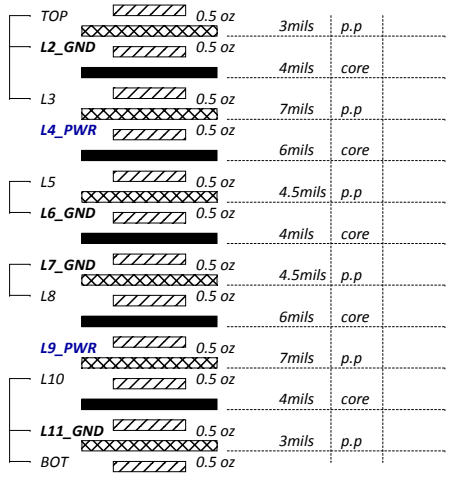
Product name : DSPM-8301E

Rev. A101-1

PCB PN : 19C2830100

Project Code :

PCB Thickness : 62 mils(1.6mm)
12 Layers



Texas Instruments
20450 Century Blvd
Germantown, MD 20874
USA

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COVER PAGE		
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Title: TITLE & TABLE OF CONTENTS

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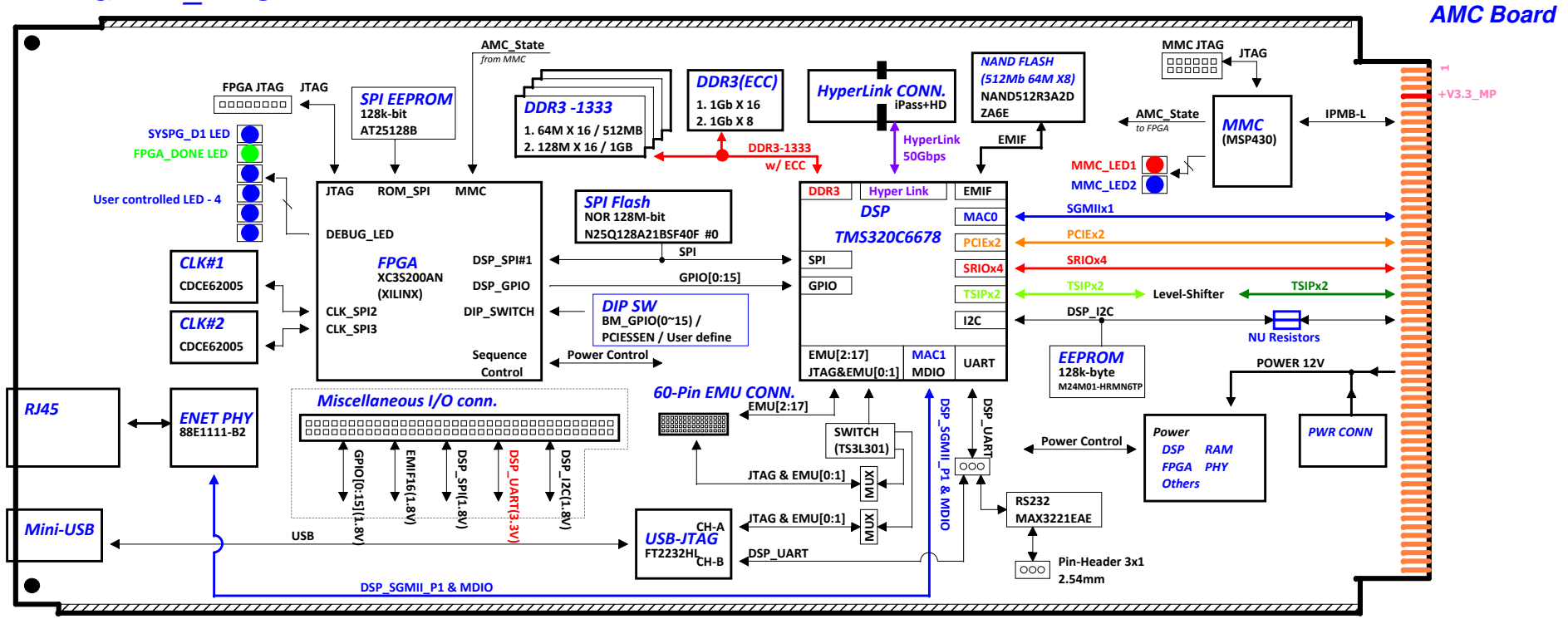
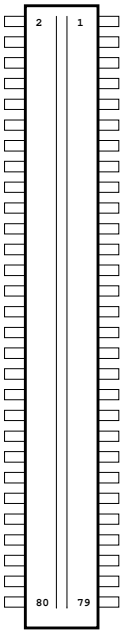
BLOCK DIAGRAM_AMC



Miscellaneous I/O 80 Pin conn. Signal

PIN	Port mapping
02	EMIFA00
04	EMIFA01
06	EMIFA02
08	EMIFA03
10	EMIFA04
12	EMIFA05
14	EMIFA06
16	EMIFA07
18	EMIFA08
20	EMIFA09
22	EMIFA10
24	EMIFA11
26	EMIFA12
28	EMIFA13
30	EMIFA14
32	EMIFA15
34	EMIFA16
36	EMIFA17
38	EMIFA18
40	EMIFA19

PIN	Port mapping
42	EMIFA20
44	EMIFA21
46	EMIFA22
48	EMIFA23
50	GPIO00
52	GPIO01
54	GPIO02
56	GPIO03
58	GPIO04
60	GPIO05
62	GPIO06
64	GPIO07
66	GPIO08
68	GPIO09
70	GPIO10
72	GPIO11
74	GPIO12
76	GPIO13
78	GPIO14
80	GPIO15



PIN	Port mapping
01	GND
03	SDA
05	SCL
07	EMIFD0
09	EMIFD1
11	EMIFD2
13	EMIFD3
15	EMIFD4
17	EMIFD5
19	EMIFD6
21	EMIFD7
23	EMIFD8
25	EMIFD9
27	EMIFD10
29	EMIFD11
31	EMIFD12
33	EMIFD13
35	EMIFD14
37	EMIFD15
39	EMIFCE1Z

PIN	Port mapping
41	EMIFCE2Z
43	EMIFBE0z
45	EMIFBE1z
47	EMIFOEz
49	EMIFWEz
51	EMIFRnW
53	EMIFWAIT1
55	TIMI0
57	TIMO0
59	TIMI1
61	TIMO1
63	SSPMISO
65	SSPMOSI
67	SSPCS1
69	SSPCK
71	UARTTXD
73	UARTRXD
75	UARTRTS
77	UARTCTS
79	GND

AMC Port mapping

PIN	Port mapping
TCLKA	TSIP_CLK0
TCLKB	TSIP_CLK1
FCLKA	100MHz
00	SGMII
01	
02	
03	
04	PCI-E_1
05	PCI-E_2
06	
07	
08	SRIO_1
09	SRIO_2
10	SRIO_3

PIN	Port mapping
11	SRIO_4
12	TSIP0 [0..3]
13	TSIP1 [0..3]
14	
15	Alternate I2C link
16	
TCLKC	TSIP_FS0
TCLKD	TSIP_FS1
17	
18	
19	
20	

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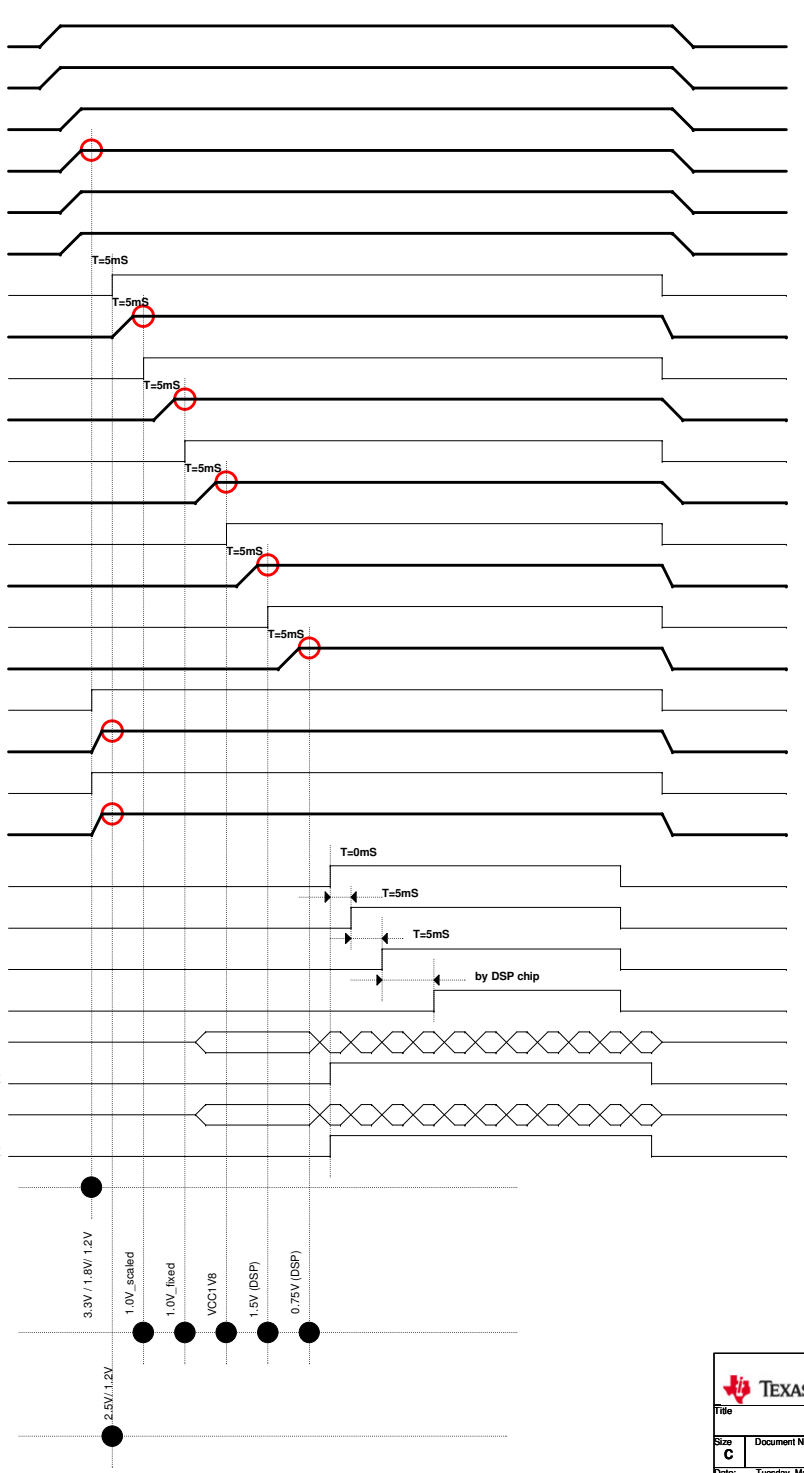
Power Sequence

Label	Time	Description
T0	1ms	S2 plane power stable to S3 enable signal assertion

				VCC3V3_MP_AMC
S0		MMC		VCC3V3_MP
S1				VCC12
S2	Other	FT2232H	XC3S200AN	VCC3V3_AUX
S3			XC3S200AN	VCC1V8_AUX
S4		88E1111	XC3S200AN	VCC1V2
S5				PMBUS & UCD9222_ENA1
S6		DSP TMS320C6678		CVDD
S7				UCD9222_VID2 & UCD9222_ENA2
S8		DSP TMS320C6678		VCC1V0
S9				VCC1V8_EN
S10		DSP TMS320C6678		VCC1V8
S11				VCC1V5_EN
S12	DDR3	DSP TMS320C6678		DDR3 SDRAM VCC1V5
S13				VCC0V75_EN
S14	DDR3	DSP TMS320C6678		DDR3 Vref VCC0V75
S15				VCC2V5_EN
S16		88E1111		VCC2V5
S17				VCC5_EN
S18		XDS560V2 Mazzenine Board		VCC5



Ther is no specific power-up nor power-down sequence.

XILINX_XC3S200AN

1.2V_AUX (VCCINT)
1.8V_AUX (VCC1V8_AUX)
3.3V_AUX (VCCAUX)

XILINX_XC3S200AN

When power on: VDD → VCC_1V0 scaled (0ms<t<100us) → VCC_1V0 Fixed (0ms<t<100us) → VCC1V8 (0ms<t<100us) → 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref)

When power down: 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref) (0ms<t<100us) → VCC1V8 (0ms<t<100us) → VCC_1V0 Fixed (0ms<t<100ms) → VCC_1V0 scaled → VDD

DSP TMS320C6678

VCC1V0 Scaled/(CVDD)
VCC1V0 Fixed/(CVDD1)
VCC1V8/ (DVDD18)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

DSP TMS320C6678

Ther is no specific power-up nor power-down sequence.

88E1111 (PHY)

2.5V
1.2V

88E1111

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Title: Power Sequence

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POWER CONSUMPTION

							Max. Power Design			Operating (for Thermal)		
		V	I	Qty	Isub.	Efficiency	Pd (W)	I12V	I3vsb	Utilization	Pd (W)	Note
CVDD (12V-->1.0V)					**8.000**			**0.741**				UCD9222 + UCD7242
	TMS320C6678	1.00	8.000	1	8.000	90%	8.889	0.741	x	70%	6.222	
VCC1V0 (12V-->1.0V)					**5.000**			**0.463**				
	TMS320C6678	1.00	5.000	1	5.000	90%	5.556	0.463	x	70%	3.889	
VCC1V5 (12V-->1.5V)					**2.300**			**0.319**				TPS54620
	TMS320C6678	1.50	0.850	1	0.850	90%	1.417	0.118	x	70%	0.992	
	DDR3	1.50	0.240	5	1.200	90%	2.000	0.167	x	100%	2.000	
	VCC0V75 (VTT for DDR3) 1.5V-->0.75V							x				TPS51200
	DDR3	0.75	0.050	5	0.250	45%	0.417	0.035	x	70%	0.292	
VCC3V3_AUX (12V-->3.3V_AUX)					**2.484**			**0.748**				TPS54620
	FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
	XDS560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
	FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
	Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
	VCC1V8_AUX (3.3V_AUX-->1.8V_AUX)							x				TPS73701DCQ
	FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
	Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
	VCC1V8 (3.3V_AUX-->1.8V)							x				TPS73701DCQ
	TMS320C6678	1.80	0.330	1	0.330	46%	1.291	0.108	x	70%	0.904	
	FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
	VCC1V2_AUX (3.3V_AUX-->1.2V_AUX)							x				TPS73701DCQ
	FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
	88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
	VCC2V5 (3.3V_AUX-->2.5V)							x				TPS73701DCQ
	88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
VCC5 (12V-->5V)					**1.000**			**0.490**				TPS54231
	XDS560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
VCC3V3_MP_AMC (150mA)					**0.048**			x	**0.048**			
	MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
Total power consumption							**Pmax.**	**I12V**	**I3VSB**		**Pop.**	
							33.298	**2.762**	**0.096**		**23.909**	

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Title: POWER CONSUMPTION

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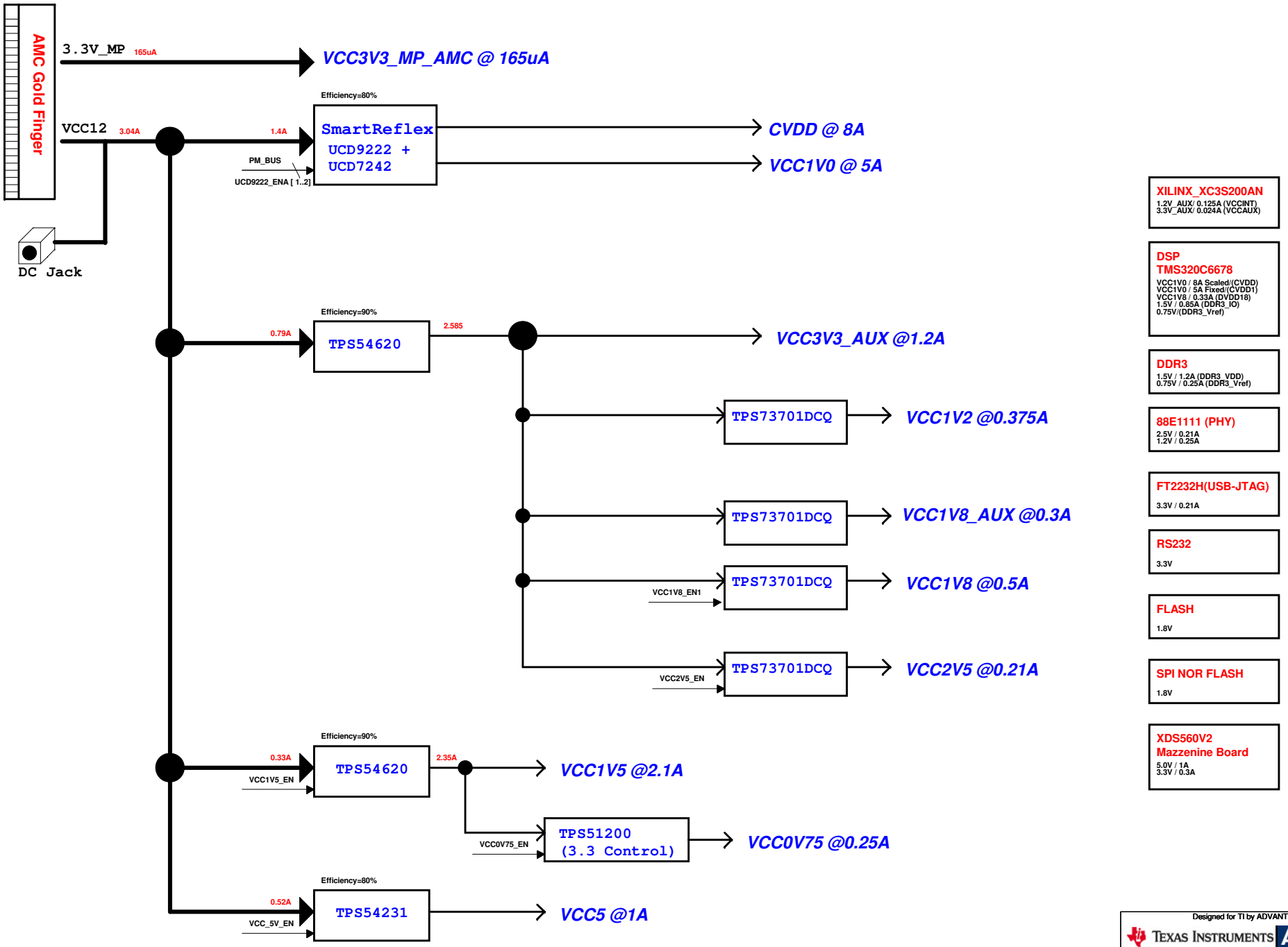
POWER DISTRIBUTION



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Title	POWER DISTRIBUTION	
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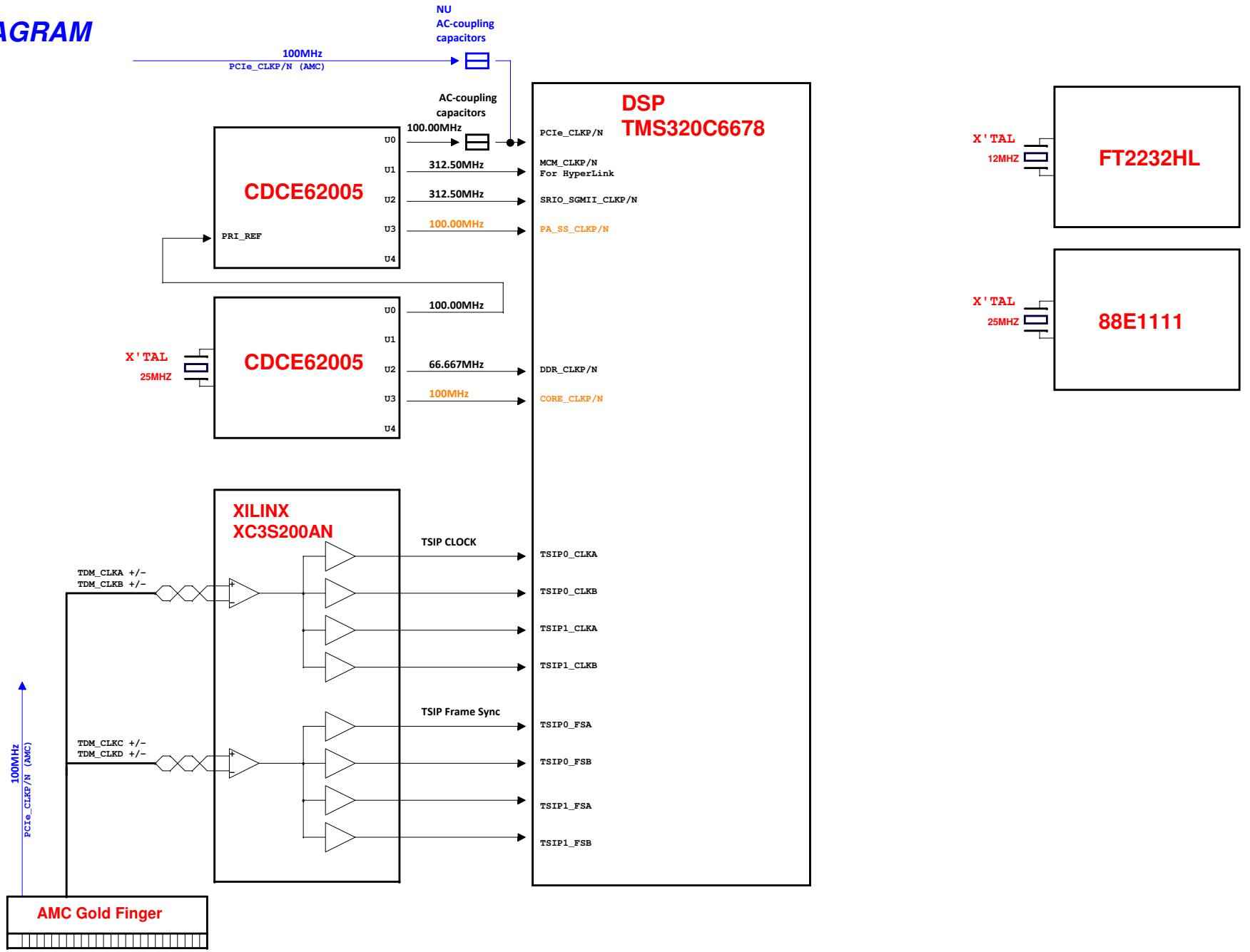
CLOCK DIAGRAM



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Title	CLOCK DIAGRAM	
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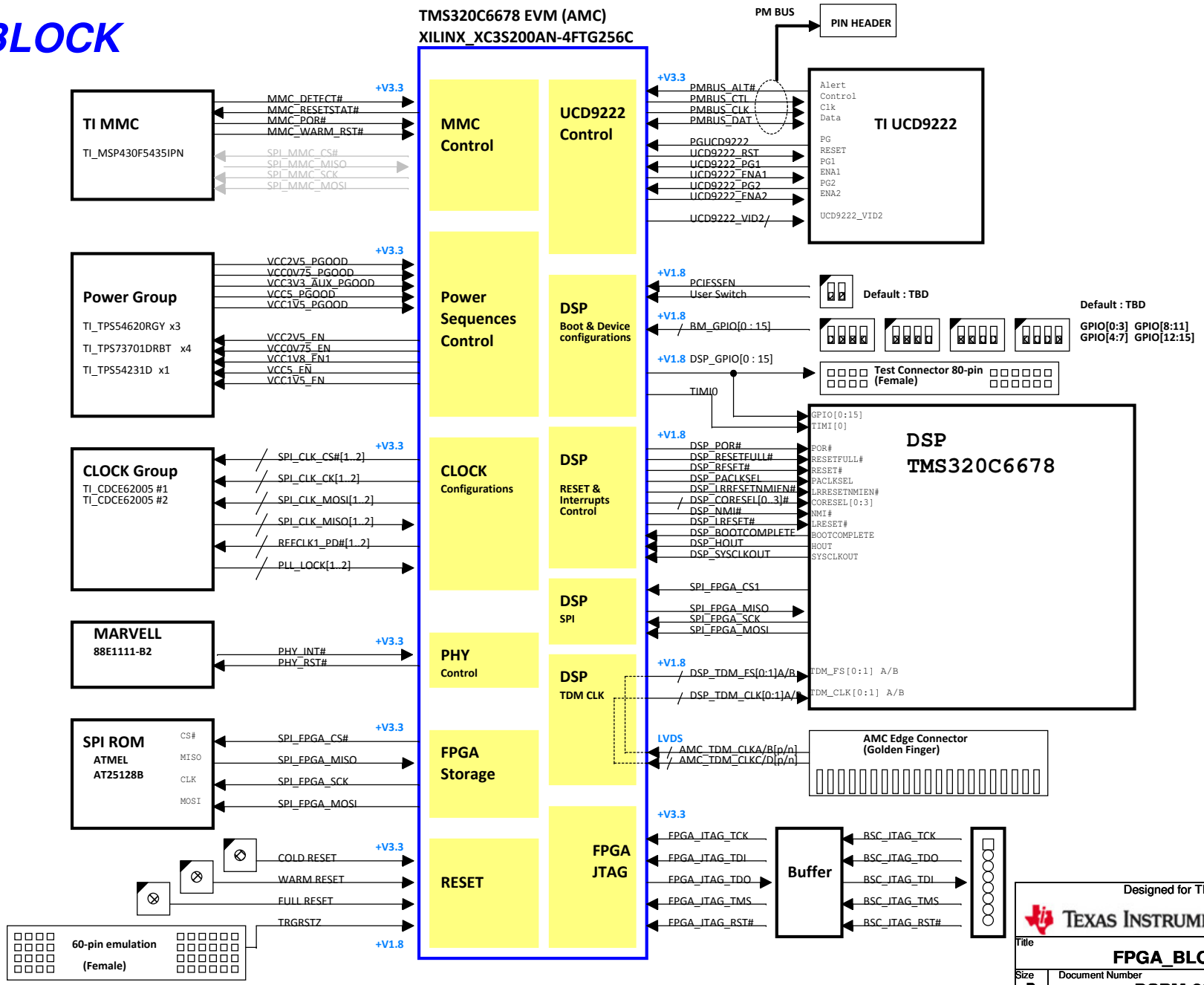
FPGA_BLOCK


TMS320C6678 EVM (AMC)
XILINX_XC3S200AN-4FTG256C
PM BUS
PIN HEADER
TI MMC
TI_MSP430F5435IPN
MMC_DETECT#
MMC_RESETSTAT#
MMC_POR#
MMC_WARM_RST#
SPI_MMC_CS#
SPI_MMC_MISO
SPI_MMC_SCK
SPI_MMC_MOSI
+V3.3
MMC Control
UCD9222 Control
PMBUS_ALT#
PMBUS_CTL
PMBUS_CLK
PMBUS_DAT
PGUCD9222
UCD9222_RST
UCD9222_PG1
UCD9222_ENA1
UCD9222_PG2
UCD9222_ENA2
UCD9222_VID2
Alert
Control
Clk
Data
PG
RESET
PG1
ENA1
PG2
ENA2
UCD9222_VID2
TI UCD9222
Power Group
TI_TPS54620RGY x3
TI_TPS73701DRBT x4
TI_TPS54231D x1
VCC2V5_PGOOD
VCC0V75_PGOOD
VCC3V3_AUX_PGOOD
VCC5_PGOOD
VCC1V5_PGOOD
VCC2V5_EN
VCC0V75_EN
VCC1V8_EN1
VCC5_EN
VCC1V5_EN
Power Sequences Control
DSP Boot & Device configurations
+V1.8
PCIESSEN
User Switch
Default : TBD
BM_GPIO[0 : 15]
Default : TBD
GPIO[0:3] GPIO[8:11]
GPIO[4:7] GPIO[12:15]
DSP_GPIO[0 : 15]
Test Connector 80-pin (Female)
TIMI0
GPIO[0:15]
TIMI[0]
CLOCK Group
TI_CDCE62005 #1
TI_CDCE62005 #2
SPI_CLK_CS#[1..2]
SPI_CLK_CK[1..2]
SPI_CLK_MOSI[1..2]
SPI_CLK_MISO[1..2]
REFCLK1_PD#[1..2]
PLL_LOCK[1..2]
CLOCK Configurations
DSP RESET & Interrupts Control
DSP_POR#
DSP_RESETFULL#
DSP_RESET#
DSP_PACLKSEL
DSP_LRRESETNMIEN#
DSP_CORESEL[0..3]#
DSP_NMI#
DSP_LRESET#
DSP_BOOTCOMPLETE
DSP_HOUT
DSP_SYSCLKOUT
POR#
RESETFULL#
RESET#
PACLKSEL
LRRESETNMIEN#
CORESEL[0:3]
NMI#
LRESET#
BOOTCOMPLETE
HOUT
SYSCLKOUT
DSP
TMS320C6678
MARVELL
88E1111-B2
PHY_INT#
PHY_RST#
PHY Control
DSP SPI
SPI_FPGA_CS1
SPI_FPGA_MISO
SPI_FPGA_SCK
SPI_FPGA_MOSI
DSP TDM CLK
DSP_TDM_FS[0:1]A/B
DSP_TDM_CLK[0:1]A/B
TDM_FS[0:1] A/B
TDM_CLK[0:1] A/B
SPI ROM
ATMEL
AT25128B
CS#
MISO
CLK
MOSI
SPI_FPGA_CS#
SPI_FPGA_MISO
SPI_FPGA_SCK
SPI_FPGA_MOSI
FPGA Storage
LVDS
AMC_TDM_CLKA/B[p/n]
AMC_TDM_CLKC/D[p/n]
AMC Edge Connector (Golden Finger)
COLD RESET
WARM RESET
FULL RESET
TRGRSTZ
60-pin emulation (Female)
RESET
FPGA JTAG
FPGA_JTAG_TCK
FPGA_JTAG_TDI
FPGA_JTAG_TDO
FPGA_JTAG_TMS
FPGA_JTAG_RST#
Buffer
BSC_JTAG_TCK
BSC_JTAG_TDO
BSC_JTAG_TDI
BSC_JTAG_TMS
BSC_JTAG_RST#
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TEXAS INSTRUMENTS
ADVANTECH
Title
FPGA_BLOCK
Size B
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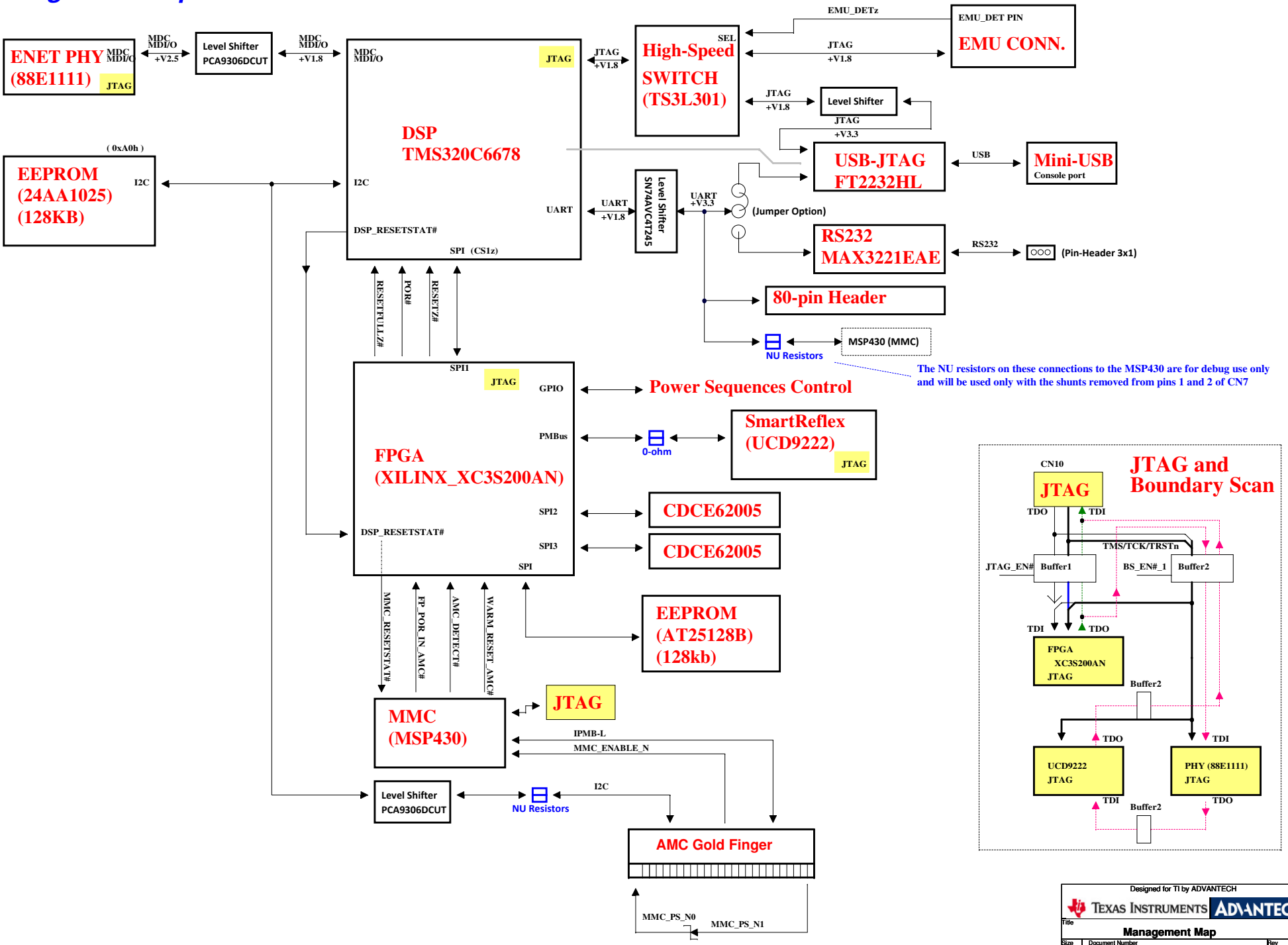
Management Map



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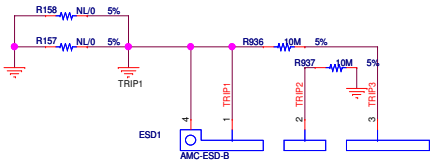
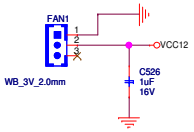
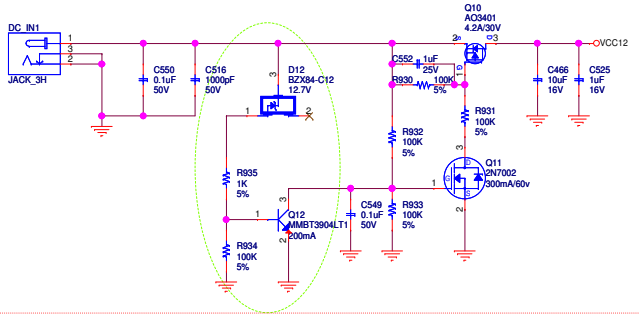
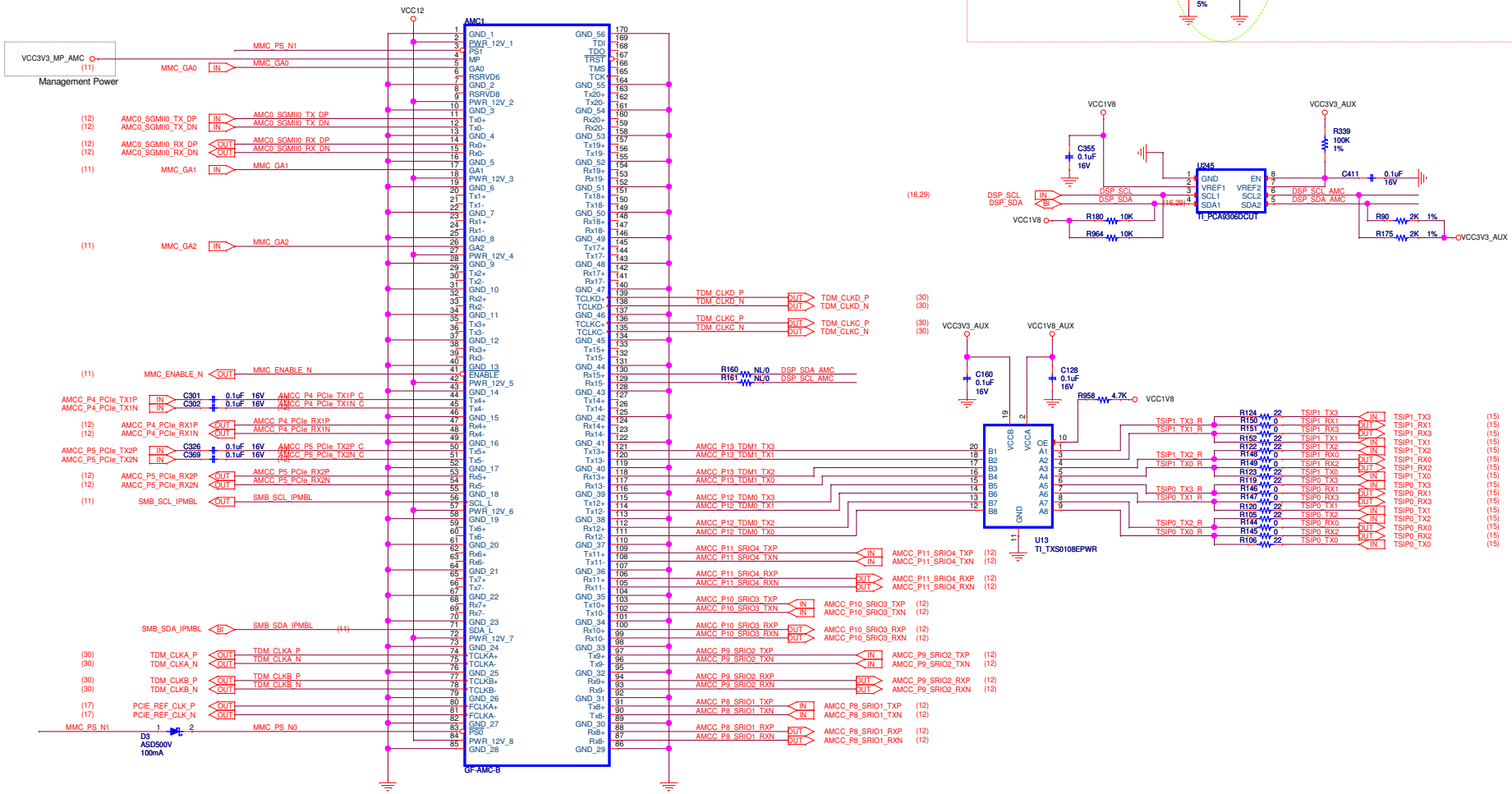
Front panel and ESD Strip





OVP: ~12.7V+0.6V = ~13.3V





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AMC GF			
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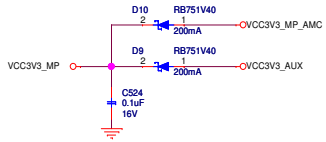
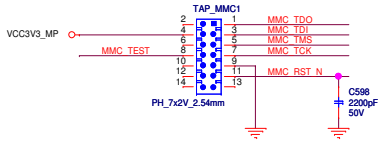
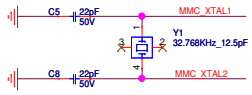
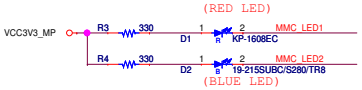
Power for MSP430

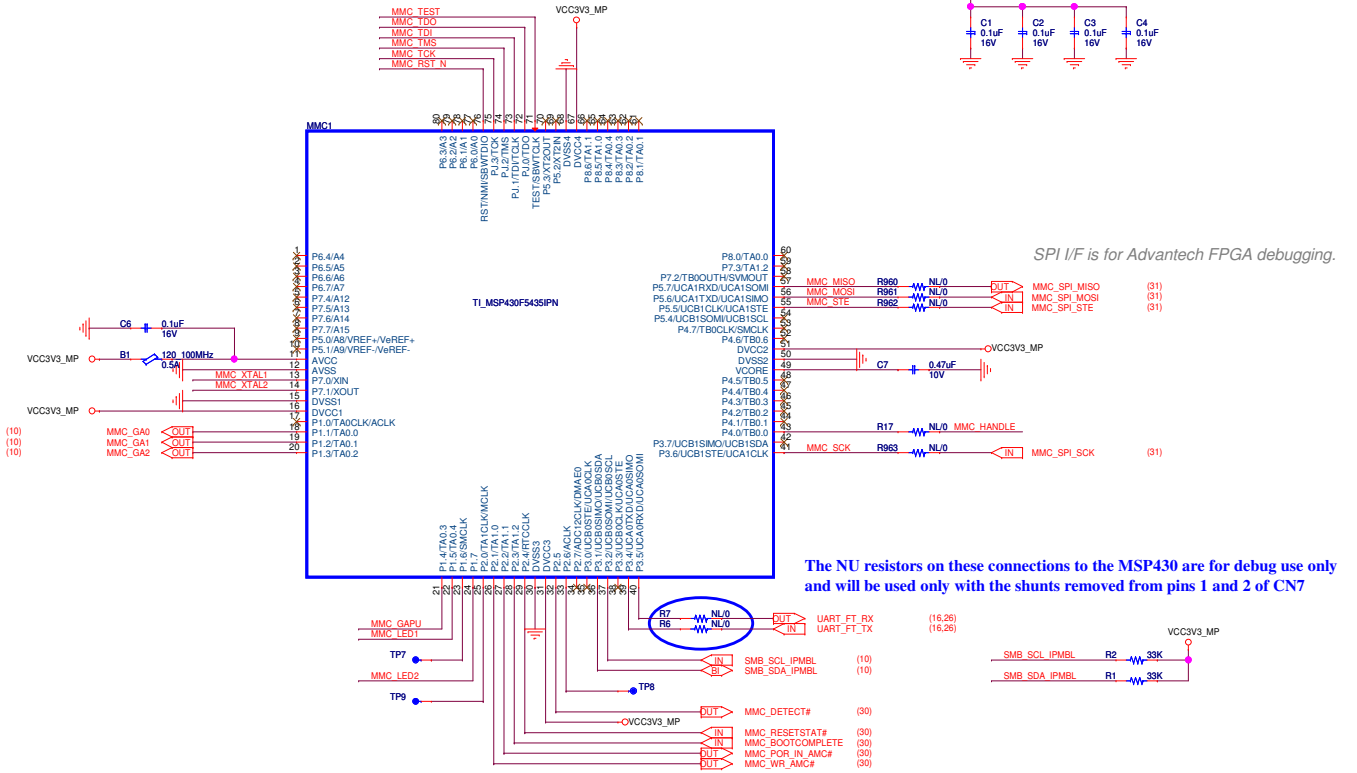


MMC JTAG



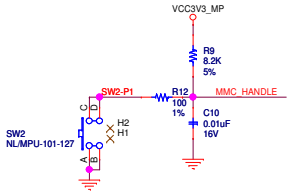


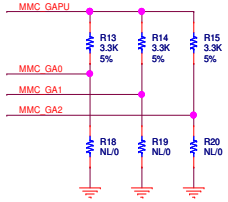


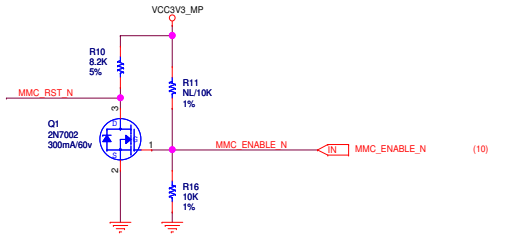


SPI I/F is for Advantech FPGA debugging.

The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7







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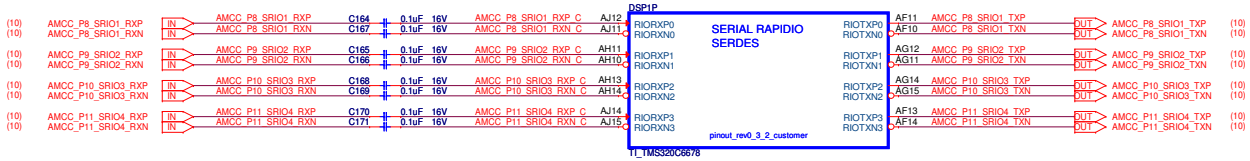
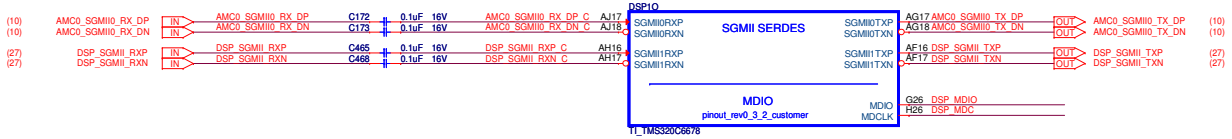
SRIO

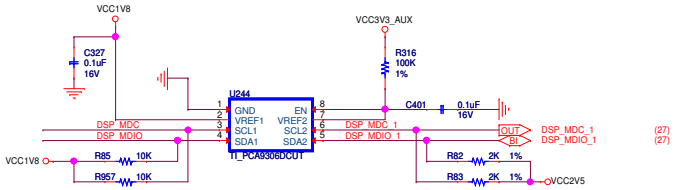


Caution!

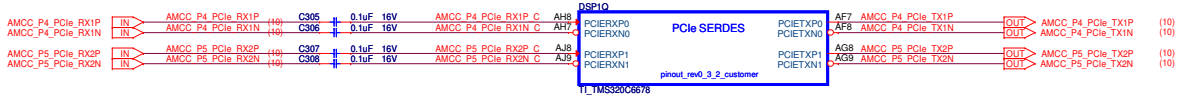
"Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

SGMII

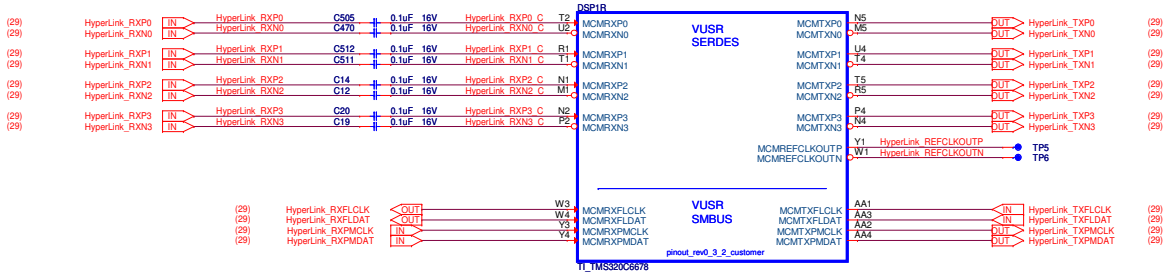




PCIE



HyperLink



"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"

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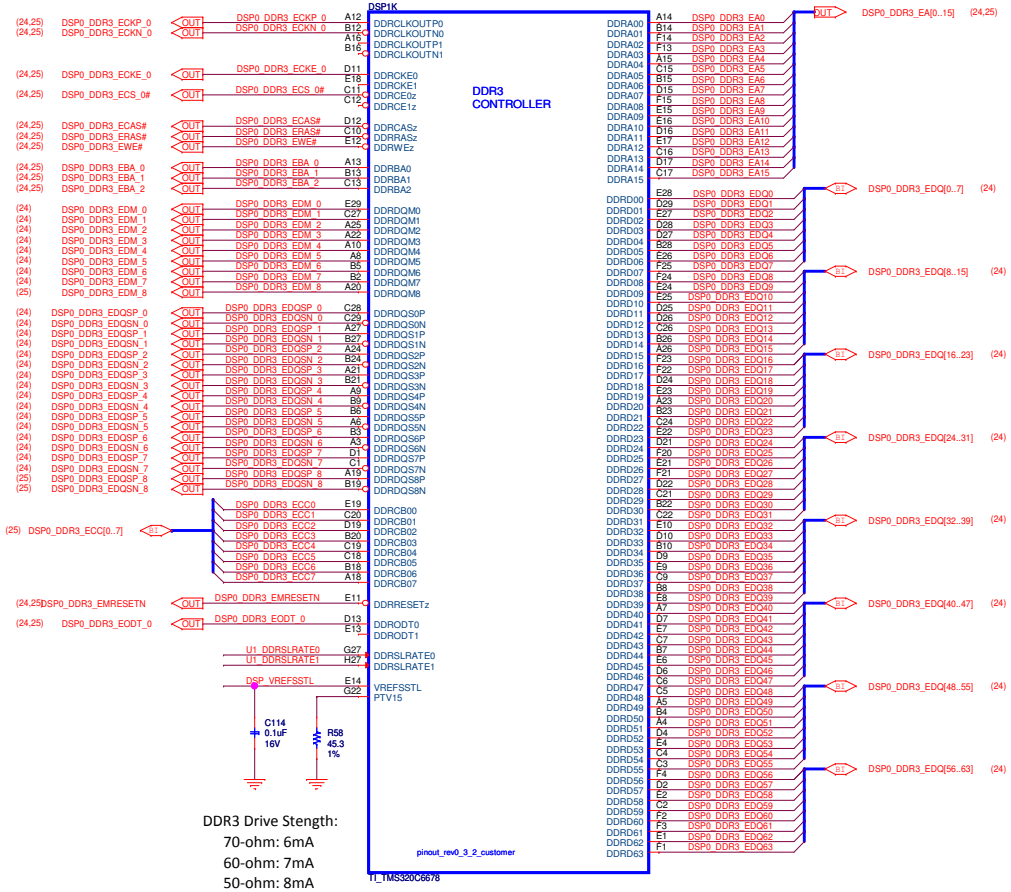


DDR3 Drive Stength:

70-ohm: 6mA

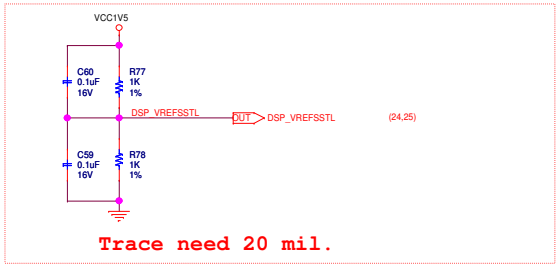
60-ohm: 7mA

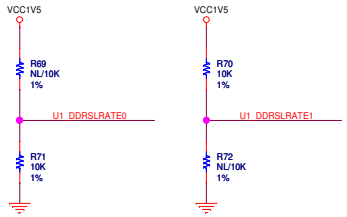
50-ohm: 8mA

45-ohm: 9mA

40-ohm: 10mA

36-ohm: 11mA





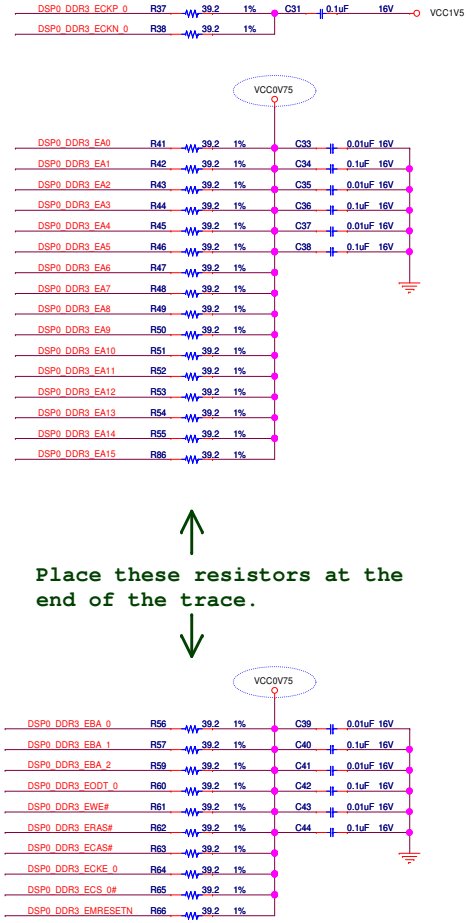
DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

0 0 Fastest

1 0 Fast

0 1 Slow

1 1 Slowest



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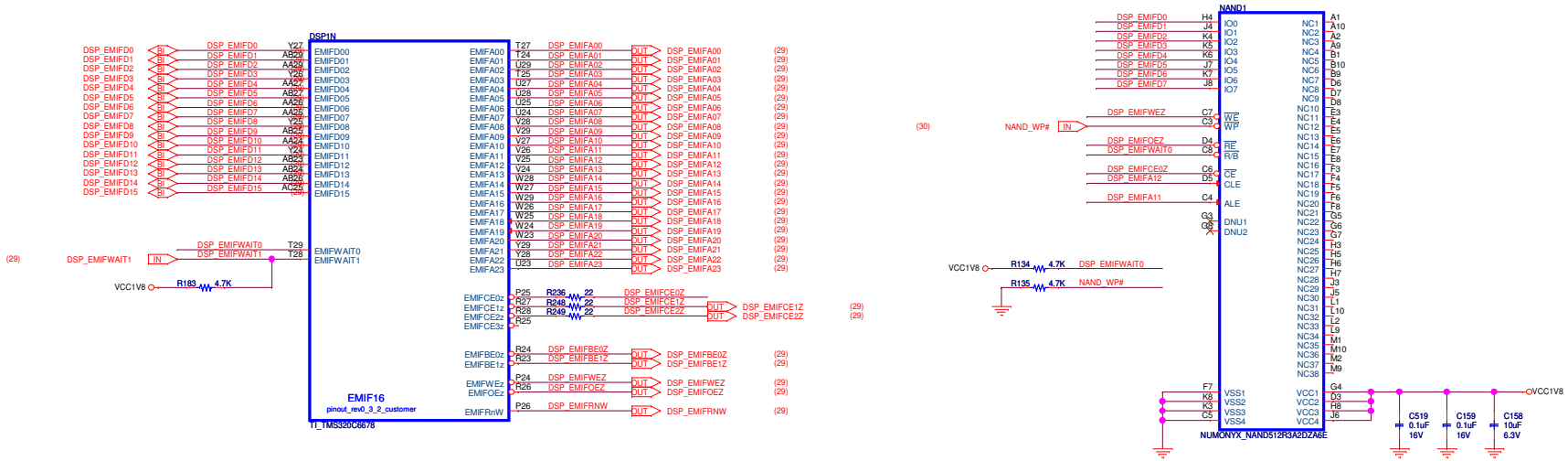

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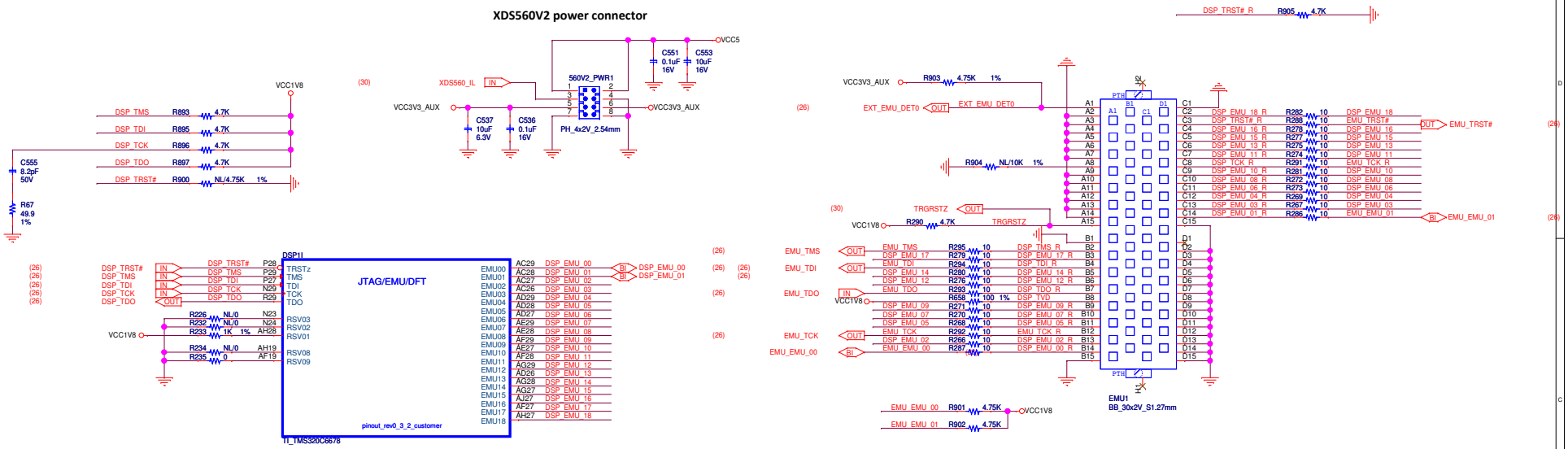
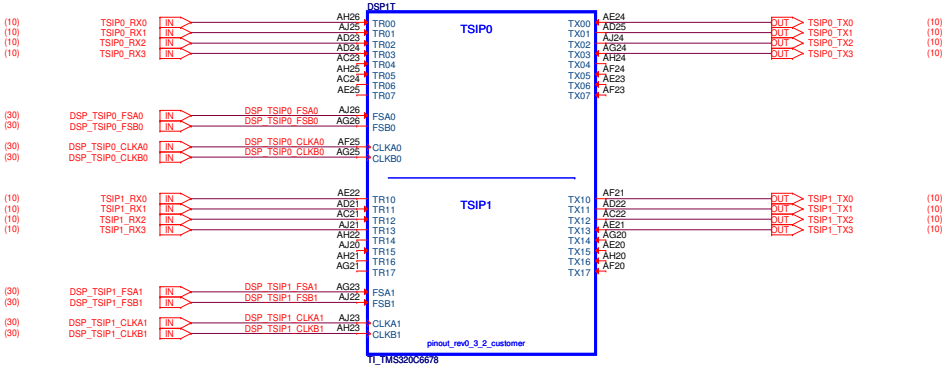
JTAG & EMU



TSIP0, 1



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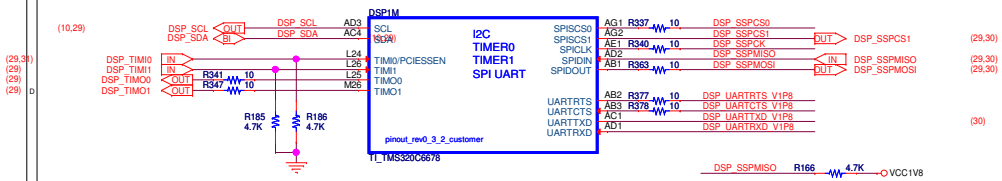
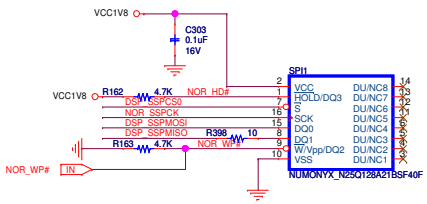
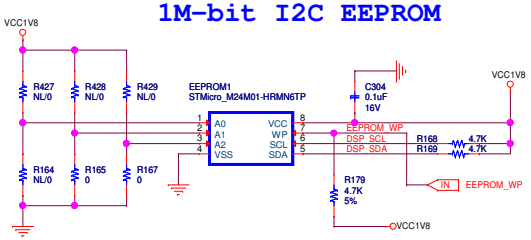
I2C, TIMER0,1, SPI, UART



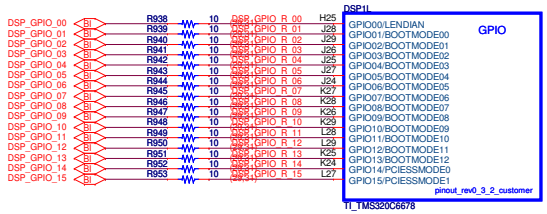
16M SPI NOR Flash

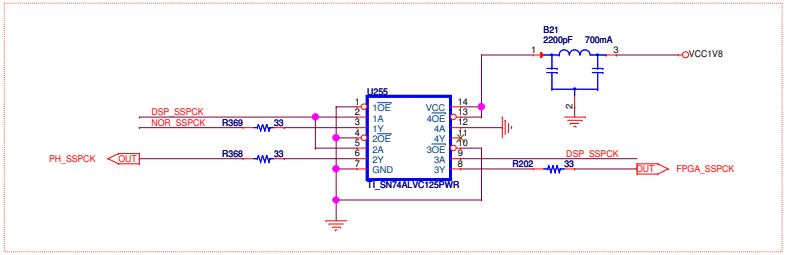


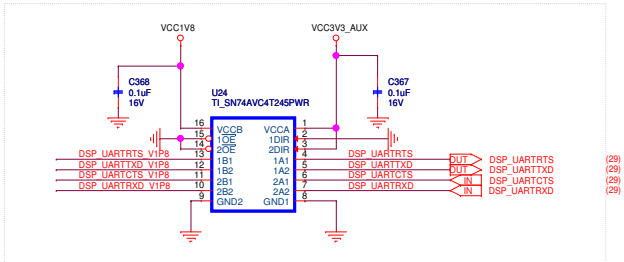
1M-bit I2C EEPROM



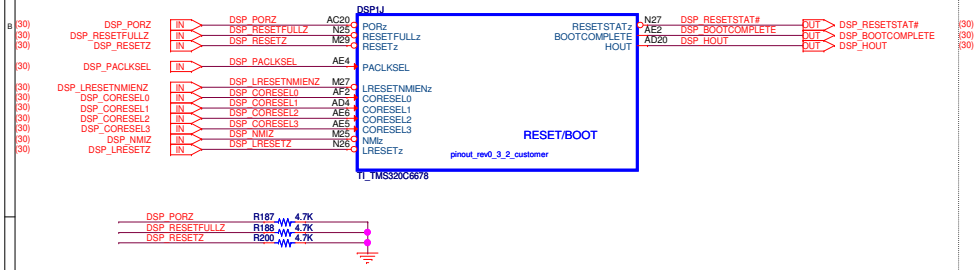
GPIO

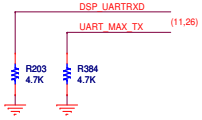


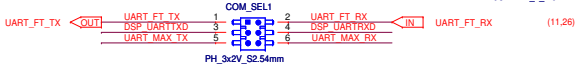




Reset Control

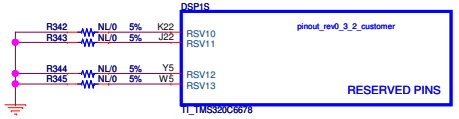


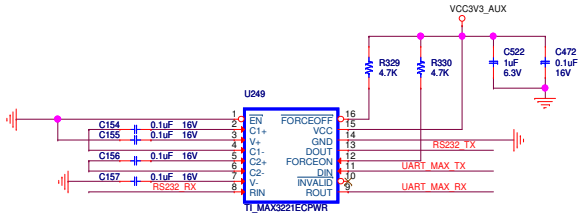


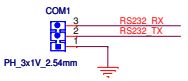


JP-UART(1-3) & (2-4) : UART over USB Connector (Default)
JP-UART(3-5) & (4-6) : UART over 3-Pin Header J5

Reserved







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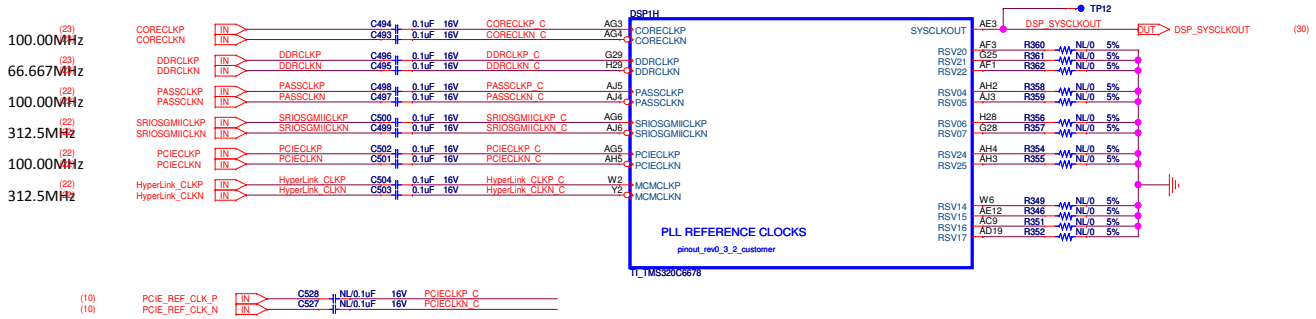
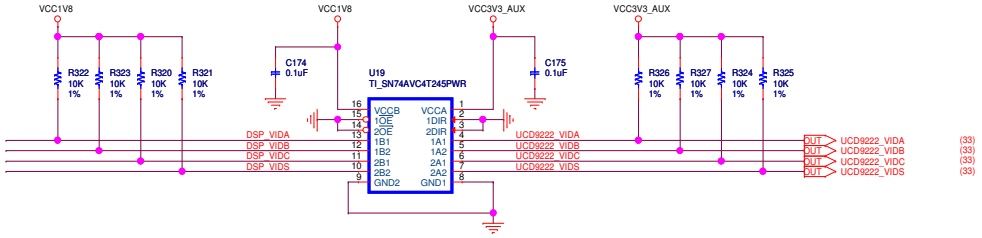
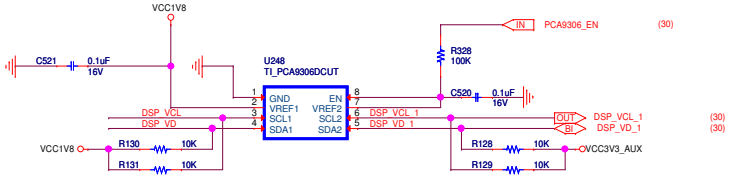
DSP CLOCK



"All DC-blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias"

Smart Reflex





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DSP_CLOCK_Smart Reflex		
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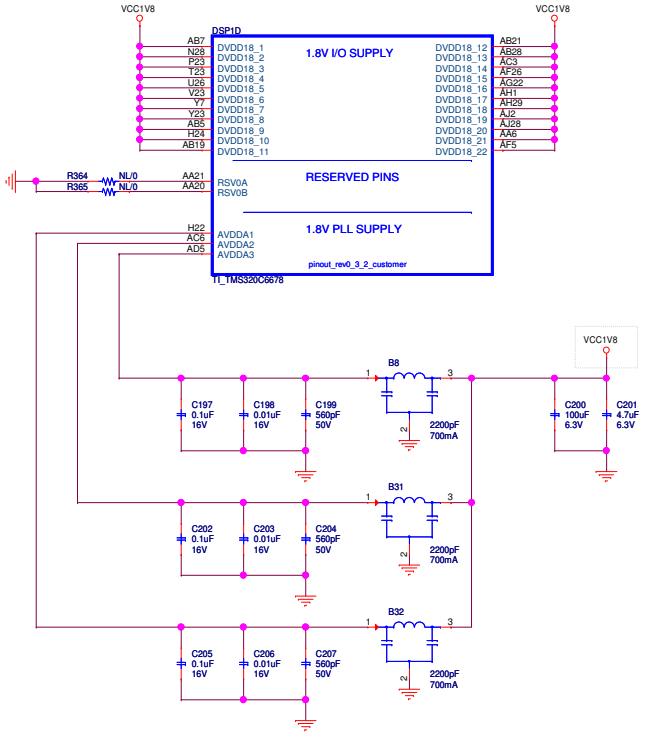
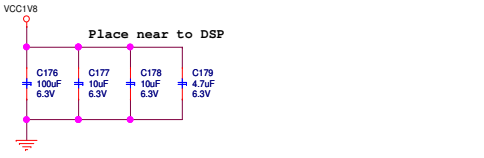
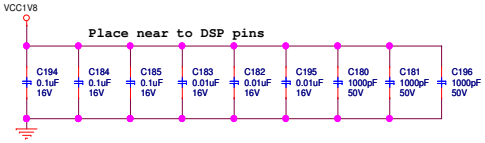
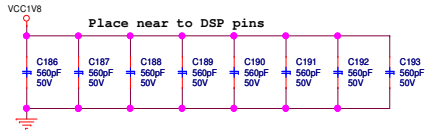
1.8V

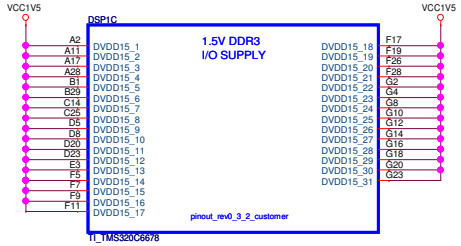


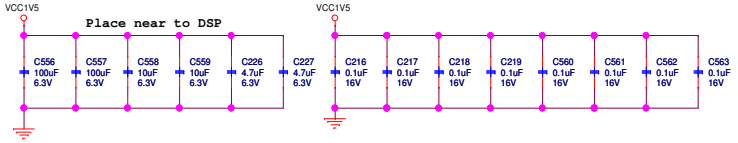


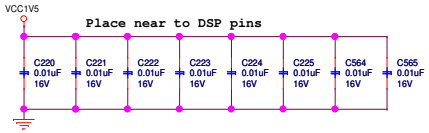


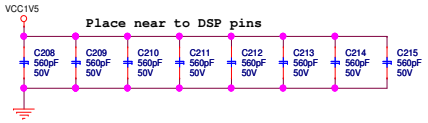


1.5V









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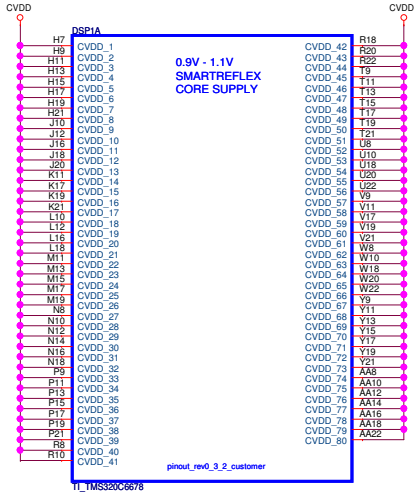
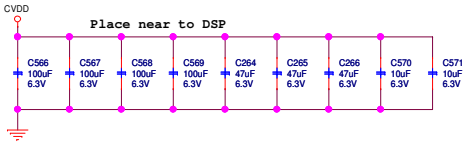
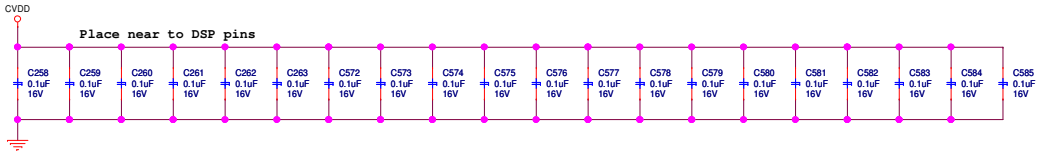
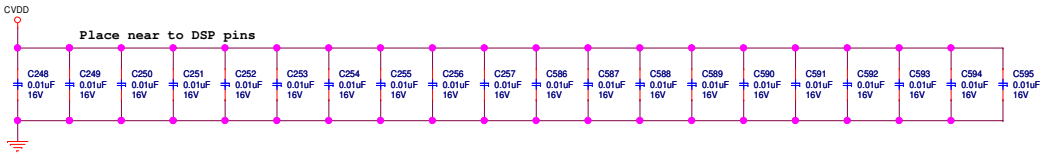
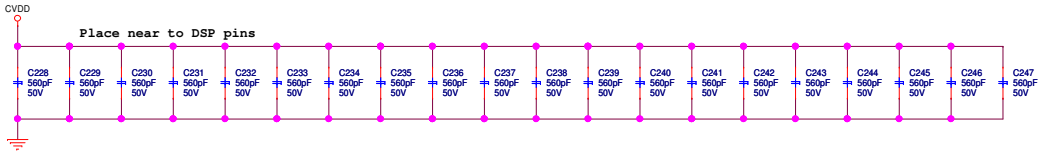
0.9V - 1.1V (Smart Reflex)



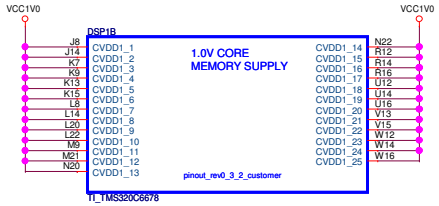


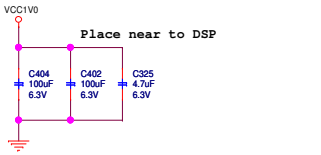


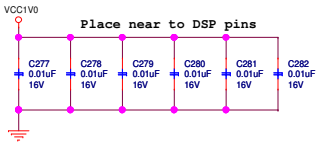


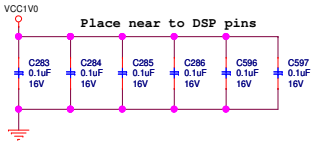


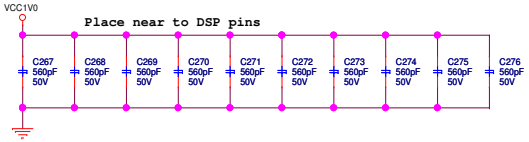
VCC1V0











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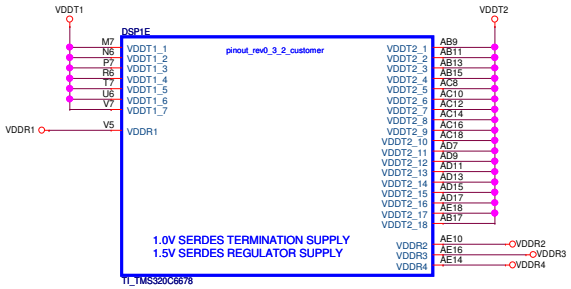
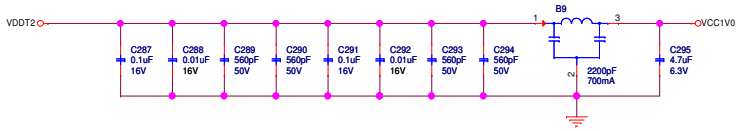
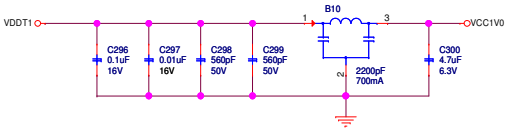
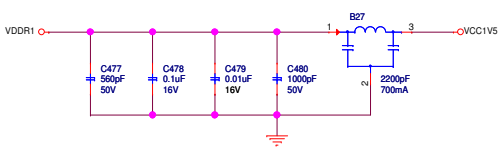
1.0V & 1.5V for Serdes

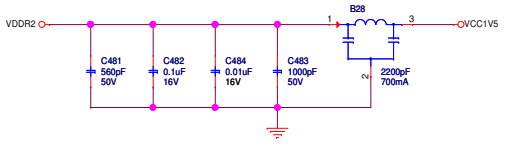


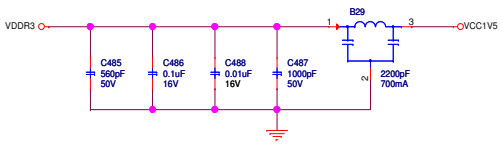
Place near to DSP pins

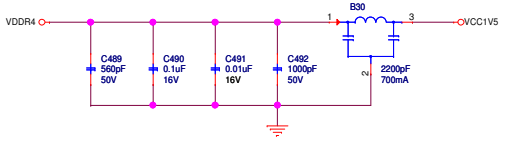












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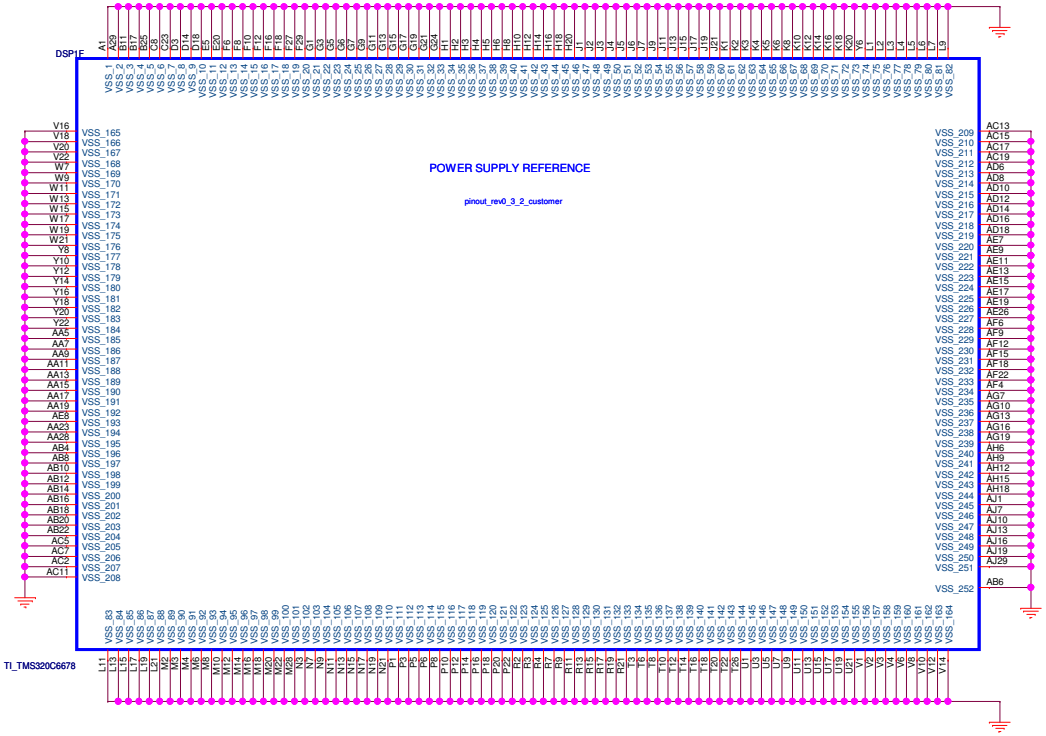

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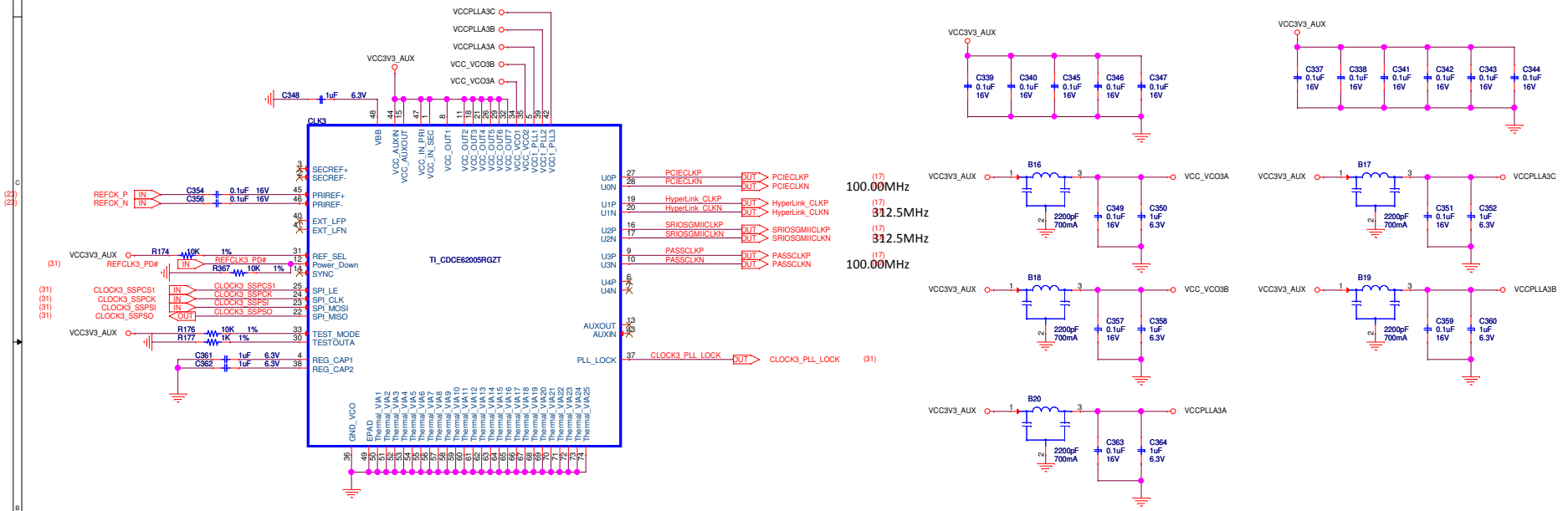
CLOCK GEN1



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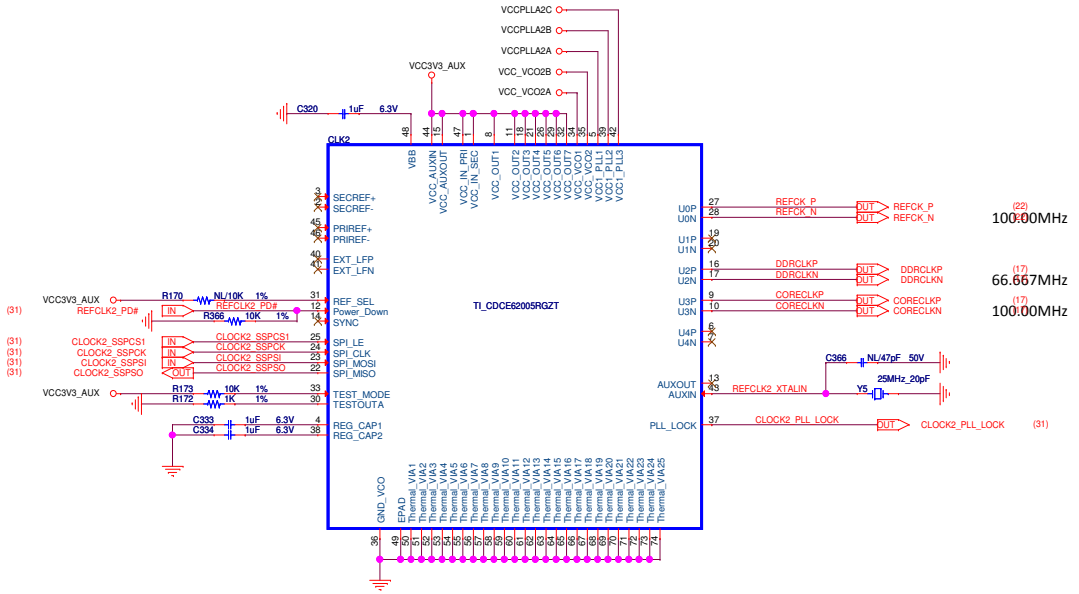
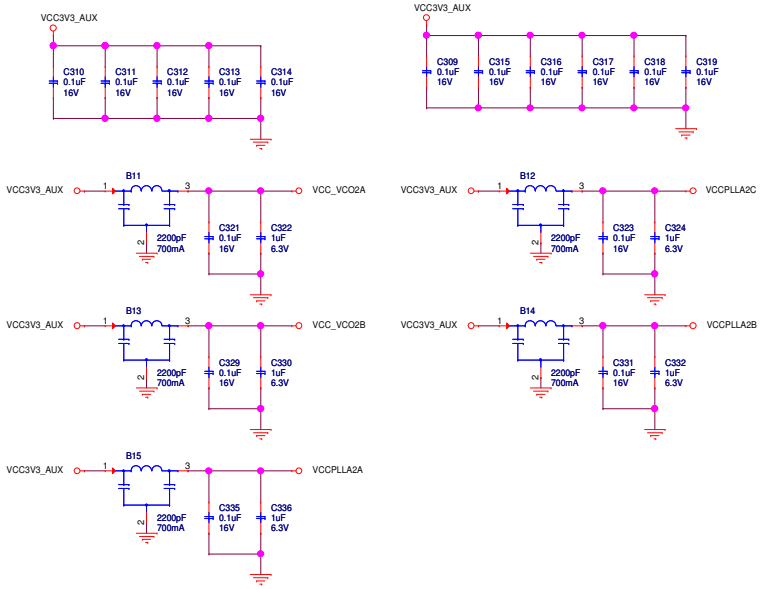
CLOCK GEN2





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Title	CLOCK GEN2	
Size: C	Document Number: DSPM-8301E	Rev: A101-1
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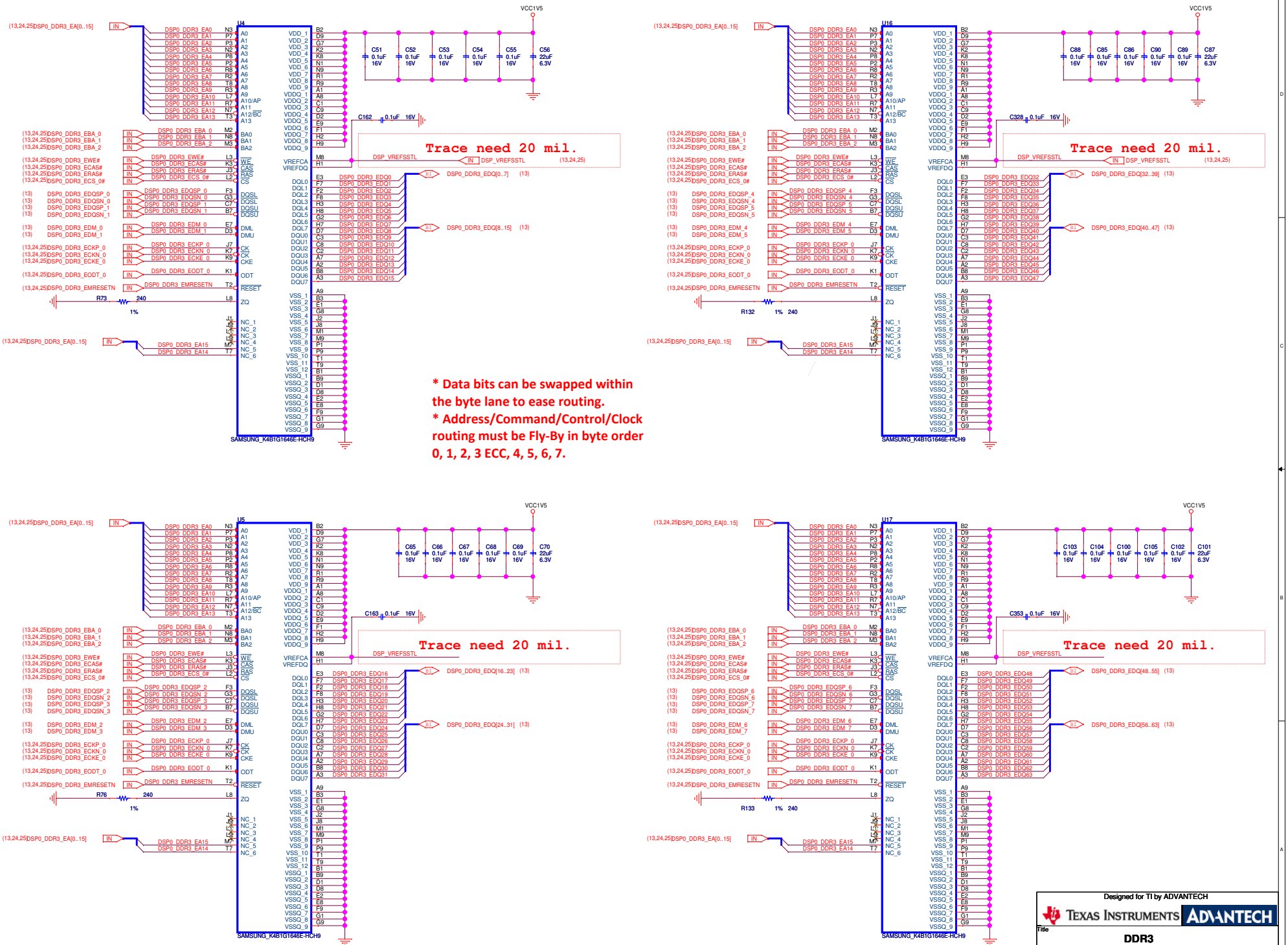
VCC1V5
U4
U16
U5
U17
SAMSUNG_K4B1G1646E-HCH9
Trace need 20 mil.
DSP_VREFSSTL
R73 240 1%
R132 1% 240
R76 240 1%
R133 1% 240
* Data bits can be swapped within the byte lane to ease routing.
* Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.
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Title
DDR3
Size C
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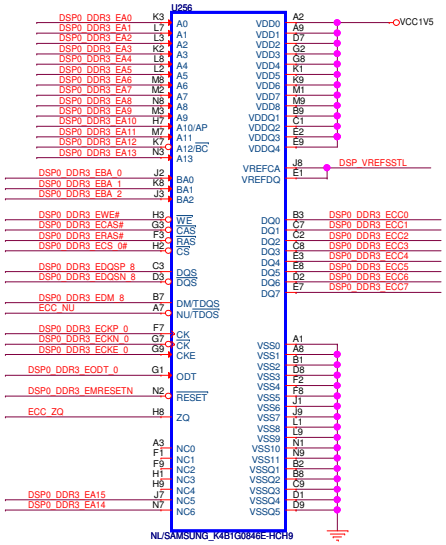
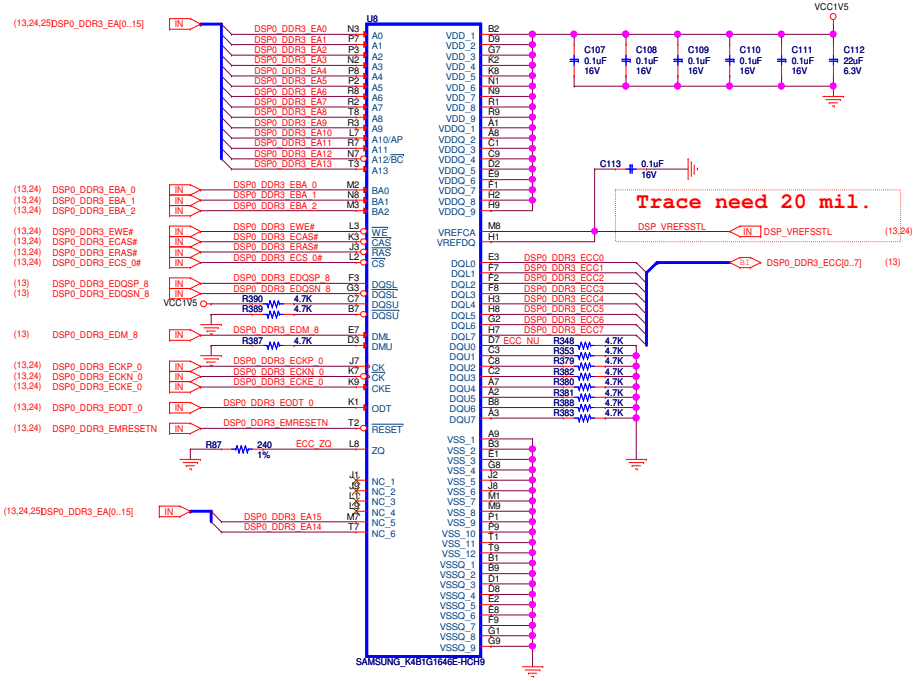
CO-LAYOUT

ECC Populated for 2Gb size.





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Title		
DDR3_ECC		
Size: C	Document Number: DSPM-8301E	Rev: A101-1
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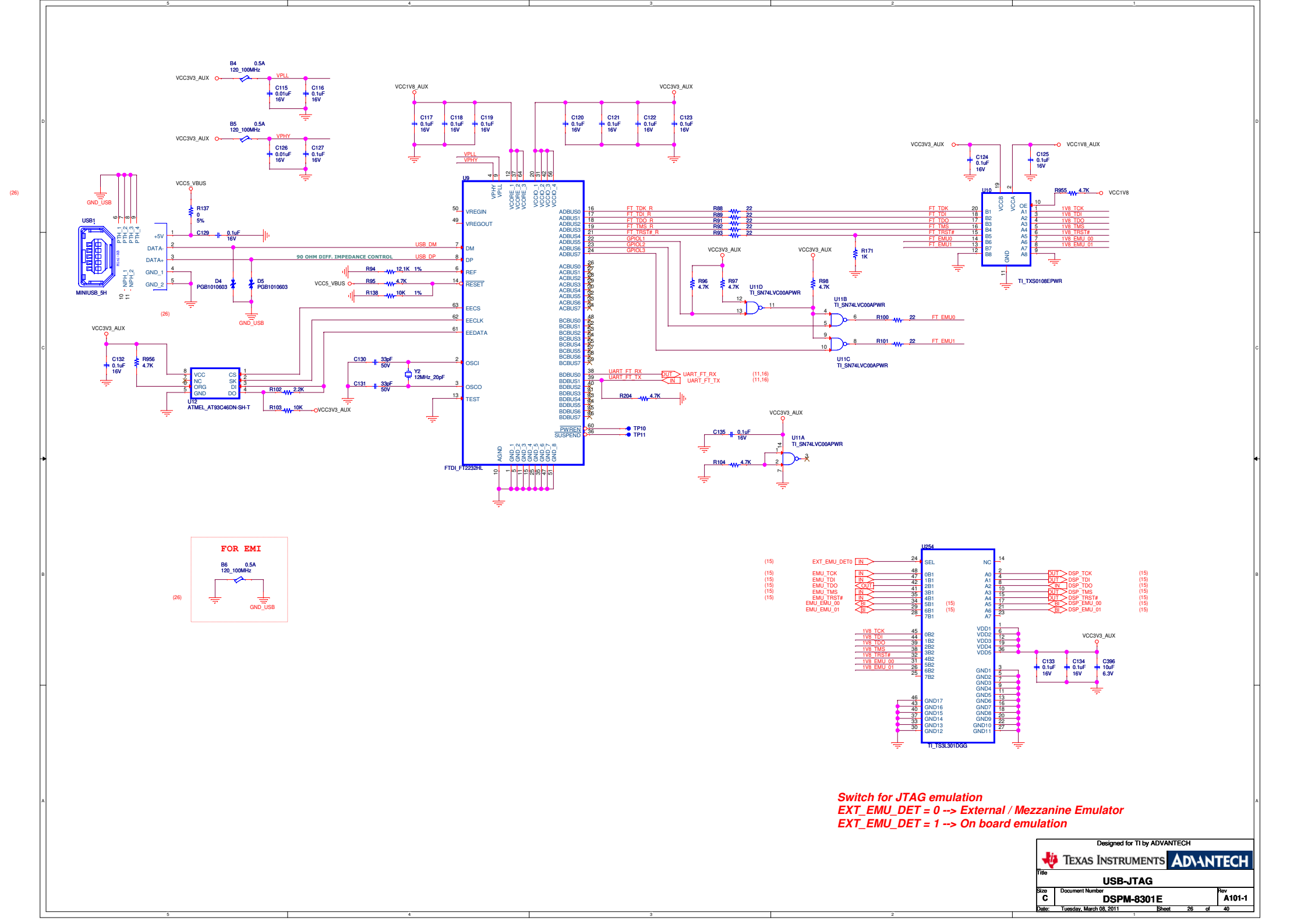
B4 0.5A 120_100MHz
VCC3V3_AUX
VPLL
C115 0.01uF 16V
C116 0.1uF 16V
B5 0.5A 120_100MHz
VPHY
C126 0.01uF 16V
C127 0.1uF 16V
VCC1V8_AUX
C117 0.1uF 16V
C118 0.1uF 16V
C119 0.1uF 16V
C120 0.1uF 16V
C121 0.1uF 16V
C122 0.1uF 16V
C123 0.1uF 16V
C124 0.1uF 16V
C125 0.1uF 16V
VCC5_VBUS
R137 0 5%
USB1
MINIUSB_SH
C129 0.1uF 16V
D4 PGB1010603
D5 PGB1010603
GND_USB
90 OHM DIFF. IMPEDANCE CONTROL
USB_DM
USB_DP
R94 12.1K 1%
R95 4.7K
R138 10K 1%
U9
FTDI_FT2232HL
VREGIN
VREGOUT
DM
DP
REF
RESET
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
PWREN
SUSPEND
U12
ATMEL_AT93C46DN-SH-T
C132 0.1uF 16V
R956 4.7K
R102 2.2K
R103 10K
C130 33pF 50V
C131 33pF 50V
Y2 12MHz_20pF
FT_TDK_R
FT_TDI_R
FT_TDO_R
FT_TMS_R
FT_TRST#_R
GPIOL1
GPIOL2
GPIOL3
R88 22
R89 22
R91 22
R92 22
R93 22
U10
TI_TXS0108EPWR
FT_TDK
FT_TDI
FT_TDO
FT_TMS
FT_TRST#
FT_EMU0
FT_EMU1
R955 4.7K
1V8_TCK
1V8_TDI
1V8_TDO
1V8_TMS
1V8_TRST#
1V8_EMU_00
1V8_EMU_01
R171 1K
R96 4.7K
R97 4.7K
R98 4.7K
U11D
TI_SN74LVC00APWR
U11B
TI_SN74LVC00APWR
U11C
TI_SN74LVC00APWR
R100 22
R101 22
FT_EMU0
FT_EMU1
UART_FT_RX
UART_FT_TX
R204 4.7K
TP10
TP11
U11A
TI_SN74LVC00APWR
C135 0.1uF 16V
R104 4.7K
FOR EMI
B6 0.5A 120_100MHz
U25A
TI_TSSL301DGG
EXT_EMU_DET0
EMU_TCK
EMU_TDI
EMU_TDO
EMU_TMS
EMU_TRST#
EMU_EMU_00
EMU_EMU_01
DSP_TCK
DSP_TDI
DSP_TDO
DSP_TMS
DSP_TRST#
DSP_EMU_00
DSP_EMU_01
C133 0.1uF 16V
C134 0.1uF 16V
C396 10uF 6.3V
Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation
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Title
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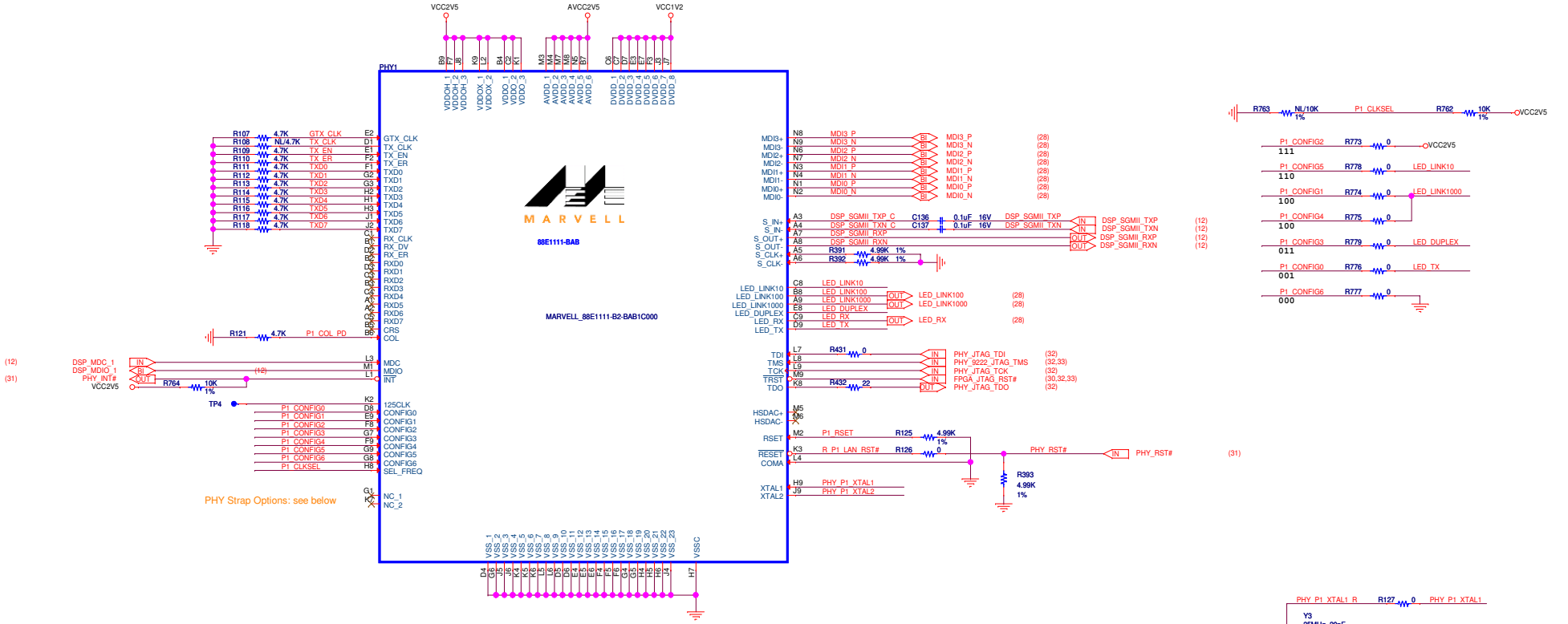

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

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Title: Gigabit Ethernet PHY

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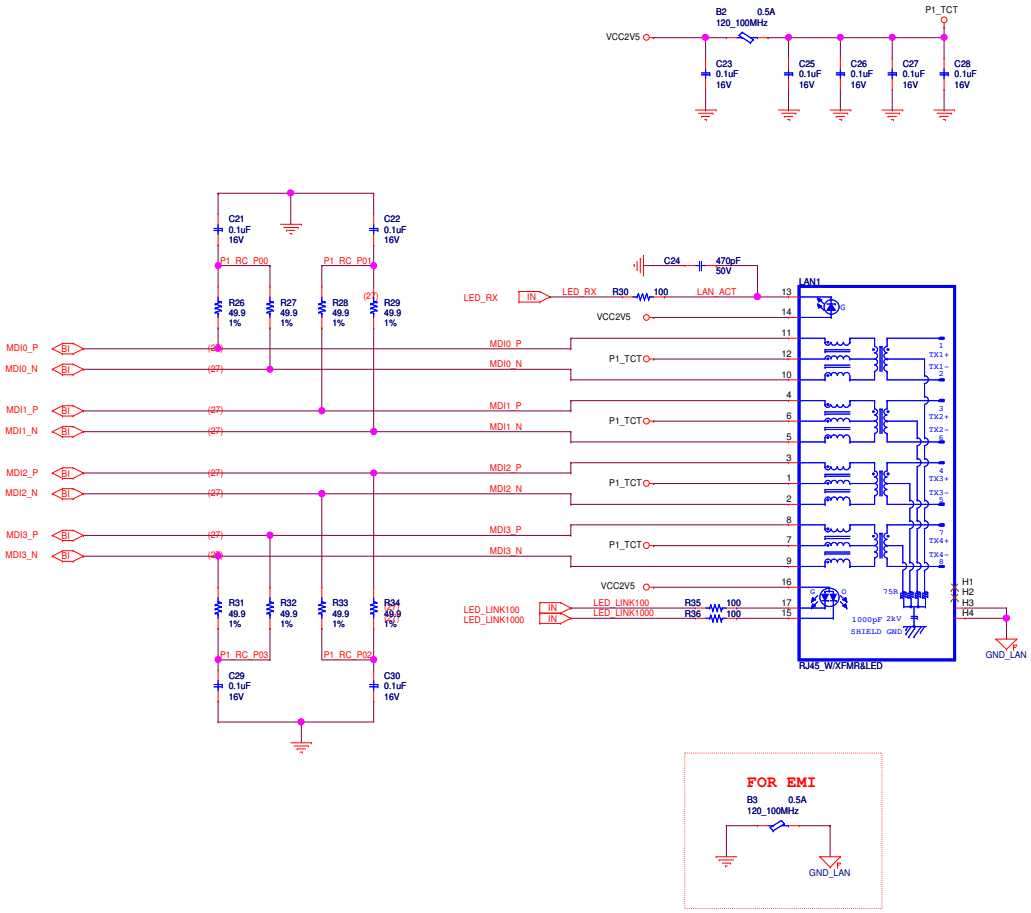
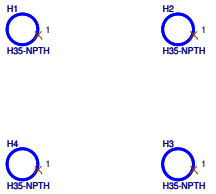
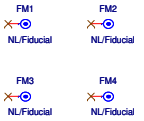
RJ-45

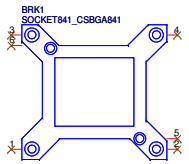


Heatsink Holes



On board





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RJ45		
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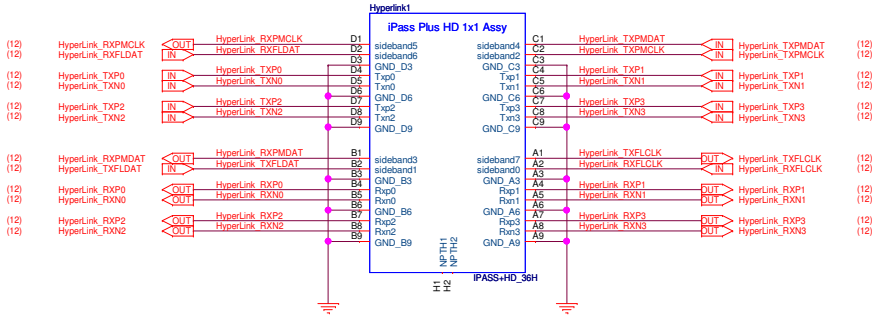
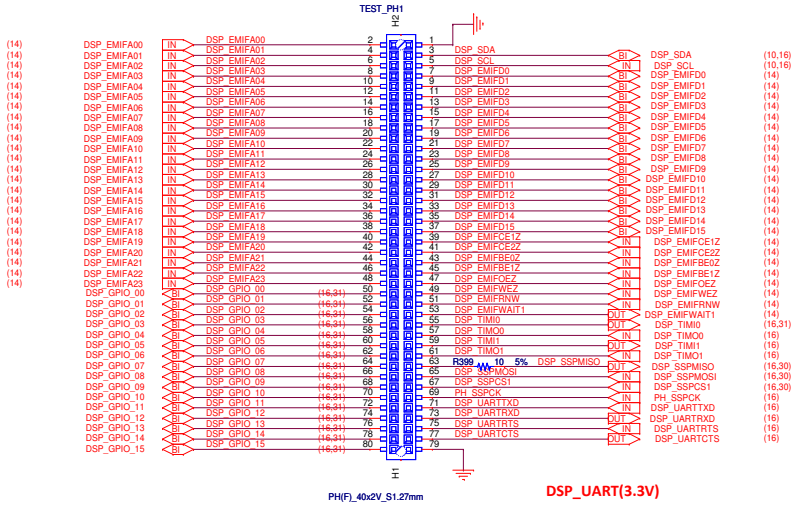
IPASS+HD for HyperLink Bus connection



Pin Header for debug

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS



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Title	Connectors for HyperLink & Debug	
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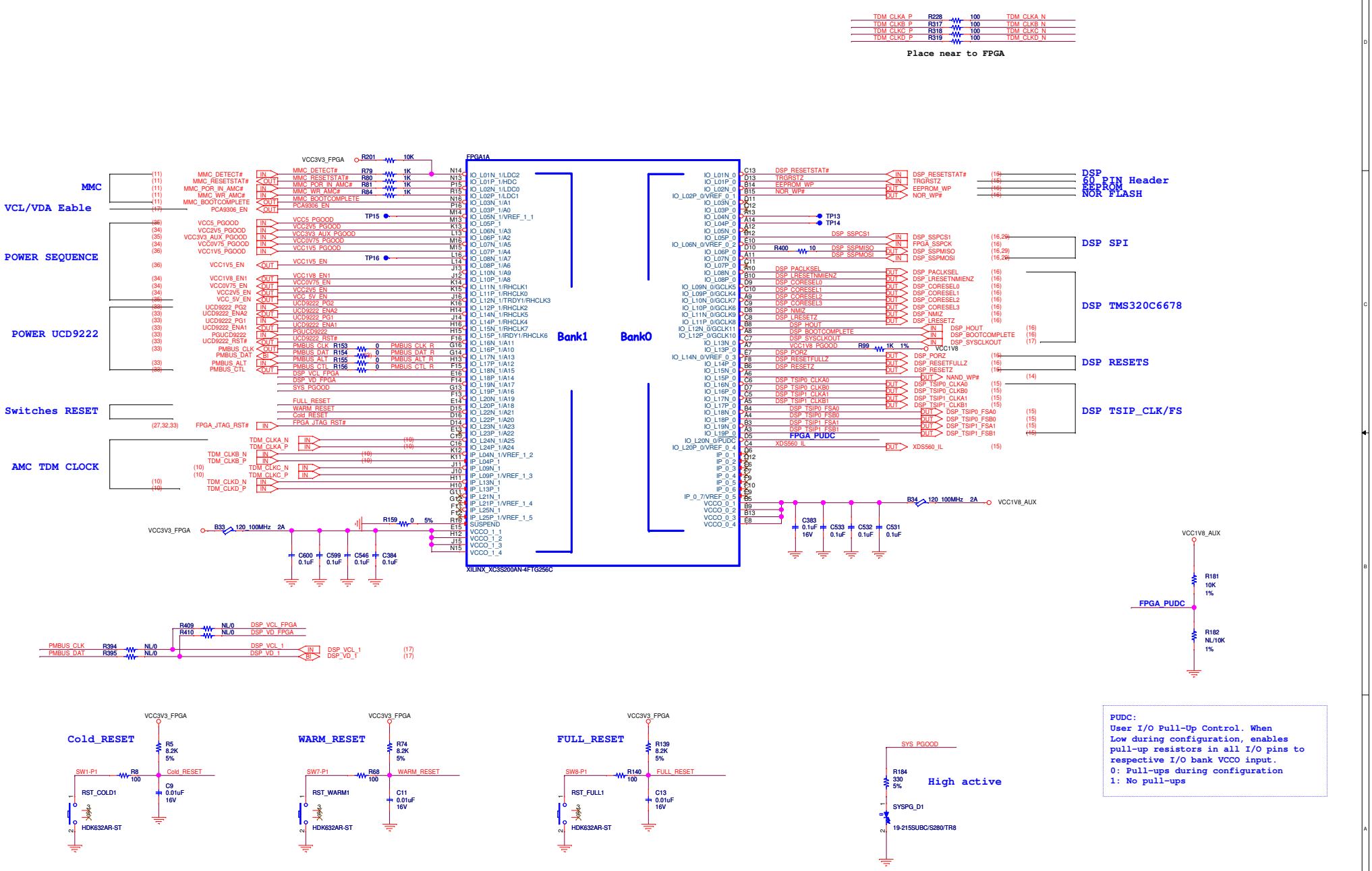
Place near to FPGA
MMC
VCL/VDA Eable
POWER SEQUENCE
POWER UCD9222
Switches RESET
AMC TDM CLOCK
FPGA1A
Bank1
Bank0
XILINX_XC3S200AN-4FTG256C
DSP
60 PIN Header
EEPROM
NOR FLASH
DSP SPI
DSP TMS320C6678
DSP RESETS
DSP TSIP_CLK/FS
FPGA_PUDC
Cold_RESET
WARM_RESET
FULL_RESET
High active
PUDC:
User I/O Pull-Up Control. When
Low during configuration, enables
pull-up resistors in all I/O pins to
respective I/O bank VCCO input.
0: Pull-ups during configuration
1: No pull-ups
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TEXAS INSTRUMENTS
ADVANTECH
Title
FPGA_XC3S200AN_A
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C
Document Number
DSPM-8301E
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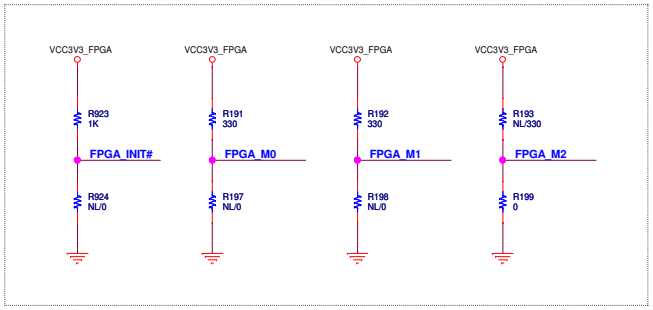
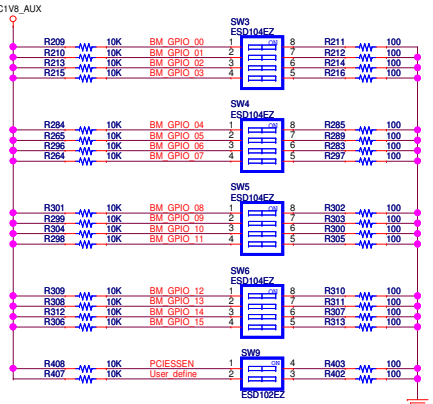
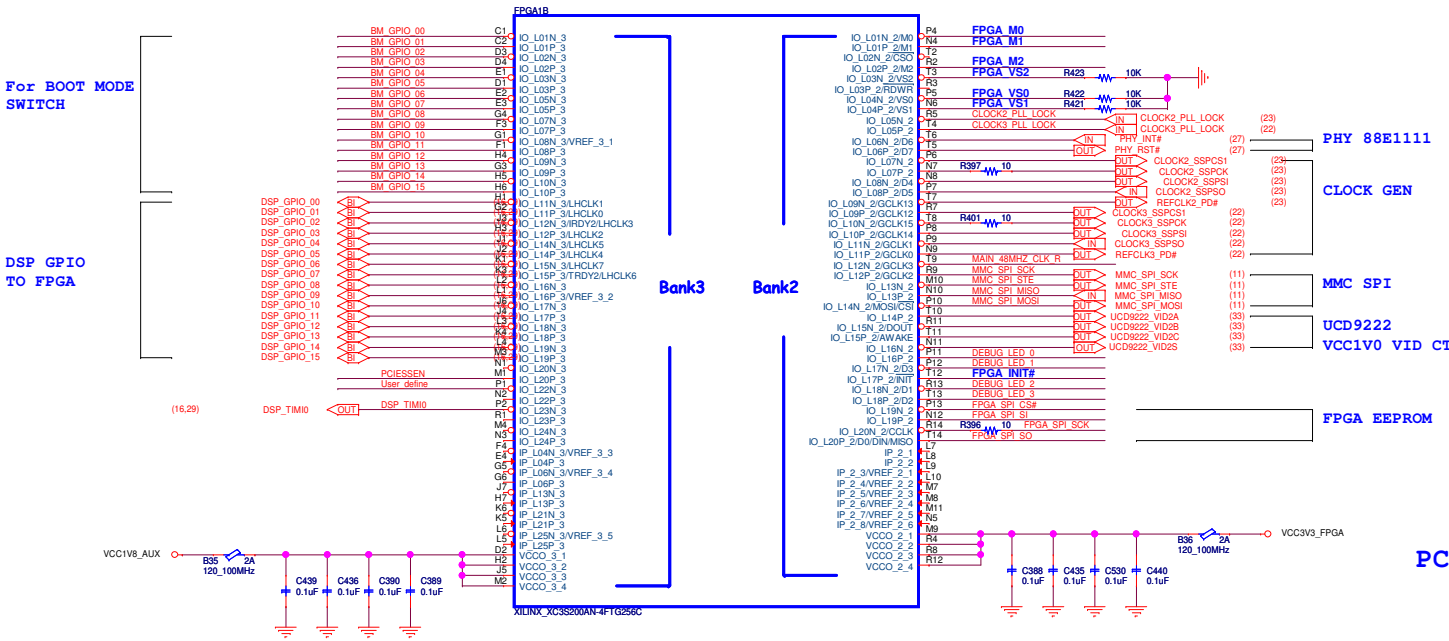
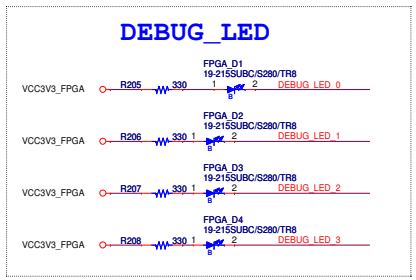
BOOT STRAP CONFIGURATION

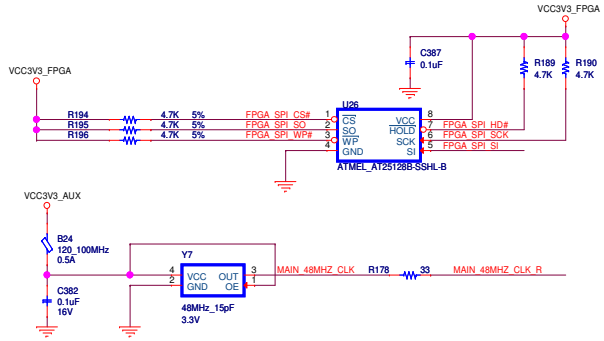
default value : TBD











Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function	
			Pull Up	Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian	Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device	
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device	
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device	
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg	
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg	
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg	
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg	
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg	
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg	
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg	
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C	
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C	
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C	
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex	
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex	

Boot Device

BM_GPIO 3 2 1	BOOT Device	NOTE
0 0 0	EMIF16	
0 0 1	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCIe	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

Device Configuration

BM_GPIO [10:4]	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.

PLL Settings

BM_GPIO 13 12 11	INPUT CLK (MHz)	CorePac System PLL Configuration
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

PCIe Mode selection(PCIESSMODE[1:0])

BM_GPIO[15:14] INPUT	Description
00b	PCIe in End-point mode
01b	PCIe in Legacy End-point mode(no support for MSI)
10b	PCIe in Legacy Root complex mode

PCIESSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIE subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIE subsystem is enabled

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TEXAS INSTRUMENTS ADVANTECH

Title: FPGA_XC3S200AN_B

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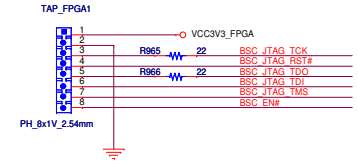
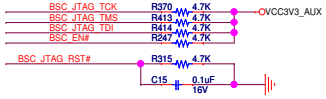
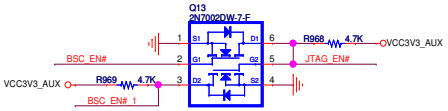
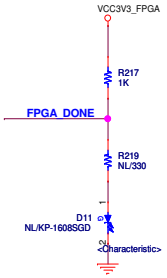
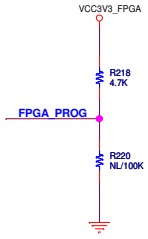
FPGA JTAG



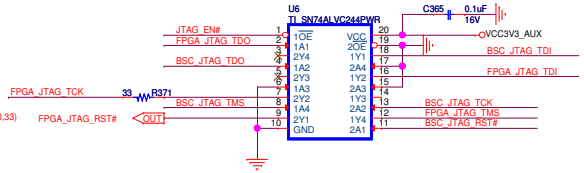


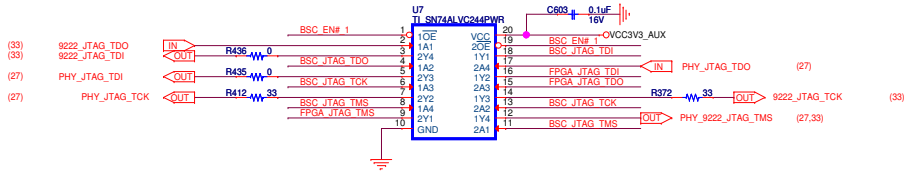






During Configuration :
Must be High to allow
configuration to start.





For boundary scan by pass test

Always enabling :

BSC_JTAG_RST# --> FPGA_JTAG_RST#.
BSC_JTAG_TCK --> FPGA_JTAG_TCK

When BSC_EN# = 1:

JTAG port (CN10) is only for FPGA debug and programming.

BSC_JTAG_TDO --> FPGA_JTAG_TDI
BSC_JTAG_TDI <-- FPGA_JTAG_TDO
BSC_JTAG_TMS --> FPGA_JTAG_TMS

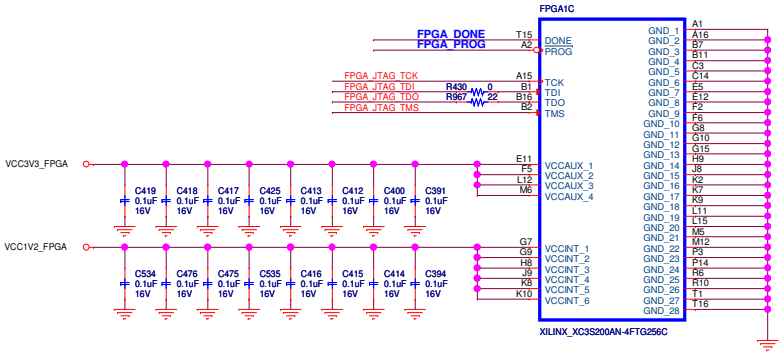
When BSC_EN# = 0:

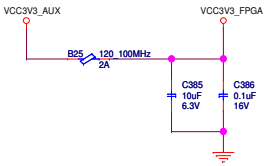
JTAG port (CN10) is a boundary scan feature.
The sequence is FPGA, 88E1111, then UCD9222.

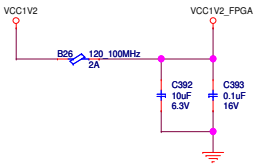
BSC_JTAG_TCK --> FPGA_JTAG_TCK

BSC_JTAG_TCK --> 9222_JTAG_TCK

BSC_JTAG_TMS --> PHY_9222_JTAG_TMS
BSC_JTAG_TCK --> PHY_JTAG_TCK
BSC_JTAG_TDO --> FPGA_JTAG_TDI
FPGA_JTAG_TDO --> PHY_JTAG_TDI
PHY_JTAG_TDO --> 9222_JTAG_TDI
9222_JTAG_TDO --> BSC_JTAG_TDI







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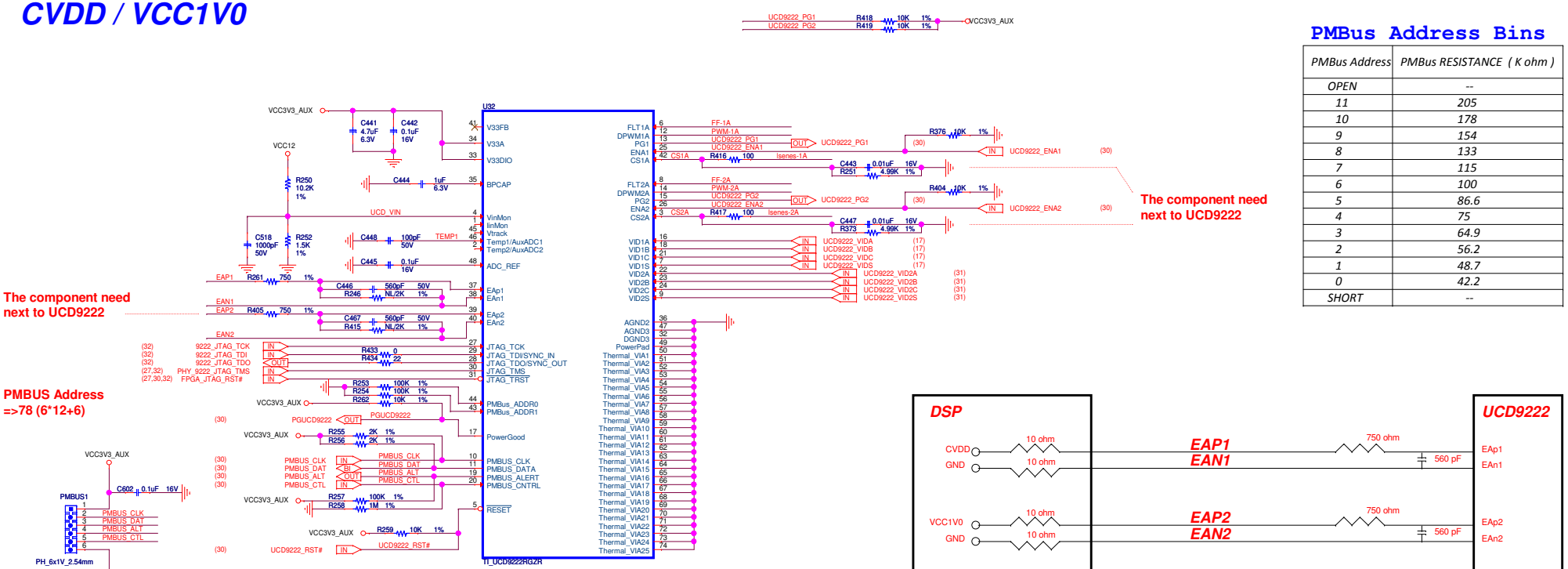
CVDD / VCC1V0



PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Each 22uF Cin cap needs to tightly coupled to Vin and PGND of the UCD7242.

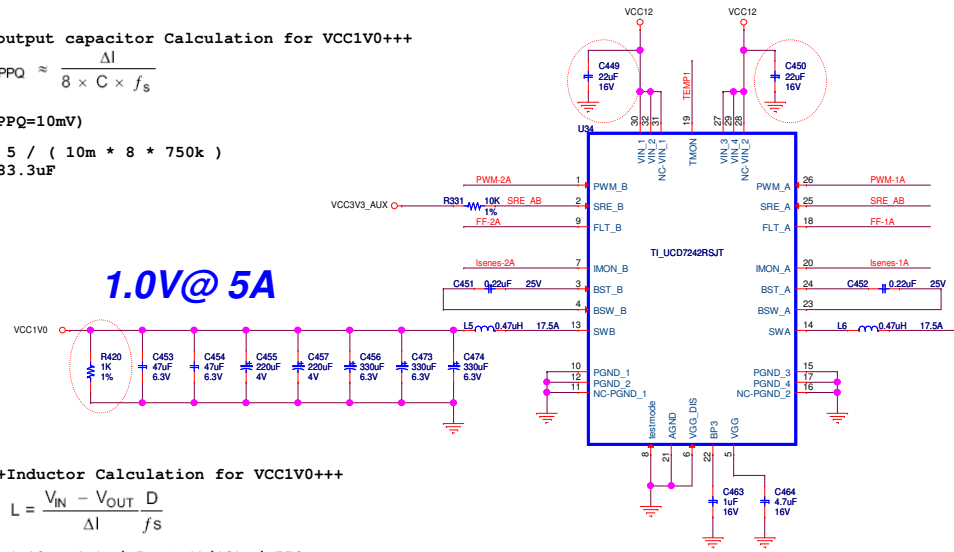
+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

C= 5 / (10m * 8 * 750k)
C=83.3uF

1.0V@ 5A

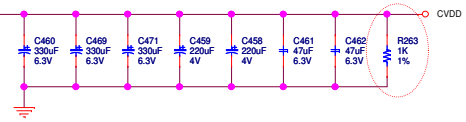


+++Inductor Calculation for VCC1V0+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{fs}$$

L= (12 - 1) / 5 * (1/12) / 750K
L= (11 / 5) * (0.083 / 750K)
L= 0.243 uH

DSP Vcore @8A



+++Inductor Calculation for CVDD+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{fs}$$

L= (12 - 1) / (8) * (1/12) / 750K
L= (11 / 8) * (0.083 / 750K)
L= 0.152 uH

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

C= 8 / (10m * 8 * 750k)
C= 133.3uF

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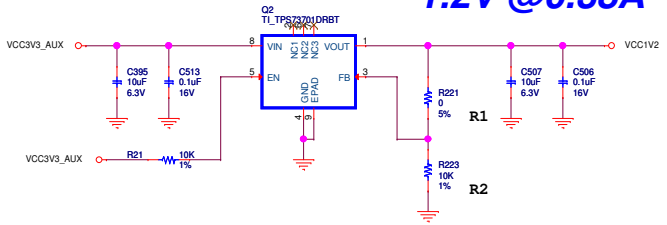
VCC1V2

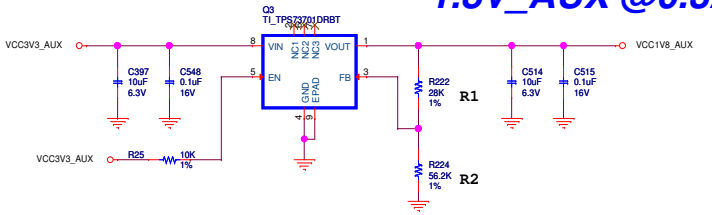
1.2V @0.38A



Vout=(R1+R2)/R2*1.204
1.204V = (0+10k)/10k*1.204

VCC1V8_AUX

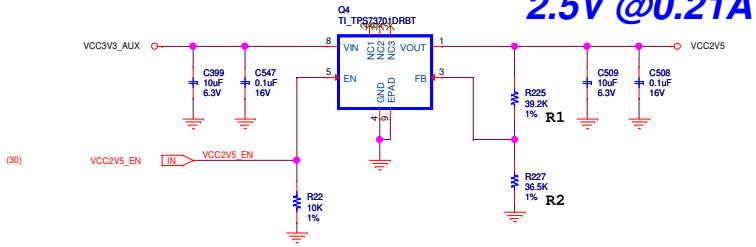
1.8V_AUX @0.3A



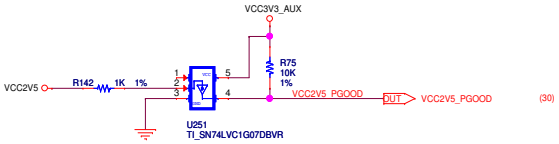
Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC2V5

2.5V @0.21A

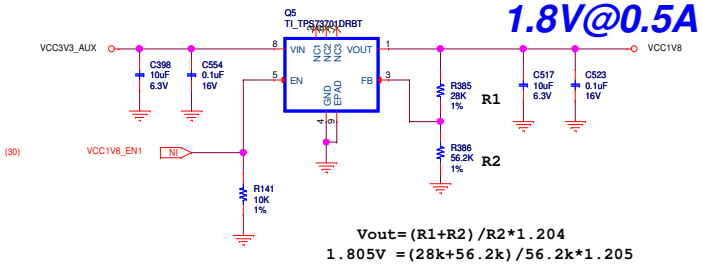


Vout=(R1+R2)/R2*1.204
2.50V =(39.2k+36.5k)/36.5k*1.204



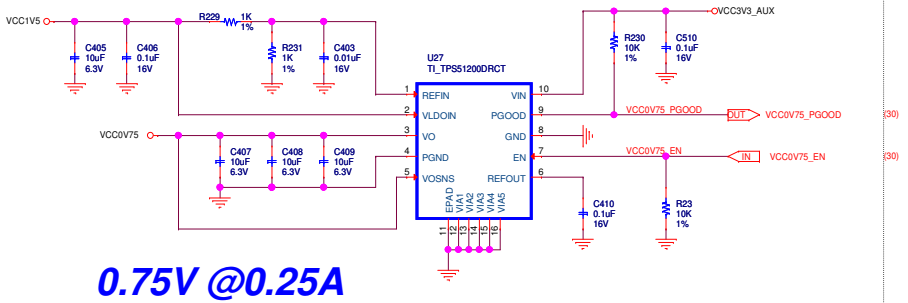
VCC1V8

1.8V@0.5A



Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC0V75



0.75V @0.25A

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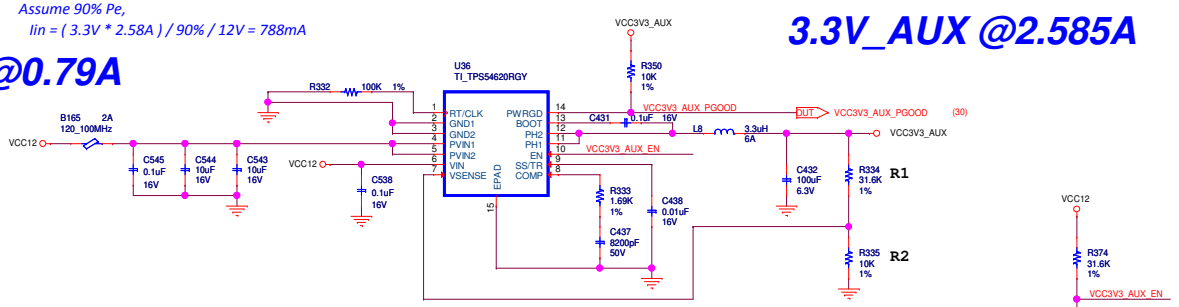
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.585A



Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)

+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2.58)/(1MHz*0.0825)
Cout=(5.16)/(82500)
Cout=63uF
Reference Capacitor=100uF

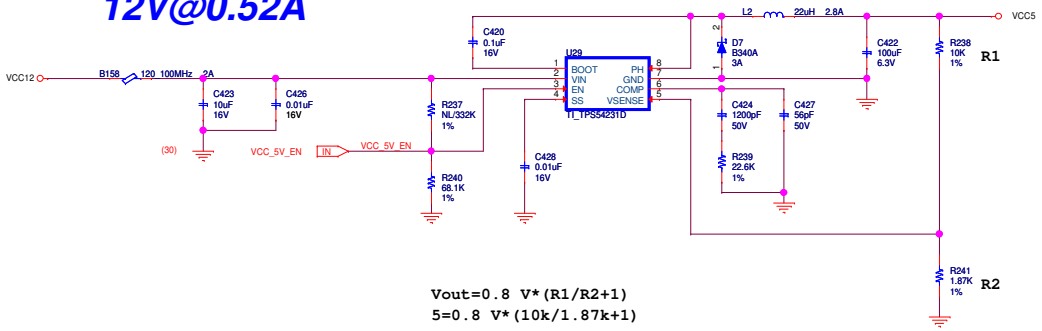
+++Inductor Calculation+++ (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12.6 - 3.3)/2.58 * Kind) * (3.3 / (12.7 * 1MHz))
L = ((9.3/2.58 * 0.3) * (3.3 / (12.7M))
L = (9.3/0.774) * (0.26M)
L = 3.12uH
Reference Inductor 3.3uH

VCC5

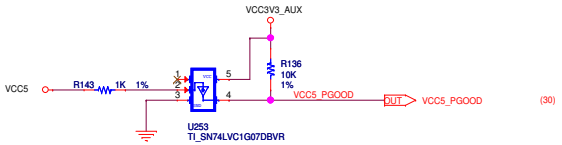
Assume 80% Pe,
*Iin = (5V * 1A) / 80% / 12V = 520mA*

12V@0.52A

5V @1A



Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)



+++output capacitor Calculation+++

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max})$$

Cout=1/(2 * 3.14 * 5 * 25K)
Cout=1.3 uf
Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12.6 - 5)/1 * Kind) * (5 / (12.7 * 570K))
L = ((7.6/ 0.3) * (5 / (7239K))
L = (25.3) * (0.69M)
L = 17.5uH
Reference Inductor 22uH

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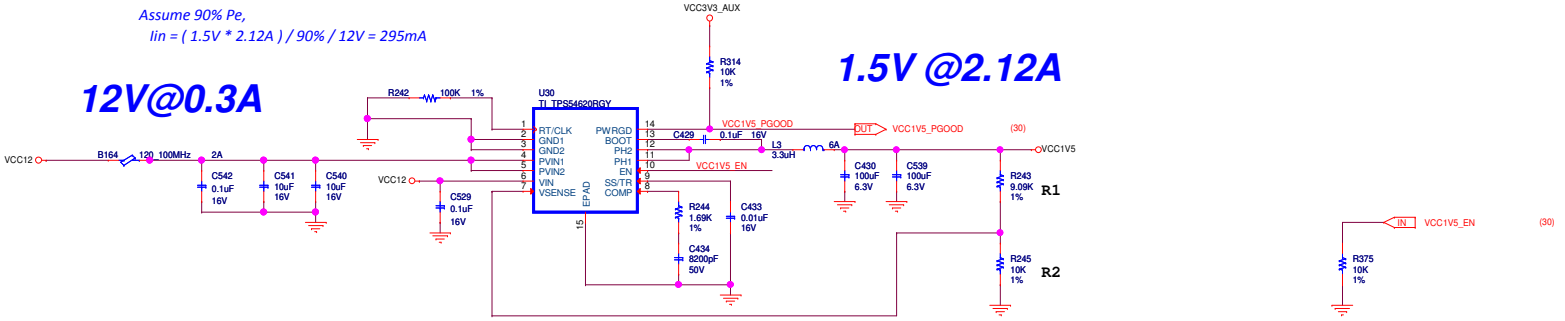
VCC1V5

Assume 90% Pe,
*Iin = (1.5V * 2.12A) / 90% / 12V = 295mA*

12V@0.3A

1.5V @2.12A



Vout=0.8 V*(R1/R2+1)

1.52=0.8 V*(9.09k/10k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)

+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2.12)/(1MHz*0.0375)
Cout=(4.24)/(37500)
Cout=113uF
Reference Capacitor=100uF*2=200uF

+++Inductor Calculation+++ (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12.6 - 1.5)/2.12 * Kind) * (1.5 / (12.7M))
L = ((11.1/2.12 * 0.3) * (1.5 / (12.7M))
L = (11.1/0.636) * (0.12M)
L = 2.09uH
Reference Inductor 3.3uH

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