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AMD E8870 4GB PCIEX16

Mini DP X4 Low profile

ER24FL-SK4

GFX-AE8870L16-5J

MPN : 1A1-E000236ADP

Embedded PCIe Graphics

4 x Mini DP with cable locking

AMD RADEON GRAPHICS

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1. Specification

Model Name	GFX-AE8870L16-5J
Graphics Engine	AMD Radeon E8870
Process Node	28 nm
Engine Clock (max)	1000 MHz
Graphics Memory	128-bit, 4 GB GDDR5
Memory Clock (max)	1500 MHz / 6.0 Gbps
Bus Interface	PCI Express® 3.0 (x16)
Shader Processing Units	768 Shaders
Floating Point Performance	1536 GFLOPs
DirectX® Capability	DirectX® 11.2
Shader Model	Shader Model 5.0
OpenGL™	OpenGL™ 4.3
OpenCL™	OpenCL™ 1.2
Unified Video Decoder (UVD)	UVD4.2 for H.264, VC-1, MPEG-2 MPEG-4 part 2 decode
Display Interface	4 x Mini DP with cable locking
Multi display	X4
Power Consumption	75 W
Operating Temperature	0°C ~ 55°C
Dimension	168 x 69 mm

2. Functional Overview

2.1. Memory Interface

AMD Radeon E8870 has four DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel, and must run at the same voltage.

Supported DRAM Component Organizations:

- 4, 8, or 16 banks (2, 3, or 4 bank bits). Single- or dual-rank.
- Rows: 1024, 2048, 4096, 8192, 16384, 32768, or 65536 (10, 11, 12, 13, 14, 15, or 16 bits).
- Columns: 256, 512, 1024, or 2048 (8, 9, or 10 bits).
- CS (chip select): 1 or 2.

2.2. Acceleration Features

- Support for all DirectX® 11.2 features, including the full-speed 32-bit floating point per component operation.
- Shader Model 5.0 geometry and pixel support in a unified shader architecture.
- Support for OpenGL 4.3.
- Support for OpenCL™ 1.2
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).
- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Angle-invariant algorithm for improved quality.

- Single- or two-channel data format compatibility.
- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.3. Display System

The display system supports accelerated display modes on six independent display controllers as well as legacy VGA mode emulation and VESA Super VGA graphics display on two cloned display controllers with independent timings for each display. The full features of the display system are outlined in the following sections.

2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output when using dual-Link DVI up to 1920 × 1200 @ 60 Hz
- Supports industry-standard CEA-861-E video modes including 480p, 720p,1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—165 MP/s (megapixels per second) for single-link DVI
  - DVI—330 MP/s for dual-link DVI
  - HDMI—297 MP/s
- Compliant with the DVI electrical specification

2.5. DisplayPort Features

- Supports all the mandatory features of the DisplayPort Standard Version 1.2

and the following optional features:

- ACM packet-type support
- ISRC packet-type support
- Y-only colormetry

- DisplayPort Multi-streaming Transport (MST) allowing any number of display pipelines to drive a single DisplayPort interface (provided the DisplayPort link bandwidth is not exceeded)
- Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
  - Four, two, or one lane(s)
  - 5.4-, 2.7-, or 1.62-Gbps link-data rate per lane
  - The eDP mode port also supports the 3.24-Gbps link rate option
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth
- The following table shows the maximum pixel rates for four, two, or one lane(s) at 5.4-Gbps link rate.

	18 bpp	24 bpp	30 bpp
One Lane	240 MP/s	180 MP/s	144 MP/s
Two Lanes	480 MP/s	360 MP/s	288 MP/s
Four Lanes	597 MP/s	597 MP/s	576 MP/s

- Enhanced audio capabilities for DisplayPort 1.2:
  - Supports PCM audio rates up to 192 kHz.
  - Dolby-TrueHD bitstream and DTS-HD Master Audio bitstream capable.
  - Multiple independent audio streams allowing each DisplayPort display to support audio
    - HDMI display also gets its own independent audio stream
  - Supports Global Time Code (GTC) using the regular AUX channel—GTC master mode only.

2.6. Integrated HD-Audio Controller (Azalia) and Codec

- HD-audio HDMI, DisplayPort, and wireless display outputs.
- Multiple output stream DMAs.
- Maximum output bandwidth of 73.728 Mbit/s.

- Low power ECN support.
- Hardware silent stream.
- Function level reset.
- Compatible Microsoft® UAA driver support for basic audio.
- For advanced functionality (as follows), an AMD or a third party driver is required.
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR Compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD.
- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD.
- Plug-and-Play:
  - Sink audio format capabilities declaration.
  - Sink information.
  - AV association.
- Lip sync information.
- HDCP content protection

2.7. CRT DAC

- One integrated triple 10-bit DAC with built-in reference circuit, which takes output from either one of the internal display controllers (primary or secondary).
- A single RGB-CRT output.
- Support for the stereo-sync signal to drive a 3D display.
- A maximum pixel frequency of 400 MHz.
- An individual power-down feature for each of the three guns.
- Compliant with the VSIS electrical specification.
- Integrated with a built-in bandgap reference circuitry.
- A static detection circuitry (S_detect) for hot-plug/unplug capability
- An integrated static monitor-detection circuit

2.8. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.

- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

3. PIN Assignment and Description

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground

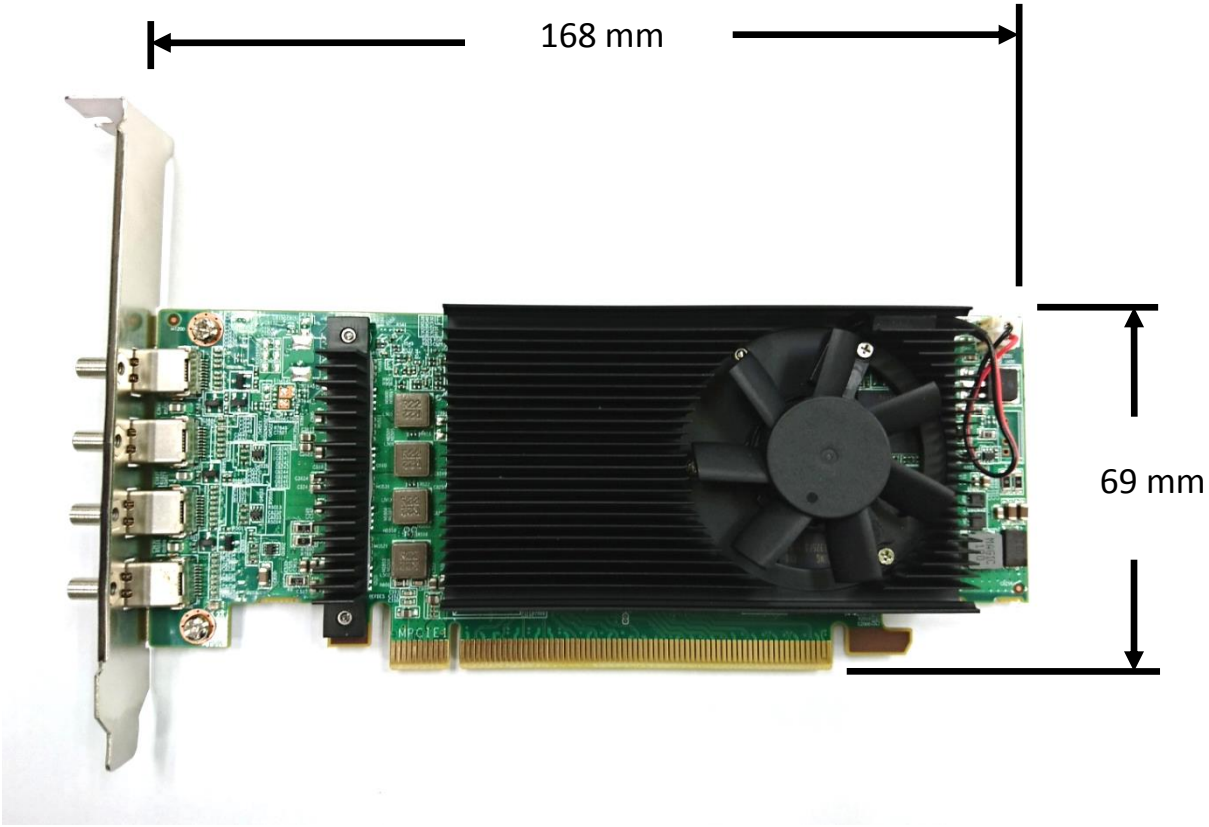
Pin	Side B Connector		Side A Connector	
#	**Name**	**Description**	**Name**	**Description**
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground
50	HSOp(8)	Transmitter Lane 8, Differential pair	RSVD	Reserved
51	HSOn(8)		GND	Ground
52	GND	Ground	HSIp(8)	Receiver Lane 8, Differential pair
53	GND	Ground	HSIn(8)	
54	HSOp(9)	Transmitter Lane 9, Differential pair	GND	Ground
55	HSOn(9)		GND	Ground
56	GND	Ground	HSIp(9)	Receiver Lane 9, Differential pair
57	GND	Ground	HSIn(9)	
58	HSOp(10)	Transmitter Lane 10, Differential pair	GND	Ground
59	HSOn(10)		GND	Ground
60	GND	Ground	HSIp(10)	Receiver Lane 10, Differential pair
61	GND	Ground	HSIn(10)	
62	HSOp(11)	Transmitter Lane 11,	GND	Ground

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
63	HSOn(11)	Differential pair	GND	Ground
64	GND	Ground	HSIp(11)	Receiver Lane 11, Differential pair
65	GND	Ground	HSIn(11)	
66	HSOp(12)	Transmitter Lane 12, Differential pair	GND	Ground
67	HSOn(12)		GND	Ground
68	GND	Ground	HSIp(12)	Receiver Lane 12, Differential pair
69	GND	Ground	HSIn(12)	
70	HSOp(13)	Transmitter Lane 13, Differential pair	GND	Ground
71	HSOn(13)		GND	Ground
72	GND	Ground	HSIp(13)	Receiver Lane 13, Differential pair
73	GND	Ground	HSIn(13)	
74	HSOp(14)	Transmitter Lane 14, Differential pair	GND	Ground
75	HSOn(14)		GND	Ground
76	GND	Ground	HSIp(14)	Receiver Lane 14, Differential pair
77	GND	Ground	HSIn(14)	
78	HSOp(15)	Transmitter Lane 15, Differential pair	GND	Ground
79	HSOn(15)		GND	Ground
80	GND	Ground	HSIp(15)	Receiver Lane 15, Differential pair
81	PRSNT#2	Hot plug present detect	HSIn(15)	
82	RSVD#2	Hot Plug Detect	GND	Ground

4. Board Configuration

4.1 Board Dimension

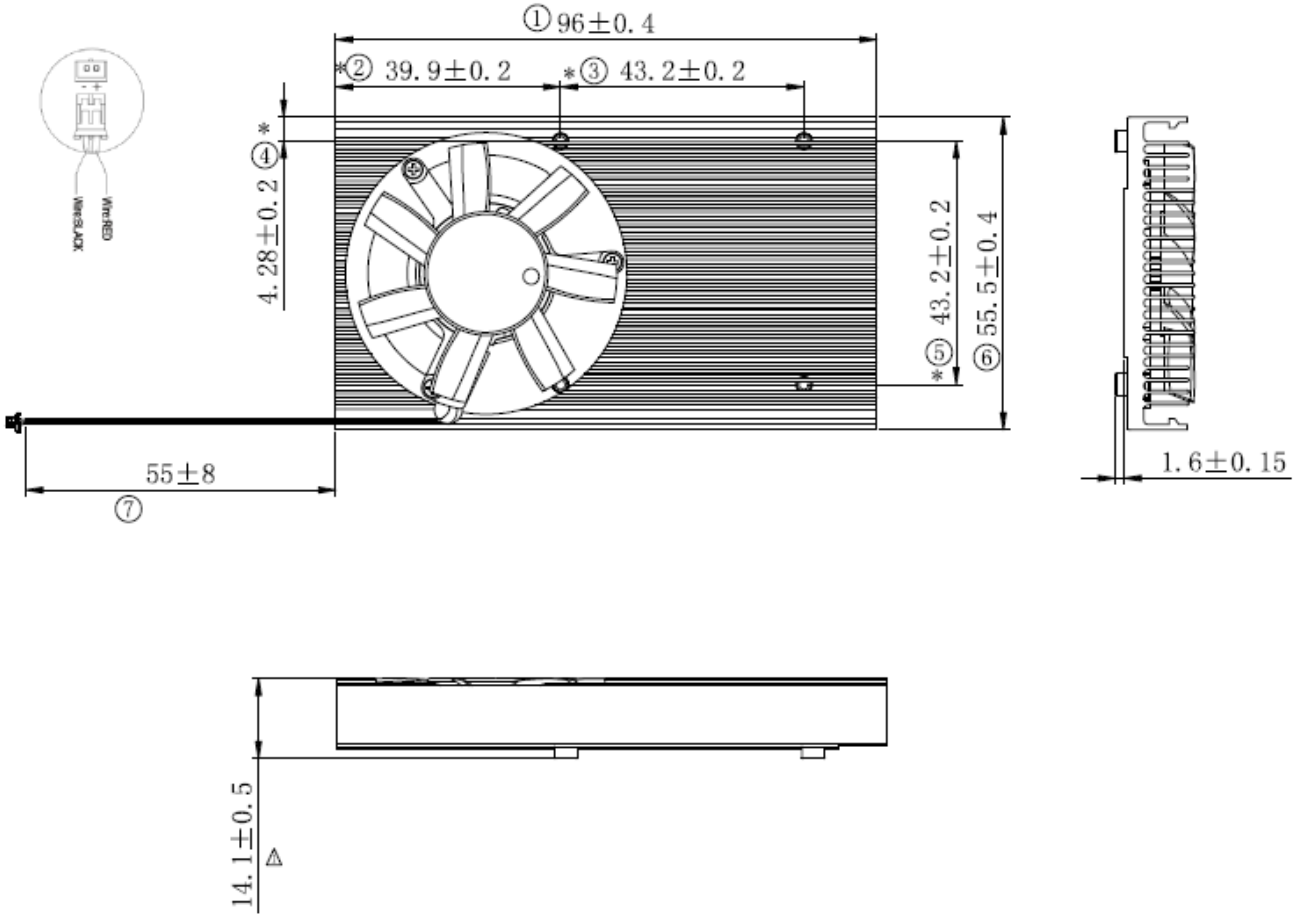


4.2 Display Interface

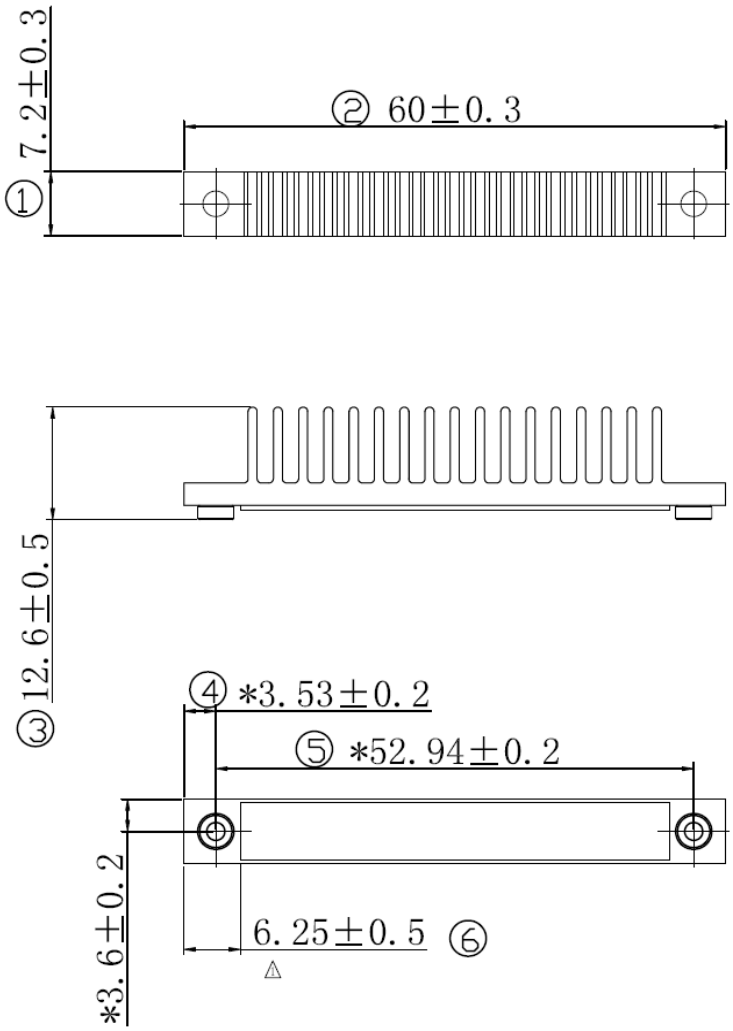
5. Thermal Mechanism

5.1 Fan Thermal Module

(Unit : mm)



5.2 MOSFET Thermal Sink



Change log list

Rev.	Data	History
1.0	2016/05/05	1st Draft.