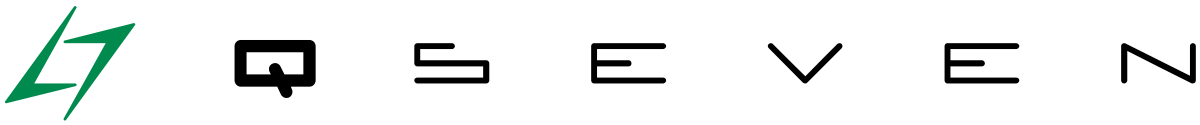


Qseven™ Design Guide

Guidelines for designing Qseven™ carrier boards.

Qseven™ Design Guide

Revision 0.8 (Release candidate)

Revision History

Revision	Date (dd.mm.yy)	Author	Revision History
0.1	02.02.09	Qseven™ Consortium	Initial Draft
0.2	16.02.09	Qseven™ Consortium	Updates throughout document.
0.3	19.02.09	Qseven™ Consortium	English proofreading.
0.4	26.06.09	Qseven™ Consortium	Added changes requested by the consortium members and updated schematics (SP30E90001_VC3)
0.5	09.07.09	Qseven™ Consortium	Added PCB footprint of Qseven™ module and MXM connector
0.6	04.08.09	Qseven™ Consortium	Added changes requested by the consortium members
0.7	21.08.09	Qseven™ Consortium	Created release candidate.
0.8	16.09.09	Qseven™ Consortium	Updated to current schematics (SP31E90001). Changed component height value for carrier board components located under Qseven™ module. Added Figure 2-1.

Preface

This document provides information for designing a custom system carrier board for Qseven™ modules. This document includes reference schematics for the external circuitry required to implement the various Qseven™ peripheral functions. It also explains how to extend the supported buses and how to add additional peripherals and expansion slots to a Qseven™ based system.

This design guide is not a specification. It contains additional detail information but does not replace the Qseven™ specification. It's strongly recommended to use the latest Qseven™ specification and the module vendor's product manuals as reference material.

Disclaimer

The information contained within this Qseven™ Design Guide, including but not limited to any product specification, is subject to change without notice.

The Qseven™ Consortium provides no warranty with regard to this Qseven™ Design Guide or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. The Qseven™ Consortium assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the Qseven™ interface specification. In no event shall the Qseven™ Consortium be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this Qseven™ interface specification or any other information contained herein or the use thereof.

The typical application circuits described in this document may not be suitable for all applications. In particular, additional components may need to be added to these circuits in order to meet specific ESD, EMC or safety isolation requirements. Such regulatory requirements and the techniques for meeting them vary by industry and are beyond the scope of this document.

Intended Audience

This Qseven™ Design Guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols may be used in this specification:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Qseven™ Design Guide 0.8 Release Candidate

Copyright Notice

Trademarks

Intel and Pentium are registered trademarks of Intel Corporation. ExpressCard is a registered trademark of Personal Computer Memory Card International Association (PCMCIA). PCI Express is a registered trademark of Peripheral Component Interconnect Special Interest Group (PCI-SIG). All product names and logos are property of their owners.

Lead-Free Designs (RoHS)

All Qseven™ designs shall be created from lead-free components in order to be RoHS compliant.

Qseven™ Logo usage

The Qseven™ logo is freely available for members of the Qseven™ consortium. The logo can only be applied to products that are fully compliant to the latest specification of the Qseven™ standard.

High resolution formats are available at the members area www.qseven-standard.org.

Electrostatic Sensitive Device

All electronic parts described in this design guide are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a carrier board or module except at an electrostatic-free workstation. Additionally, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging.

Key Words

- ***May*** - Indicates flexibility of choice with no implied recommendation or requirement.
- ***Shall*** - Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.
- ***Should*** - Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations but there is still a choice in implementation.

Qseven™ Concept

The Qseven™ concept is an off-the-shelf, multi vendor, Single-Board-Computer (SBC) that integrates all the core components of a typical PC and is mounted onto an application specific carrier board. Qseven™ modules have a standardized form factor of 70mm x 70mm and have specified pinouts based on the high speed MXM system connector which are standardized regardless of the vendor. The Qseven™ module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, audio, mass storage, network and multiple USB ports. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven™ module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a densely packed solution, which results in a more reliable product while simplifying system integration. Most importantly, Qseven™ applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class Qseven™ modules. Simply unplug one module and replace it with another, no redesign is necessary.

Qseven™ offers the newest I/O technologies on this minimum size form factor.

Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express. Next-generation high speed serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8 and x16 link.
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
MXM	Mobile PCI Express Module a standard for mobile modular graphics cards
GBE	Gigabit Ethernet
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial interface standard for hard disks.
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
HDA	High Definition Audio
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
SDIO	Secure Digital Input Output
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
SMB	System Management Bus
LVDS	Low-Voltage Differential Signaling
ACPI	Advanced Control Programmable Interface
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EC.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Schematics Naming Conventions

Term	Description
VCC12V	12 volt input power rail.
VCC5V	5 volt input power rail.
VCC3V3	3.3 volt input power rail.
VCC5V_A	5 volt input power rail during standby.
VCC3V3_A	3.3 volt input power rail during standby.
VCC3_RTC	+2.0V to +3.3V CMOS battery power
VCC1V5	1.5 volt auxiliary power rail.

Contents

Tables

Figures

1 Customer Feedback

The Qseven™ Design Guide has been created to help customers design Qseven™ compliant carrier boards. It should be used in conjunction with the Qseven™ Specification as well as any other relevant information with regards to the implementation of the interfaces mentioned within this document.

The guidelines set forth in this document have been carefully thought out by engineers of the Qseven™ consortium and are considered to be the most important factors when designing a Qseven™ carrier board. The Qseven™ consortium is committed to helping customers who are designing Qseven™ compliant carrier boards by sharing our expertise and providing the best possible support and documentation. Therefore, we welcome any suggestions our valued customers may have with regards to additional information that should be included in this Qseven™ Design Guide. Additionally, we encourage any feedback about the contents of this document with regards to clarity and understanding.

If you have any suggestions about additional content, or any questions about the existing content, please contact the Qseven™ consortium via email at info@qseven-standard.org

2 Qseven™ Specification Overview

2.1 Qseven™ Mechanical Characteristics

The Qseven™ module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

Edge-fingers on the module are referenced to the PCB slot center with an overall PCB thickness of 1.2mm ±0.1mm measured across the fingers including the plating and/or metalization on both sides. A bevel is optional but the edge shall be free of burrs and shall not have sharp edges.

The components located on the top side of the module are up to 5.5mm high. Components mounted on the backside of the Qseven™ module (in the space between the bottom surface of the module PCB and the top surface of the carrier board PCB) shall have a height of 2.5mm ±0.1 (dimension 'B' in Figure 2-1). When using a MXM connector with a resulting height between carrier board and Qseven™ module of 2.7mm, carrier board component placement below the Qseven™ module is prohibited.

Carrier board component placement below the Qseven™ module is only permitted when using a MXM connector with a resulting height between carrier board and Qseven™ module of 5.0mm (dimension 'A' in Figure 2-1) and no carrier board component shall exceed a height of 2.2mm ±0.1 (dimension 'C' in Figure 2-1). Using carrier board topside components up to 2.2mm allows a gap of 0.3mm between carrier board topside components and the Qseven™ module bottom side components. This may not be sufficient in some situations. In carrier board applications in which vibration or board flex is a concern, then the carrier board component height should be restricted to a value less than 2.2mm that yields a clearance that is sufficient for the application. Refer to Table 2-1 regarding MXM connector specifications.

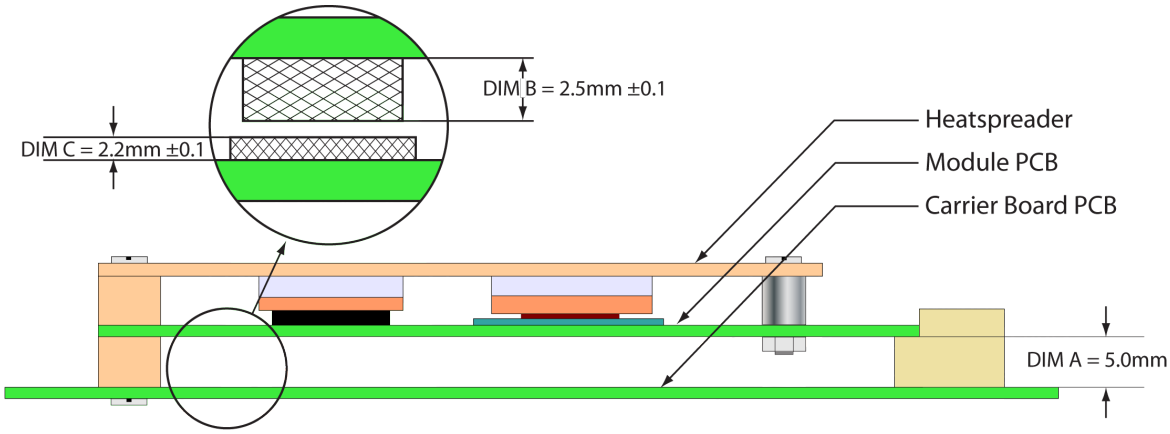


Figure 2-1 Bottom Side Qseven™ Module and Carrier Board Component Heights

The heatspreader offered for Qseven™ modules acts as a thermal coupling device and is not a heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heatspreader. The dissipation of heat will vary between different CPU boards. Refer to the Qseven™ module's user's guide for heatspreader dimensions and specifications.

The standoffs for the heatspreader and carrier board must not exceed 5.6mm overall external diameter. This ensures that the standoff contact area does not exceed the defined mounting hole footprint on the Qseven™ module. The screw that is to be used for mounting must be a metric thread M2.5 DIN7985 / ISO7045.

Qseven™ modules are defined to feature ultra low power CPU and chipset solutions with an ultra low “Thermal Design Power” (TDP). Furthermore, the modules power consumption should not exceed 12W.

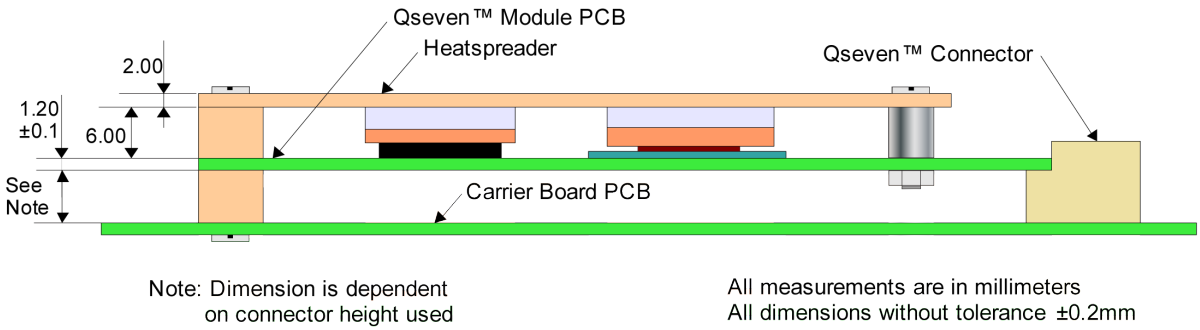
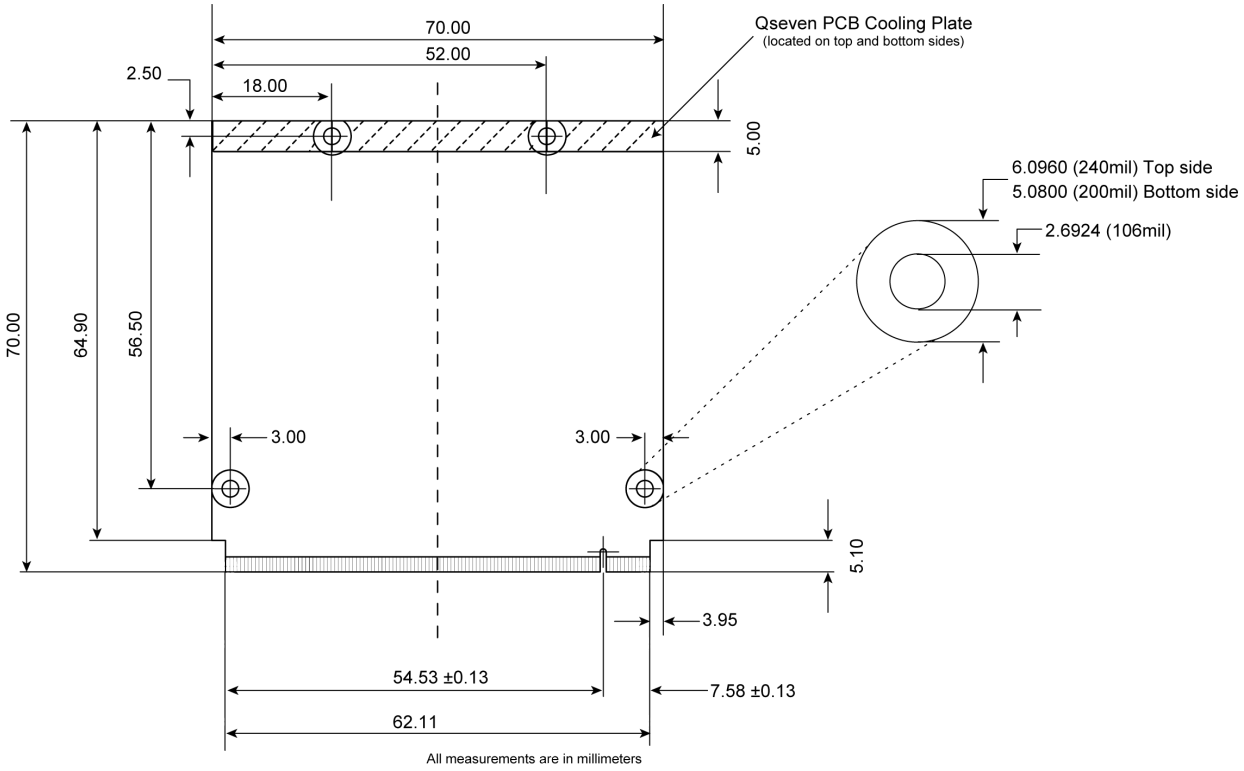


Figure 2-2 Overall Height including Heatspreader of the Qseven™ Module

2.2 Mechanical Dimensions

2.2.1 Qseven™ Module Outline

Figure 2-3 Mechanical Dimensions of the Qseven™ Module



Qseven Module Top Side

The Qseven™ PCB cooling plate shown in Figure 2-3 is to be used as a cooling interface between the Qseven™ module and the application specific cooling solution.

2.2.2 MXM Connector

The Qseven™ carrier board utilizes a 230-pin card-edge connector to connect the Qseven™ module. Originally, this card-edge connector was designed for MXM graphics modules that are used for PCI Express capable notebook graphics cards. The card-edge connector is following the MXM specification and therefore this connector type is also known as a MXM connector.

The MXM edge connector is the result of an extensive collaborative design effort with the industry's leading notebook manufacturers. This collaboration has produced a robust, low-cost edge connector that is capable of handling high-speed serialized signals.

The MXM connector accommodates various connector heights for different carrier board applications needs. This specification suggests two connector heights, 7.8mm and 5.5mm.

Table 2-1 MXM Connector

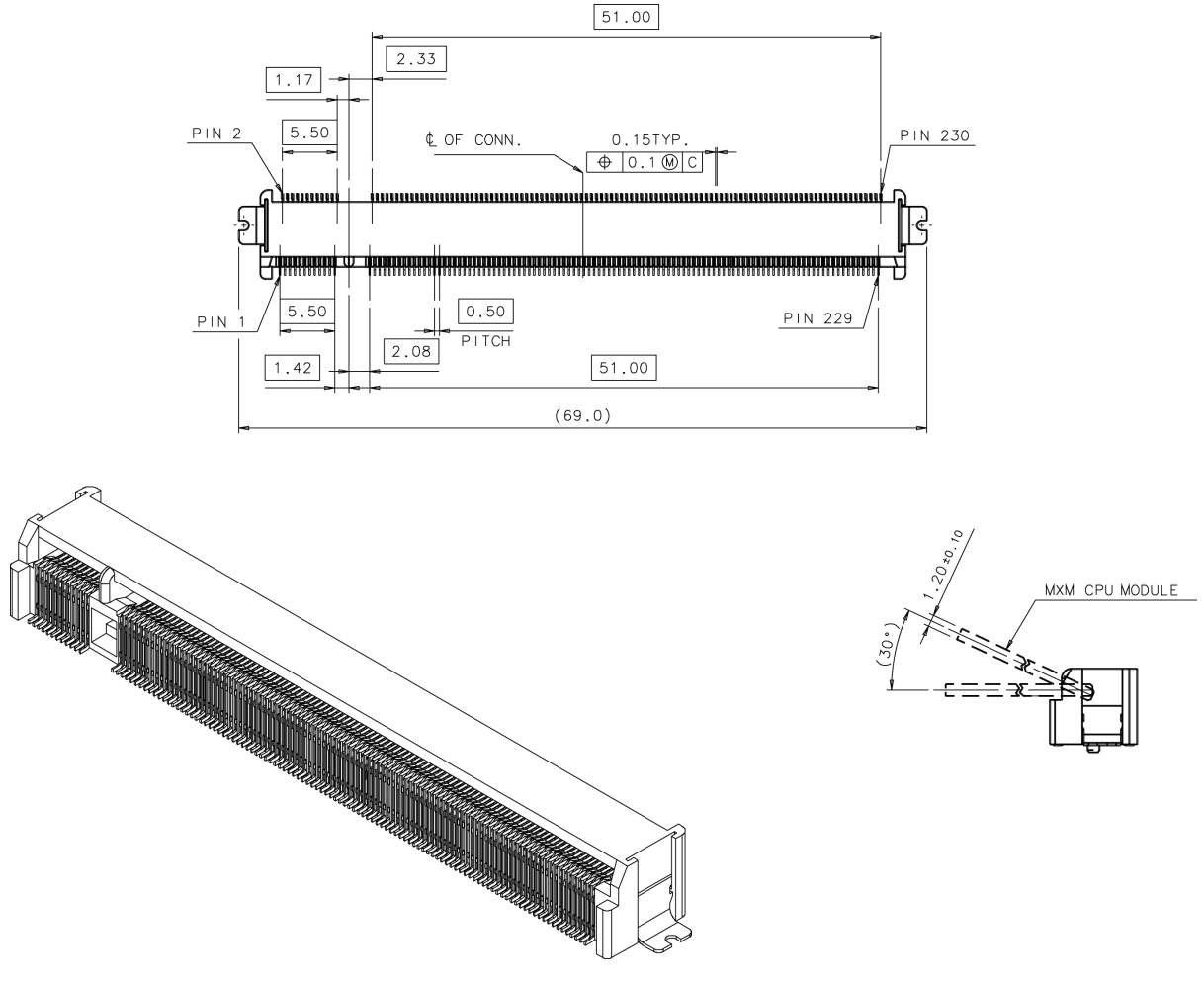
Manufacturer	Part Number	Specification	Resulting height between carrier board and Qseven™ module	Overall height of the MXM Connector
Foxconn	AS0B326-S78N-7F	AS0B326-S78N-7F	5.0mm	7.8mm
Foxconn	AS0B321-S78N-7F	AS0B321-S78N-7F	5.0mm	7.8mm
Foxconn	AS0B326-S55N-7F	AS0B326-S78N-7F	2.7mm	5.5mm
Speedtech	B33P102-XX1X	SPEC0378	5.0mm	7.5mm
Speedtech	B33P102-XX2X	SPEC0378	2.7mm	5.2mm
Lotes	Refer to manufacturer	SP-AAA-MXM-001	5.0mm	7.8mm
Lotes	Refer to manufacturer	SP-AAA-MXM-001	2.7mm	5.5mm

Note

The connectors mentioned in Table 2-1 are only a partial list of what is offered by the manufacturers. For more information about additional variants contact the manufacturer.

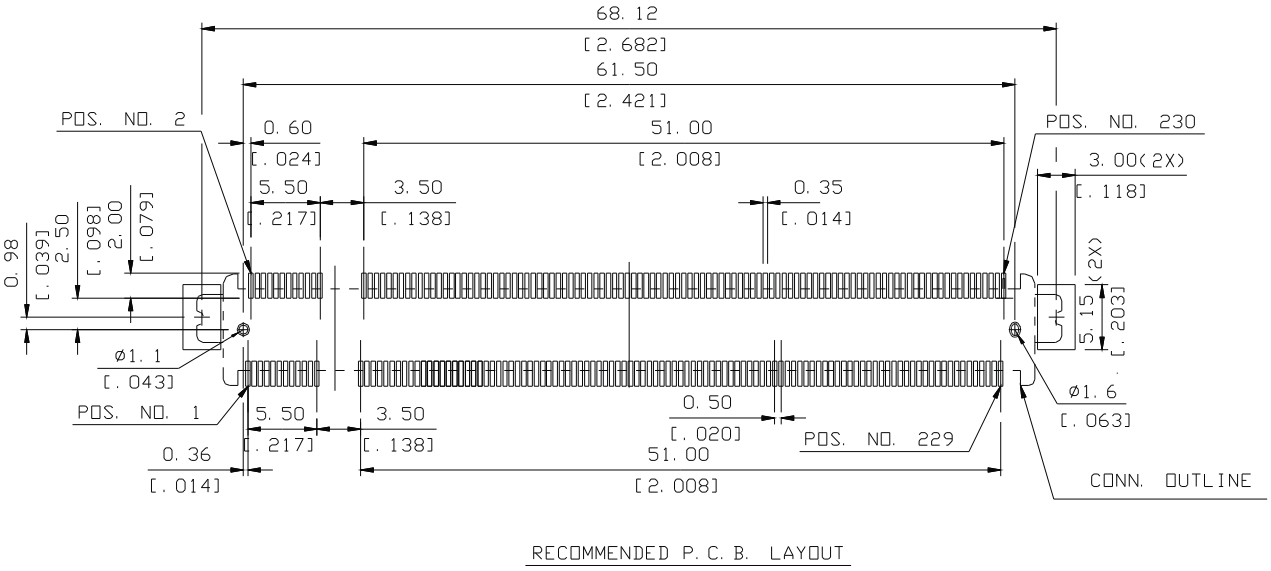
2.2.2.1 MXM Connector Dimensions

Figure 2-4 MXM Connector



2.2.2.2 MXM Connector Footprint

Figure 2-5 Carrier Board PCB Footprint for the MXM Connector



2.2.2.3 Qseven™ Module and MXM Connector PCB Footprint

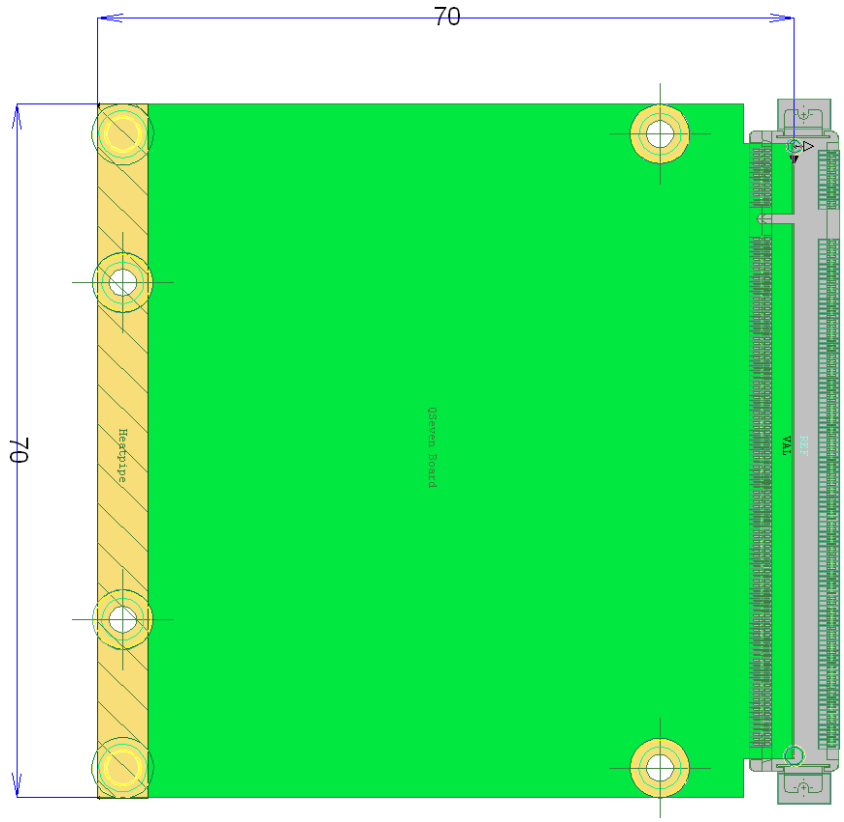


Figure 2-6 PCB footprint for the Qseven™ Module inserted in the MXM carrier board connector

3 Connector Pin Assignments

There are 115 edge fingers on the top and bottom side of the Qseven™ module that mate with the MXM connector. Table 3-1 lists the pin assignments for all 230 edge fingers.

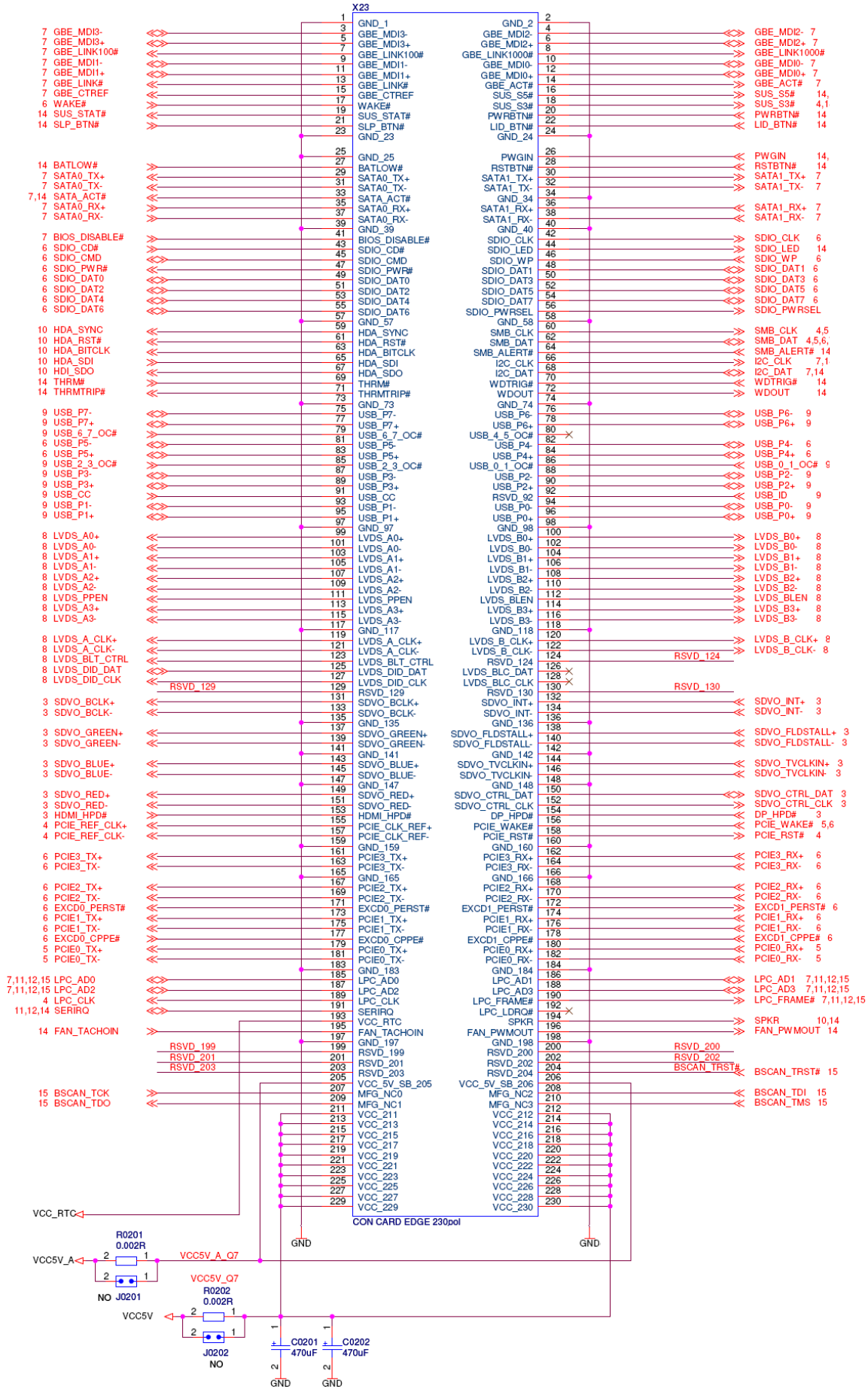
Table 3-1 Connector Pinout Description

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
	KEY		KEY
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	RSVD
57	GND	58	GND
59	HDA_SYNC	60	SMB_CLK
61	HDA_RST#	62	SMB_DAT
63	HDA_BITCLK	64	SMB_ALERT#
65	HDA_SDI	66	I2C_CLK
67	HDA_SDO	68	I2C_DAT
69	THRM#	70	WDTRIG#

Pin	Signal	Pin	Signal
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7-	76	USB_P6-
77	USB_P7+	78	USB_P6+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5-	82	USB_P4-
83	USB_P5+	84	USB_P4+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CC	92	USB_HC_SEL
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	LVDS_A0+	100	LVDS_B0+
101	LVDS_A0-	102	LVDS_B0-
103	LVDS_A1+	104	LVDS_B1+
105	LVDS_A1-	106	LVDS_B1-
107	LVDS_A2+	108	LVDS_B2+
109	LVDS_A2-	110	LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	LVDS_A3+	114	LVDS_B3+
115	LVDS_A3-	116	LVDS_B3-
117	GND	118	GND
119	LVDS_A_CLK+	120	LVDS_B_CLK+
121	LVDS_A_CLK-	122	LVDS_B_CLK-
123	LVDS_BLT_CTRL	124	RSVD
125	LVDS_DID_DAT	126	LVDS_BLC_DAT
127	LVDS_DID_CLK	128	LVDS_BLC_CLK
129	RSVD	130	RSVD
131	SDVO_BCLK+	132	SDVO_INT+
133	SDVO_BCLK-	134	SDVO_INT-
135	GND	136	GND
137	SDVO_GREEN+	138	SDVO_FLDSTALL+
139	SDVO_GREEN-	140	SDVO_FLDSTALL-
141	GND	142	GND
143	SDVO_BLUE+	144	SDVO_TVCLKIN+
145	SDVO_BLUE-	146	SDVO_TVCLKIN-
147	GND	148	GND
149	SDVO_RED+	150	SDVO_CTRL_DAT
151	SDVO_RED-	152	SDVO_CTRL_CLK
153	HDMI_HPD#	154	DP_HPD#

Pin	Signal	Pin	Signal
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	EXCD0_PERST#	172	EXCD1_PERST#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	EXCD0_CPPE#	178	EXCD1_CPPE#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR
195	FAN_TACHOIN	196	FAN_PWMOUT
197	GND	198	GND
199	RSVD	200	RSVD
201	RSVD	202	RSVD
203	RSVD	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

Figure 3-1 Qseven™ Connector Schematics


X23
GND_1
GND_2
GBE_MDI3-
GBE_MDI2-
GBE_MDI3+
GBE_MDI2+
GBE_LINK100#
GBE_LINK1000#
GBE_MDI1-
GBE_MDI0-
GBE_MDI1+
GBE_MDI0+
GBE_LINK#
GBE_ACT#
GBE_CTREF
SUS_S5#
WAKE#
SUS_S3#
SUS_STAT#
PWRBTN#
SLP_BTN#
LID_BTN#
GND_23
GND_24
GND_25
PWGIN
BATLOW#
RSTBTN#
SATA0_TX+
SATA1_TX+
SATA0_TX-
SATA1_TX-
SATA_ACT#
GND_34
SATA0_RX+
SATA1_RX+
SATA0_RX-
SATA1_RX-
GND_39
GND_40
BIOS_DISABLE#
SDIO_CLK
SDIO_CD#
SDIO_LED
SDIO_CMD
SDIO_WP
SDIO_PWR#
SDIO_DAT1
SDIO_DAT0
SDIO_DAT3
SDIO_DAT2
SDIO_DAT5
SDIO_DAT4
SDIO_DAT7
SDIO_DAT6
SDIO_PWRSEL
GND_57
GND_58
HDA_SYNC
SMB_CLK
HDA_RST#
SMB_DAT
HDA_BITCLK
SMB_ALERT#
HDA_SDI
I2C_CLK
HDA_SDO
I2C_DAT
THRM#
WDTRIG#
THRMTRIP#
WDOUT
GND_73
GND_74
USB_P7-
USB_P6-
USB_P7+
USB_P6+
USB_6_7_OC#
USB_4_5_OC#
USB_P5-
USB_P4-
USB_P5+
USB_P4+
USB_2_3_OC#
USB_0_1_OC#
USB_P3-
USB_P2-
USB_P3+
USB_P2+
USB_CC
RSVD_92
USB_P1-
USB_P0-
USB_P1+
USB_P0+
GND_97
GND_98
LVDS_A0+
LVDS_B0+
LVDS_A0-
LVDS_B0-
LVDS_A1+
LVDS_B1+
LVDS_A1-
LVDS_B1-
LVDS_A2+
LVDS_B2+
LVDS_A2-
LVDS_B2-
LVDS_PPEN
LVDS_BLEN
LVDS_A3+
LVDS_B3+
LVDS_A3-
LVDS_B3-
GND_117
GND_118
LVDS_A_CLK+
LVDS_B_CLK+
LVDS_A_CLK-
LVDS_B_CLK-
LVDS_BLT_CTRL
RSVD_124
LVDS_DID_DAT
LVDS_BLC_DAT
LVDS_DID_CLK
LVDS_BLC_CLK
RSVD_129
RSVD_130
SDVO_BCLK+
SDVO_INT+
SDVO_BCLK-
SDVO_INT-
GND_135
GND_136
SDVO_GREEN+
SDVO_FLDSTALL+
SDVO_GREEN-
SDVO_FLDSTALL-
GND_141
GND_142
SDVO_BLUE+
SDVO_TVCLKIN+
SDVO_BLUE-
SDVO_TVCLKIN-
GND_147
GND_148
SDVO_RED+
SDVO_CTRL_DAT
SDVO_RED-
SDVO_CTRL_CLK
HDMI_HPD#
DP_HPD#
PCIE_REF_CLK+
PCIE_CLK_REF+
PCIE_WAKE#
PCIE_REF_CLK-
PCIE_CLK_REF-
PCIE_RST#
GND_159
GND_160
PCIE3_TX+
PCIE3_RX+
PCIE3_TX-
PCIE3_RX-
GND_165
GND_166
PCIE2_TX+
PCIE2_RX+
PCIE2_TX-
PCIE2_RX-
EXCD0_PERST#
EXCD1_PERST#
PCIE1_TX+
PCIE1_RX+
PCIE1_TX-
PCIE1_RX-
EXCD0_CPPE#
EXCD1_CPPE#
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PCIE0_RX+
PCIE0_TX-
PCIE0_RX-
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GND_184
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_CLK
LPC_FRAME#
SERIRQ
LPC_LDRQ#
VCC_RTC
SPKR
FAN_TACHOIN
FAN_PWMOUT
GND_197
GND_198
RSVD_199
RSVD_200
RSVD_201
RSVD_202
RSVD_203
RSVD_204
VCC_5V_SB_205
VCC_5V_SB_206
MFG_NC0
MFG_NC2
MFG_NC1
MFG_NC3
VCC_211
VCC_212
VCC_213
VCC_214
VCC_215
VCC_216
VCC_217
VCC_218
VCC_219
VCC_220
VCC_221
VCC_222
VCC_223
VCC_224
VCC_225
VCC_226
VCC_227
VCC_228
VCC_229
VCC_230
CON CARD EDGE 230pol
GBE_MDI3- 7
GBE_MDI3+ 7
GBE_LINK100# 7
GBE_MDI1- 7
GBE_MDI1+ 7
GBE_LINK# 7
GBE_CTREF 7
WAKE# 6
SUS_STAT# 14
SLP_BTN# 14
BATLOW# 14
SATA0_TX+ 7
SATA0_TX- 7
SATA_ACT# 7,14
SATA0_RX+ 7
SATA0_RX- 7
BIOS_DISABLE# 7
SDIO_CD# 6
SDIO_CMD 6
SDIO_PWR# 6
SDIO_DAT0 6
SDIO_DAT2 6
SDIO_DAT4 6
SDIO_DAT6 6
HDA_SYNC 10
HDA_RST# 10
HDA_BITCLK 10
HDA_SDI 10
HDI_SDO 10
THRM# 14
THRMTRIP# 14
USB_P7- 9
USB_P7+ 9
USB_6_7_OC# 9
USB_P5- 6
USB_P5+ 6
USB_2_3_OC# 9
USB_P3- 9
USB_P3+ 9
USB_CC 9
USB_P1- 9
USB_P1+ 9
LVDS_A0+ 8
LVDS_A0- 8
LVDS_A1+ 8
LVDS_A1- 8
LVDS_A2+ 8
LVDS_A2- 8
LVDS_PPEN 8
LVDS_A3+ 8
LVDS_A3- 8
LVDS_A_CLK+ 8
LVDS_A_CLK- 8
LVDS_BLT_CTRL 8
LVDS_DID_DAT 8
LVDS_DID_CLK 8
RSVD_129
SDVO_BCLK+ 3
SDVO_BCLK- 3
SDVO_GREEN+ 3
SDVO_GREEN- 3
SDVO_BLUE+ 3
SDVO_BLUE- 3
SDVO_RED+ 3
SDVO_RED- 3
HDMI_HPD# 3
PCIE_REF_CLK+ 4
PCIE_REF_CLK- 4
PCIE3_TX+ 6
PCIE3_TX- 6
PCIE2_TX+ 6
PCIE2_TX- 6
EXCD0_PERST# 6
PCIE1_TX+ 6
PCIE1_TX- 6
EXCD0_CPPE# 6
PCIE0_TX+ 5
PCIE0_TX- 5
7,11,12,15 LPC_AD0
7,11,12,15 LPC_AD2
LPC_CLK 4
SERIRQ 11,12,14
FAN_TACHOIN 14
RSVD_199
RSVD_201
RSVD_203
BSCAN_TCK 15
BSCAN_TDO 15
GBE_MDI2- 7
GBE_MDI2+ 7
GBE_LINK1000# 7
GBE_MDI0- 7
GBE_MDI0+ 7
GBE_ACT# 7
SUS_S5# 14,
SUS_S3# 4,1
PWRBTN# 14
LID_BTN# 14
PWGIN 14,
RSTBTN# 14
SATA1_TX+ 7
SATA1_TX- 7
SATA1_RX+ 7
SATA1_RX- 7
SDIO_CLK 6
SDIO_LED 14
SDIO_WP 6
SDIO_DAT1 6
SDIO_DAT3 6
SDIO_DAT5 6
SDIO_DAT7 6
SDIO_PWRSEL
SMB_CLK 4,5
SMB_DAT 4,5,6,
SMB_ALERT# 14
I2C_CLK 7,1
I2C_DAT 7,14
WDTRIG# 14
WDOUT 14
USB_P6- 9
USB_P6+ 9
USB_P4- 6
USB_P4+ 6
USB_0_1_OC# 9
USB_P2- 9
USB_P2+ 9
USB_ID 9
USB_P0- 9
USB_P0+ 9
LVDS_B0+ 8
LVDS_B0- 8
LVDS_B1+ 8
LVDS_B1- 8
LVDS_B2+ 8
LVDS_B2- 8
LVDS_BLEN 8
LVDS_B3+ 8
LVDS_B3- 8
LVDS_B_CLK+ 8
LVDS_B_CLK- 8
RSVD_124
RSVD_130
SDVO_INT+ 3
SDVO_INT- 3
SDVO_FLDSTALL+ 3
SDVO_FLDSTALL- 3
SDVO_TVCLKIN+ 3
SDVO_TVCLKIN- 3
SDVO_CTRL_DAT 3
SDVO_CTRL_CLK 3
DP_HPD# 3
PCIE_WAKE# 5,6
PCIE_RST# 4
PCIE3_RX+ 6
PCIE3_RX- 6
PCIE2_RX+ 6
PCIE2_RX- 6
EXCD1_PERST# 6
PCIE1_RX+ 6
PCIE1_RX- 6
EXCD1_CPPE# 6
PCIE0_RX+ 5
PCIE0_RX- 5
LPC_AD1 7,11,12,15
LPC_AD3 7,11,12,15
LPC_FRAME# 7,11,12,15
SPKR 10,14
FAN_PWMOUT 14
RSVD_200
RSVD_202
BSCAN_TRST# 15
BSCAN_TDI 15
BSCAN_TMS 15
VCC_RTC
GND
GND
R0201
0.002R
VCC5V_A
VCC5V_A_Q7
NO J0201
VCC5V_Q7
R0202
0.002R
VCC5V
J0202
NO
C0201
470uF
C0202
470uF
GND
GND

3.1 Signal Descriptions

The following section describes the signals on Qseven™ MXM connector that are provided over the edge-fingers of the Qseven™ module. Refer to the Qseven™ Specification for information about this.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Differential pairs are indicated by trailing '+' and '-' signs for the positive or negative signal. All required pull-ups or pull-down resistors shall be implemented on the Qseven™ module. This ensures that none of the signals that are not used will be left floating.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Table 3-2 Signal Tables Terminology Descriptions

Term	Description
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Bi-directional 3.3V tolerant active during suspend and running state.
I_{OL}	Output low current. The I_{OL} is the maximum output low current the module must be able to drive to an external circuitry.
I_{IL}	Input low current. The I_{IL} is the maximum input low current that must be provided to the Qseven module via external circuitry in order to guarantee a proper logic low level of the signal.
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
OC	Open collector
P	Power input/output
PP	Push Pull
PDS	Pull-down strap
REF	Reference voltage output. May be sourced from a module power plane.
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
USB	In compliance with the Universal Serial Bus Specification, Revision 2.0
GBE	In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet
SATA	In compliance with Serial ATA specification, Revision 1.0a
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

3.2 PCI Express Interface Signals

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. A PCI Express lane consists of dual simplex channels, each implemented as a low-voltage differentially driven transmit pair and receive pair. They are used for simultaneous transmission in each direction. The bandwidth of a PCI Express link can be scaled by adding signal pairs to form multiple lanes between two devices. The Qseven™ module provides configurations with x1 and x4 link widths. Each single lane has a raw data transfer rate of 2.5Gbps @ 1.25GHz.

The PCI Express interface of the Qseven™ module consists of minimum 2 and up to 4 lanes, each with a receive and transmit differential signal pair designated from PCIE0_RX (+ and -) to PCIE3_RX (+ and -) and correspondingly from PCIE0_TX (+ and -) to PCIE3_TX (+ and -). According to the PCI Express specification, these four lanes can be configured as several PCI Express x1 links or to a combined x4 link. These configuration possibilities are based on the Qseven™ module's chipset capabilities. Refer to the vendor specific Qseven™ module documentation for the module that you are using for additional information about this subject.

Table 3-3 Signal Definition PCI Express

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IIL}	I/O
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	PCIE		I
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	PCIE		O
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	PCIE		I
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	PCIE		O
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	PCIE		I
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	PCIE		O
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	PCIE		I
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	PCIE		O
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	PCIE		O
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	CMOS 3.3V Suspend	≥ 5 mA	I
PCIE_RST#	158	Reset Signal for external devices.	CMOS 3.3V	max 1 mA	O

Note

There are a maximum of 4 PCI Express TX and RX differential pairs supported on the Qseven™ module standard. Depending on the features supported by the Qseven™ module and the core logic chipset used, these lines may be used to form x1 or x4 PCI Express links. The documentation for the Qseven™ module shall clearly identify, which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

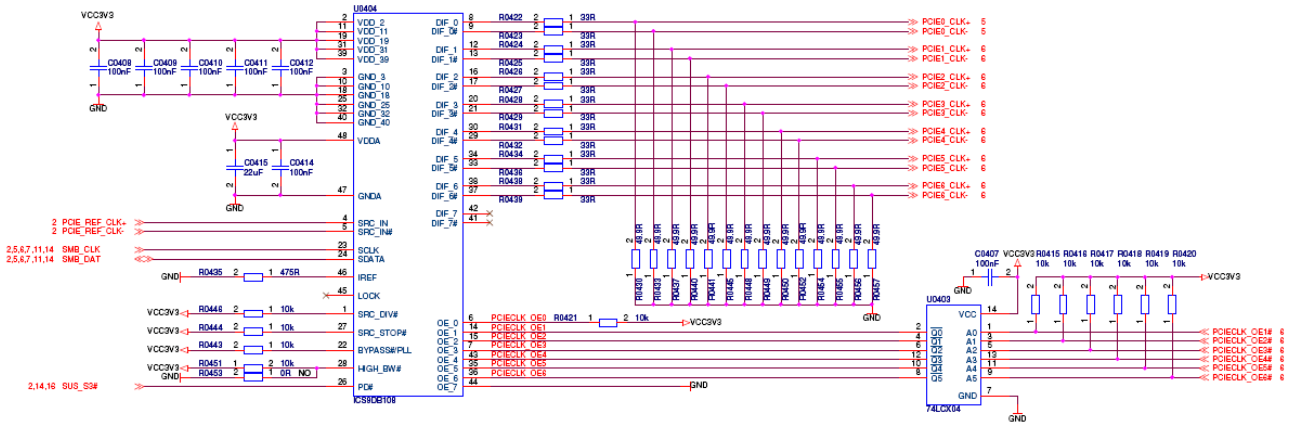
3.3 PCI Express Implementation Guidelines

3.3.1 PCI Express Reference Clock

PCI Express does not specify the external clock source for PCI Express devices. It only provides a 100MHz differential Serial Reference Clock (SRC), which can be used by the internal PLL of the PCI Express device to generate the required 1.25GHz clock. The corresponding Serial Reference Clock signals *'PCI_CLK_REF+'* and *'PCI_CLK_REF-'* can be found on the Qseven™ module connector on pins 155 and 157. In an application where more than one PCI Express slot or device is needed, the differential Serial Reference Clock signal must be replicated by using a zero-delay buffer. Figure 3-1 shows an example implementing the ICS9DB108 PCI Express zero-delay buffer from Integrated Circuit Systems (ICS) (http://www.idt.com). This zero-delay buffer provides eight Serial Reference Clock outputs including clock request functionality. This circuit is also used on the Qseven™ evaluation carrier board.

The PCI Express architecture has specified the clock signal to be embedded in the serial data stream for synchronization of the two devices. For carrier board designs that implement PCI Express connectors for external add-in card devices, the SRC is required on the connector interface. External add-in cards may utilize this SRC differential signal pair to reduce jitter for maintaining maximum data transfer rate. For detailed information about this subject refer to chapter 2.1 of the 'PCI Express™ Card Electromechanical Specification Revision 1.1'.

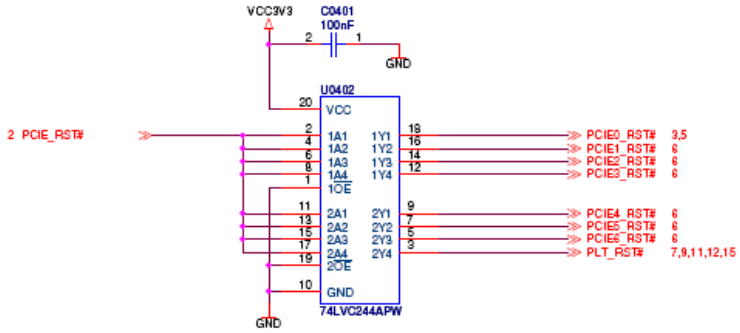
Figure 3-2 PCI Express Clock Buffer Example



3.3.2 PCI Express Reset

The Qseven™ module provides one PCI Express Reset signal on pin 158 of the Qseven™ connector. It is recommended to use a buffer to replicate the Reset signal on the carrier board when more than one PCI Express slot or device is needed. Figure 3-3 shows an implementation example.

Figure 3-3 PCI Express Reset Buffer Example



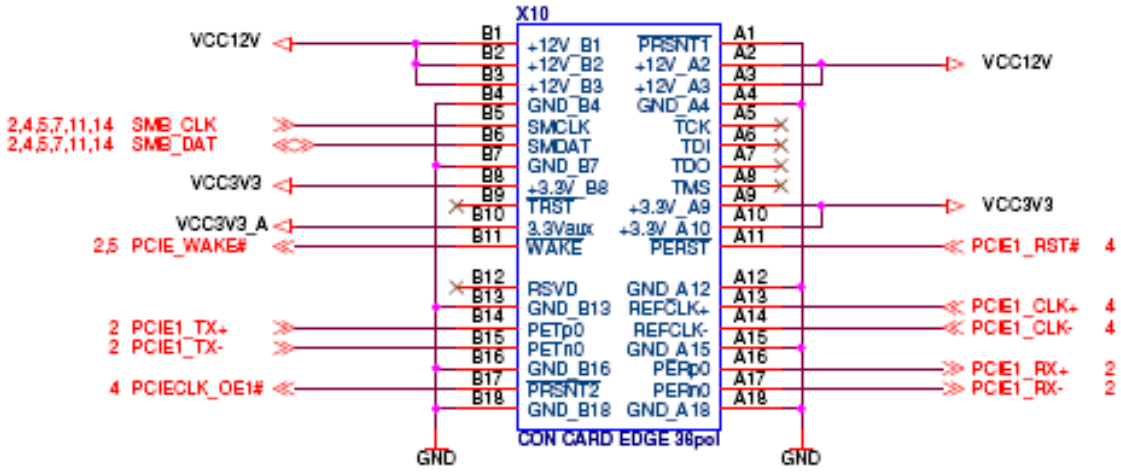
3.3.3 PCI Express Lane Configurations

The lane configuration possibilities of the PCI Express interface of a Qseven™ module is dependent on the module's chipset. If an application requires a x4 PCI Express link, it may be necessary to implement a hardware strap on the carrier board in order to tell the module's chipset to switch the PCI Express lanes 0-3 from x1 to x4 mode. The configuration possibilities and implementation requirements may differ depending on the module's chipset. Refer to the Qseven™ module's user's guide for additional information about this subject.

3.3.4 PCI Express x1 and x4 Connectors

Figure 3-4 illustrates the pinout definition for the standard x1 PCI Express connector. The same solution has been implemented on the Qseven™ evaluation carrier board. It utilizes PCI Express lane 1.

Figure 3-4 PCI Express x1 Connector



Signal fields in Table 3-4 that do not have any light grey shading describe the pinout for the PCI Express x1 slot (1 PCI Express Lane) and the signal fields marked with light grey indicate the additional signals needed on a PCI Express x4 connector (4 PCI Express Lanes).

Table 3-4 PCI Express x1 and x4 Connector Pinout and Signal Descriptions

Pin	Signal	Description	Pin	Signal	Description
1B	+12V	12V power	1A	PRSNT1#*	Hot-Plug presence detected
2B	+12V	12V power	2A	+12V	12V power
3B	+12V	12V power	3A	+12V	12V power
4B	GND	Ground	4A	GND	Ground
5B	SMB_CLK*	SMBus Clock	5A	JTAG2*	TCK - Boundary Scan Test Clock
6B	SMB_DAT*	SMBus Data	6A	JTAG3*	TDI – Boundary Scan Test Data Input
7B	GND	Ground	7A	JTAG4*	TDO - Boundary Scan Test Data Output
8B	+3.3V	3.3V power	8A	JTAG5*	TMS - Boundary Scan Test Mode Select
9B	JTAG1*	TRST# - Boundary Scan Test Reset	9A	+3.3V	3.3V power
10B	+3.3Vaux*	3.3V auxiliary power	10A	+3.3V	3.3V power
11B	PCIE_WAKE#*	Link Reactivation	11A	PCIE_RST#*	Reset
		Mechanical Key			
12B	RSVD	Reserved	12A	GND	Ground
13B	GND	Ground	13A	PCIE_CLK_REF+*	Reference Clock differential pair positive signal
14B	PCIE0_TX+	Transmitter differential pair positive signal, Lane 0	14A	PCIE_CLK_REF-*	Reference Clock differential pair negative signal
15B	PCIE0_TX-	Transmitter differential pair negative signal, Lane 0	15A	GND	Ground
16B	GND	Ground	16A	PCIE0_RX+	Receiver differential pair positive signal, Lane 0
17B	PRSNT2#*	Hot-Plug presence detected	17A	PCIE0_RX-	Receiver differential pair negative

Pin	Signal	Description	Pin	Signal	Description
					signal, Lane 0
18B	GND	Ground	18A	GND	Ground
19B	PCIE1_TX+	Transmitter differential pair positive signal, Lane 1	19A	RSVD	Reserved
20B	PCIE1_TX-	Transmitter differential pair negative signal, Lane 1	20A	GND	Ground
21B	GND	Ground	21A	PCIE1_RX+	Receiver differential pair positive signal, Lane 1
22B	GND	Ground	22A	PCIE1_RX-	Receiver differential pair negative signal, Lane 1
23B	PCIE2_TX+	Transmitter differential pair positive signal, Lane 2	23A	GND	Ground
24B	PCIE2_TX-	Transmitter differential pair negative signal, Lane 2	24A	GND	Ground
25B	GND	Ground	25A	PCIE2_RX+	Receiver differential pair positive signal, Lane 2
26B	GND	Ground	26A	PCIE2_RX-	Receiver differential pair negative signal, Lane 2
27B	PCIE3_TX+	Transmitter differential pair positive signal, Lane 3	27A	GND	Ground
28B	PCIE3_TX-	Transmitter differential pair negative signal, Lane 3	28A	GND	Ground
29B	GND	Ground	29A	PCIE3_RX+	Receiver differential pair positive signal, Lane 3
30B	GND	Ground	30A	PCIE3_RX-	Receiver differential pair negative signal, Lane 3
31B	PRSTN2#*	Hot-Plug presence detected	31A	GND	Ground
32B	GND	Ground	32A	RSVD	Reserved

Note

** Auxiliary signals. These signals are not required by the PCI Express Architecture.*

3.3.5 PCI Express Power Requirements

To utilize the full functionality of PCI Express devices on the Qseven™ carrier board, some additional supply voltages are necessary beside the standard supply voltages of the ATX power supply. Many PCI Express devices are capable of generating wake up events during standby operation, for example an external PCI Express Ethernet device that supports 'Wake On LAN' functionality. Therefore, it is necessary to generate an additional 3.3V standby voltage on the carrier board to supply such devices during standby operation. The voltage regulator must be designed to meet the power requirements of the connected devices.

Note

Refer to the reference schematics of the Qseven™ evaluation carrier board for an example of how to implement a 3.3V standby voltage regulator.

When an external ExpressCard or PCI Express Mini Card device must be implemented on the carrier board, an additional 1.5V supply voltage is required by the appropriate card sockets. The voltage regulator must be designed to meet the power requirements of the connected devices.

Note

Refer to the reference schematics of the Qseven™ evaluation carrier board for an example of how to implement a 1.5V voltage regulator.

The PCI Express specification defines maximum power requirements for the different PCI Express connectors and/or devices. The power supply for the carrier board must be designed to meet these maximum power requirements. Table 3-5 shows the maximum current consumption defined for the different types of PCI Express connectors.

Table 3-5 PCI Express Connector Power Requirements

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk		
3.3V	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk	1.35A	1.0A
3.3V Standby (optional)	375mA @ 150uF bulk	375mA @ 150uF bulk	275mA	330mA
1.5V			750mA	500mA

Implementing PCI Express connectors on the carrier board requires distinctive decoupling of the connector supply voltages to reduce possible voltage drops and to provide an AC return path in a manner consistent with high-speed signaling techniques. Decoupling capacitors should be placed as close as possible to the power pins of the connectors. Table 3-6 shows the minimum requirements for power decoupling of the different power pin types of each PCI Express connector type.

Table 3-6 PCIe Power Decoupling Requirements

Power Pin Type	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
12V	1x 22µF, 2x 100nF	4x 22uF, 2x 100nF		
3.3V	1x 22uF, 2x 100nF	1x 100uF, 2x 100nF		
3.3V Standby (optional)	1x 22uF, 1x 100nF	1x 22uF, 1x 100nF		
1.5V				

3.3.6 PCI Express Mini Card

The PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms equipped with communication applications such as Wireless LAN. A small footprint connector can be implemented on the carrier board providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradeable, standardized PCI Express Mini Card device to the carrier board without the additional expenditure of a redesign.

In addition to a PCI Express x1 link and a USB 2.0 link, the PCI Express Mini Card interface utilizes the following control and reset signals, which are provided by the Qseven™ module.

Table 3-7 PCI Express Mini Card Control Signal Descriptions

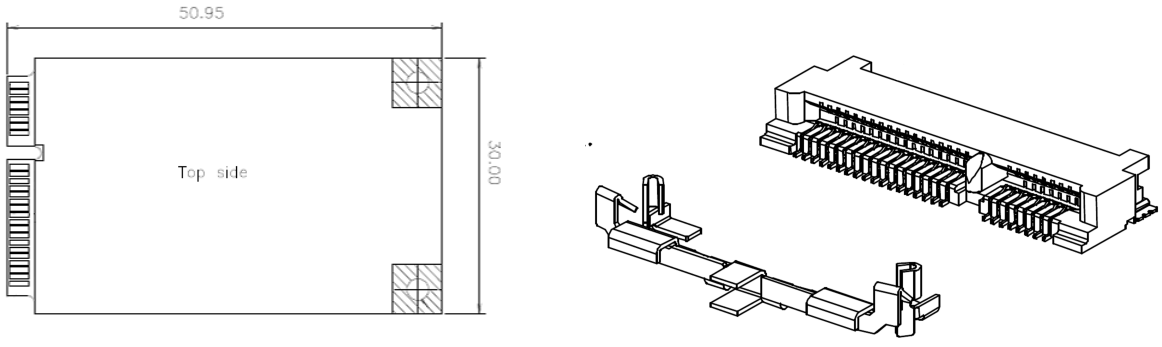
Signal	Pin	Description	I/O	Comment
EXCD0_PERST#	171	PCIe Mini Card Reset, Slot 1	O 3.3V CMOS	
EXCD1_PERST#	172	PCIe Mini Card Reset, Slot 2	O 3.3V CMOS	
SMB_CLK	60	System Management Bus Clock Signal	I/O 3.3V OD CMOS	
SMB_DAT	62	System Management Bus Data Signal	I/O 3.3V OD CMOS	

The reference circuit for PCI Express Mini Card adaptation displayed in Figure 3-6 uses the following signals that are generated on the Qseven™ evaluation carrier board.

Signal	Description	I/O	
PCIE_RST#_5	PCI Express Bus Reset	I 3.3V Standby CMOS	This signal originates from the PCI Express reset buffer shown in Figure 3-3 'PCI Express Reset Buffer Circuitry'
PCIECLK_OE5#	Request for PCI Express Serial Reference Clock. For more details see section 'PCI Express Reference Clock' for details.	I 3.3V CMOS	This signal originates from the clock buffer shown in Figure 3-2 'PCI Express Clock Buffer Circuitry'.

3.3.6.1 PCI Express Mini Card Socket

Figure 3-5 PCI Express Mini Card and Socket



A potential source for this PCI Express Mini Card carrier board connector is: AMP/Tyco HARD TRAY ASSY MINI PCI EXPRESS CONNECTOR 52 POS Article No. 1717831-1.

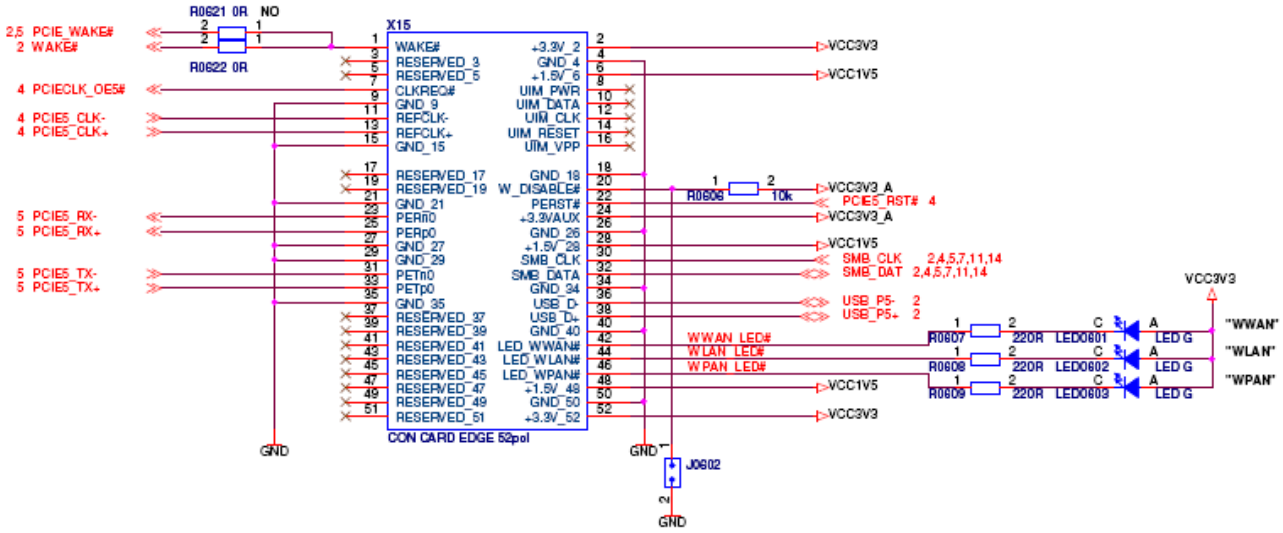
Table 3-8 PCI Express Mini Card Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	WAKE#	Request that the host interface return to full operation and respond to PCIe.	2	+3.3V	Primary voltage source, 3.3V.
3	RSVD	Reserved	4	GND	Ground
5	RSVD	Reserved	6	+1.5V	Secondary voltage source, 1.5V.
7	CLKREQ#	Reference clock request signal.	8	UIM_PWR	Power source for User Identity Modules (UIM).
9	GND	Ground	10	UIM_DATA	Data signal for UIM.
11	REFCLK-	Reference Clock differential pair negative signal.	12	UIM_CLK	Clock signal for UIM.
13	REFCLK+	Reference Clock differential pair positive signal.	14	UIM_RESET	Reset signal for UIM.
15	GND	Ground	16	UIM_VPP	Variable supply voltage for UIM.
Mechanical Key					
17	RSVD	Reserved for future second User Identity Modules interface (UIM_C8).	18	GND	Ground
19	RSVD	Reserved for future second User Identity Module interface (UIM_C4).	20	W_DISABLE	Used by the system to disable radio operation on add-in cards that implement radio frequency application.
21	GND	Ground	22	PERST#	PCI Express Reset
23	PCIEx_RX-	Receiver differential pair negative signal, Lane x.	24	3.3Vaux	Auxiliary voltage source, 3.3V.
25	PCIEx_RX+	Receiver differential pair positive signal, Lane x.	26	GND	Ground
27	GND	Ground	28	+1.5V	Secondary voltage source, 1.5V.
29	GND	Ground	30	SMB_CLK	System Management Bus Clock.
31	PCIEx_TX-	Transmitter differential pair negative signal, Lane x.	32	SMB_DATA	System Management Bus Data.
33	PCIEx_TX+	Transmitter differential pair positive Signal, Lane x.	34	GND	Ground
35	GND	Ground	36	USB_D-	USB Serial Data Interface differential pair, negative signal.
37	RSVD	Reserved for future second PCIe lane.	38	USB_D+	USB Serial Data Interface differential pair, positive signal.
39	RSVD	Reserved for future second PCIe lane.	40	GND	Ground
41	RSVD	Reserved for future second PCIe lane.	42	LED_WWAN#	LED status indicator signals provided by the system.
43	RSVD	Reserved for future second PCIe lane.	44	LED_WLAN#	LED status indicator signals provided by the system.
45	RSVD	Reserved for future second PCIe lane.	46	LED_WPAN#	LED status indicator signals provided by the system.
47	RSVD	Reserved for future second PCIe lane.	48	+1.5V	Secondary voltage source, 1.5V.
49	RSVD	Reserved for future second PCIe lane.	50	GND	Ground
51	RSVD	Reserved for future second PCIe lane.	52	+3.3V	Primary voltage source, 3.3V.

3.3.6.2 PCI Express Mini Card Reference Schematics

Figure 3-6 displays an example of how a PCI Express Mini Card socket can be connected to a Qseven™ carrier board. The same solution has been implemented on the Qseven™ evaluation carrier board. It utilizes USB Port 5 and PCI Express lane 5.

Figure 3-6 PCI Express Mini Card Reference Circuitry

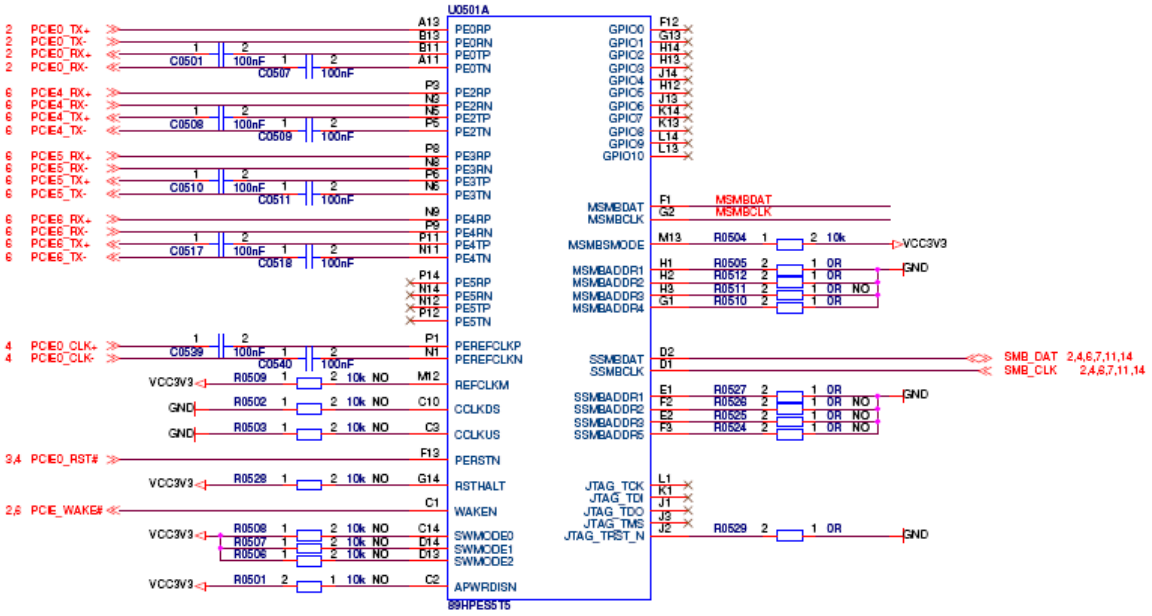


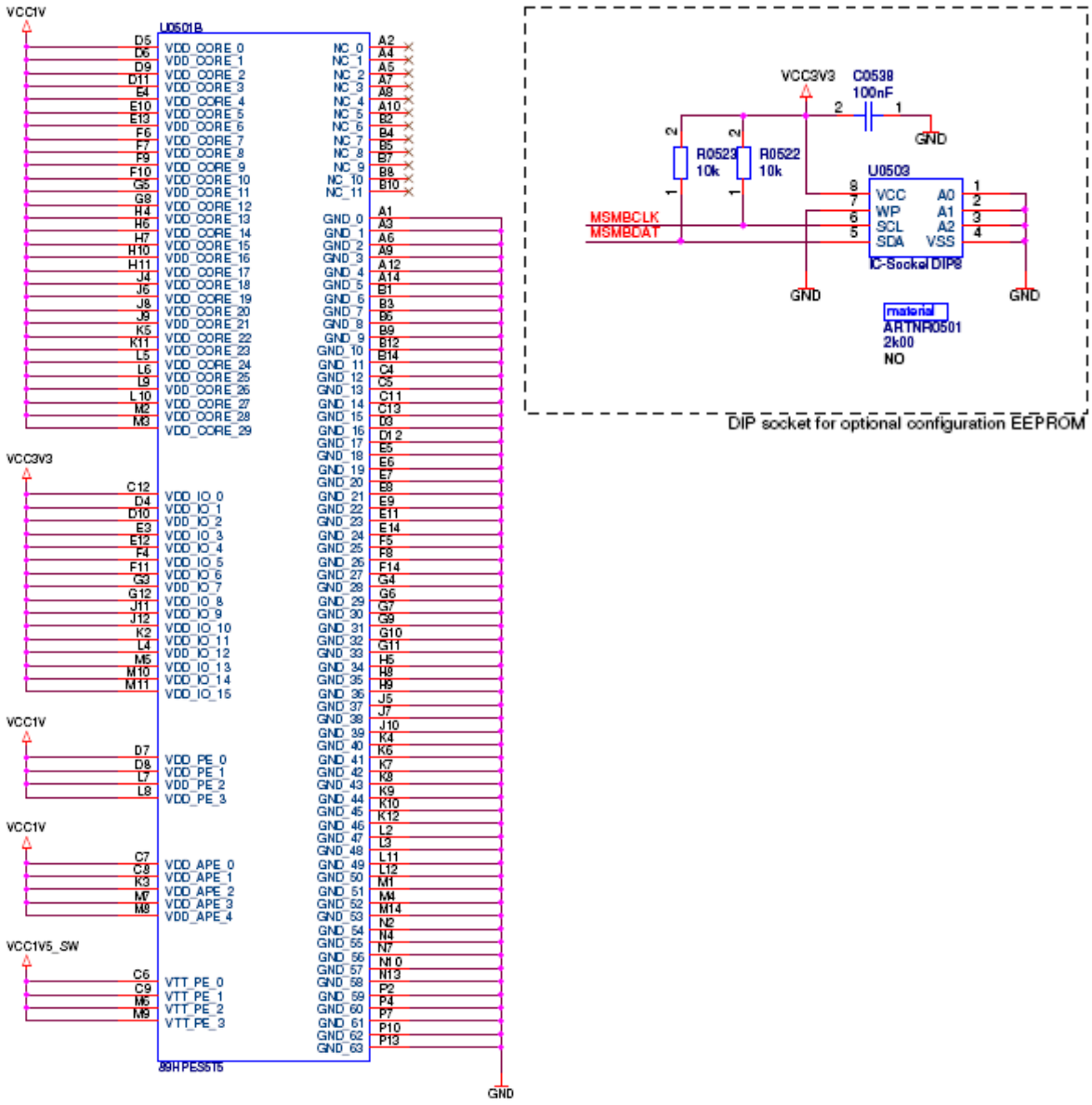
3.3.7 PCI Express Switch

In applications where additional PCI Express lanes other than those provided by the Qseven™ module are needed, a PCI Express Switch on the Qseven™ carrier board can be used to expand the number of available PCI Express lanes.

The example implemented on the Qseven™ evaluation carrier board uses the 5th Lane and a 5 Port PCI Express Switch 89HPES5T5 from IDT (http://www.idt.com). The reference schematics of the Qseven™ evaluation carrier board are shown in Figure 3-7.

Figure 3-7 PCI Express Switch Example





3.3.8 Routing Considerations for PCI Express

See section 4 of this document for trace routing guidelines and the Qseven™ specification for more information about this subject.

3.4 ExpressCard

Qseven™ modules offer optional support for two ExpressCard slots. ExpressCard is the successor to PCMCIA and PC Cards. ExpressCard takes advantage of the scalable, high-bandwidth serial PCI Express and USB 2.0 interfaces.

In addition to the signals for PCI Express x1 link and USB 2.0 link, the ExpressCard interface requires the following control signals provided by the Qseven™ module.

Table 3-9 Signal Definition ExpressCard

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
EXCD0_CPPE#	177	ExpressCard slot #0 capable card request.	CMOS 3.3V	≥ 5 mA	I
EXCD0_PERST#	171	ExpressCard slot #0 reset.	CMOS 3.3V	max. 1 mA	O
EXCD1_CPPE#	178	ExpressCard slot #1 capable card request.	CMOS 3.3V	≥ 5 mA	I
EXCD1_PERST#	172	ExpressCard slot #1 reset.	CMOS 3.3V	max. 1 mA	O

Figure 3-8 displays an example of how an ExpressCard slot can be connected to a Qseven™ embedded module. Power management for the ExpressCard slot is handled by a Texas Instruments TPS2231 Power Interface Switch (*http://www.ti.com*). This solution has been implemented on the Qseven™ evaluation carrier board. It uses PCI Express lane 6 and USB port 4.

Figure 3-8 ExpressCard Reference Circuitry

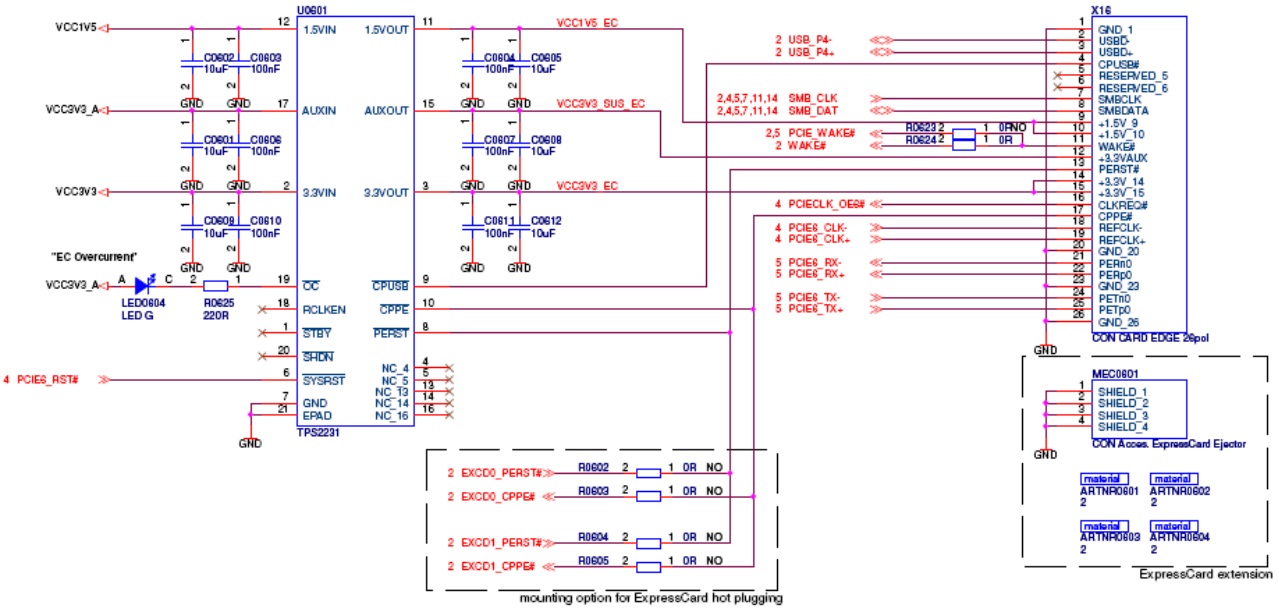


Table 3-10 ExpressCard Pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	14	+3.3V_14	Primary voltage source, 3.3V
2	USBD-	USB Serial Data Interface differential pair, negative signal	15	+3.3V_15	Primary voltage source, 3.3V
3	USBD+	USB Serial Data Interface differential pair, positive signal	16	CLKREQ#	Request that REFCLK be enabled
4	CPUSB#	USB Interface presence detect	17	CPPE#	PCI Express interface presence detect
5	Reserved_5	Reserved	18	REFCLK-	PCI Express reference clock differential pair, negative signal

Pin	Signal	Description	Pin	Signal	Description
6	Reserved_6	Reserved	19	REFCLK+	PCI Express reference clock differential pair, positive signal
7	SMBCLK	System Management Bus Clock (Optional Signal)	20	GND_20	Ground
8	SMBDATA	System Management Bus Data (Optional Signal)	21	PCIEx_RX-	PCI Express Receiver differential pair negative signal, Lane x
9	+1.5V_9	Secondary voltage source, 1.5V	22	PCIEx_RX+	PCI Express Receiver differential pair positive signal, Lane x
10	+1.5V_10	Secondary voltage source, 1.5V	23	GND_23	Ground
11	WAKE#	Request that the host interface return to full operation and respond to PCI Express	24	PCIEx_TX-	PCI Express Transmitter differential pair negative signal, Lane x
12	+3.3VAUX	Auxiliary voltage source, 3.3V	25	PCIEx_TX+	PCI Express Transmitter differential pair positive signal, Lane x
13	PERST#	PCI Express Reset	26	GND_26	Ground

3.4.1 Routing Considerations for PCI Express and USB

See section 4 of this document for trace routing guidelines and the Qseven™ specification for more information about this subject.

3.5 Gigabit Ethernet Signals

Qseven™ modules optionally provide one 10/100/1000BaseT Gigabit Ethernet LAN port compliant with the IEEE 802.3ab specification.

The LAN interface of the Qseven™ module consists of 4 pairs of low voltage differential pair signals designated from *'GBE_MDI0'* (+ and -) to *'GBE_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetics to the carrier board.

Table 3-11 Signal Definition Ethernet

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a situation in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		

GBE_LINK#	13	Ethernet controller link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_LINK100#	7	Ethernet controller 100Mbit/sec link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_LINK1000#	8	Ethernet controller 1000Mbit/sec link indicator, active low.	CMOS 3.3V OD	max 10 mA	O
GBE_ACT#	14	Ethernet controller activity indicator, active low.	CMOS 3.3V OD	max 10 mA	O

3.5.1 LAN Implementation Guidelines

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the Qseven™ module. It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests. Even if a Qseven™ module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

3.5.1.1 LAN Magnetics Modules

1000Base-T Ethernet magnetics modules are similar to those designed solely for 10/100 BaseTx Ethernet, except that there are four MDI differential signal pairs instead of two. 1000Base-T magnetics modules have a center tap pin that is connected to the reference voltage output *'GBE_CTREF'* of the Qseven™ module, which biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with one or two center tap pins. The isolation magnetics can be integrated in a RJ45 jack, which also provides activity and speed LED indicators. Alternatively, they can be designed as discrete magnetics modules, which will be connected to a pure RJ45 jack. Table 3-12 lists recommended magnetics modules and RJ45 jacks for usage on a carrier board design.

Table 3-12 Recommended LAN Magnetic Modules

Manufacturers	Part Number	Technology	Comments
Pulse Engineering	H5007	10/100/1000BaseT	Discrete magnetics module
Pulse Engineering	JK0-0036	10/100/1000BaseT	RJ45 jack with integrated magnetics and activity LEDs
Bel Fuse	S558-5999–P3	10/100/1000BaseT	Discrete magnetics module
Pulse	JW0A1P01R-E	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks
Foxconn	UB11123-J51	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks

3.5.1.2 LAN Component Placement

When using RJ45 connectors without integrated magnetics, the discrete magnetics module has to be placed as close as possible to the RJ45 connector. The distance between the magnetics module and RJ45 connector must be less than 1 inch. This distance requirement must be observed during the carrier board layout when implementing LAN. Due to the insertion loss budget of Qseven™, the overall trace

length of the MDI signal pairs on the carrier board should be less than 4 inches. Signal attenuation could cause data transfer problems for traces longer than 4 inches.

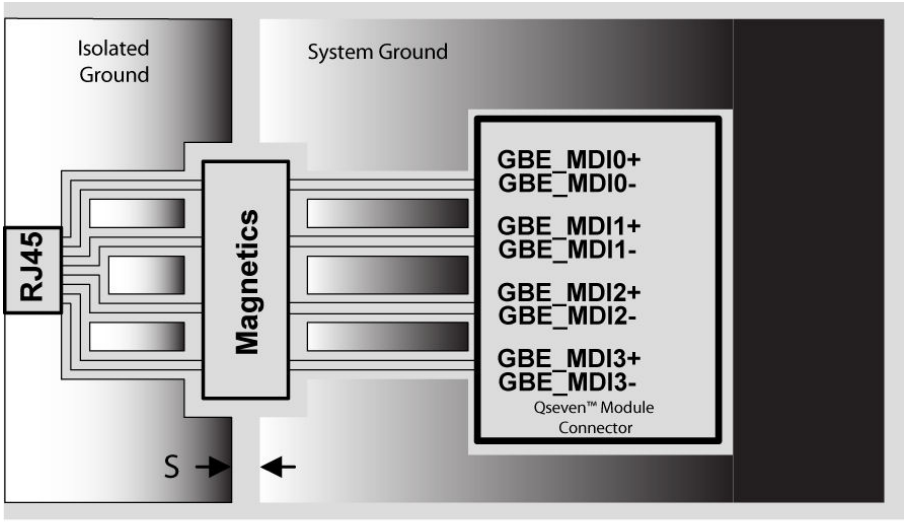
3.5.1.3 LAN Ground Plane Separation

Isolated separation between the analog ground plane and digital ground plane is recommended. If this is not implemented properly then bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to ground bounce noise.

The plane area underneath the magnetic module should be left empty. This free area is to keep transformer induced noise away from the power and system ground planes.

The isolated ground, also called chassis ground, connects directly to the fully shielded RJ45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection, a 3kV high voltage capability capacitor is recommended to connect to this chassis ground. Additionally, a ferrite bead can be placed parallel to the capacitor.

Figure 3-9 LAN Ground Plane Separation



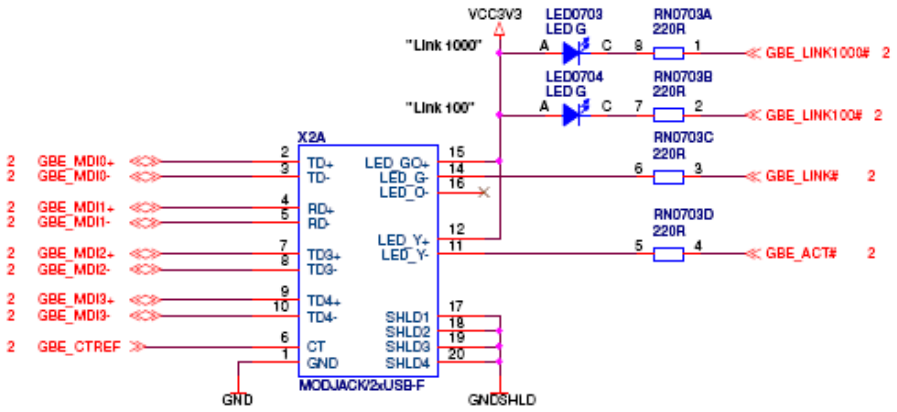
S= Ground Plane Separation

3.5.1.4 LAN Link Activity and Speed LED

The Qseven™ module has four 3.3V open drain outputs to directly drive activity, speed indication and link status LEDs. The 3.3V standby voltage should be used as LED supply voltage so that the link activity can be viewed during system standby state. Since LEDs are likely to be integrated into a RJ45 connector with integrated magnetics module, the LED traces need to be routed away from potential sources of EMI noise. Consider adding a filtering capacitor per LED for extremely noisy situations. The suggested value for this capacitor is 470pF.

3.5.1.5 LAN Reference Schematics

Figure 3-10 Example for Ethernet Magnetics



3.5.2 Routing Considerations for LAN

See section 4 of this document for trace routing guidelines and the Qseven™ specification for more information about this subject.

3.6 Serial ATA Interface Signals

Serial ATA (SATA) is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. Serial ATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard Serial ATA provides a maximum effective data transfer rate of 150MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300MB/s per port is possible. Serial ATA is completely software transparent to the IDE interface while providing a lower pin count and higher performance.

All Qseven™ modules provide up to 2 Serial ATA channels, each with a receive and transmit differential signal pair designated from *'SATA0_RX'* (+ and -) to *'SATA1_RX'* (+ and -) and correspondingly from *'SATA0_TX'* (+ and -) to *'SATA1_TX'* (+ and -). The appropriate signals can be found on the Qseven™ module connector.

Table 3-13 Signal Definition SATA

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	SATA		I
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	SATA		O
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	SATA		I
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	SATA		O
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	max. 10mA	O

Figure 3-11 shows an example for the implementation of a Serial ATA hard drive connector on the Qseven™ carrier board (in this example Serial ATA channel 0 of the Qseven™ module is used). The Serial ATA hard drive can be powered directly from a standard ATX power supply or by a Serial ATA power connector implemented on the carrier board.

Figure 3-11 Example for Serial ATA Implementation (Data and Power)

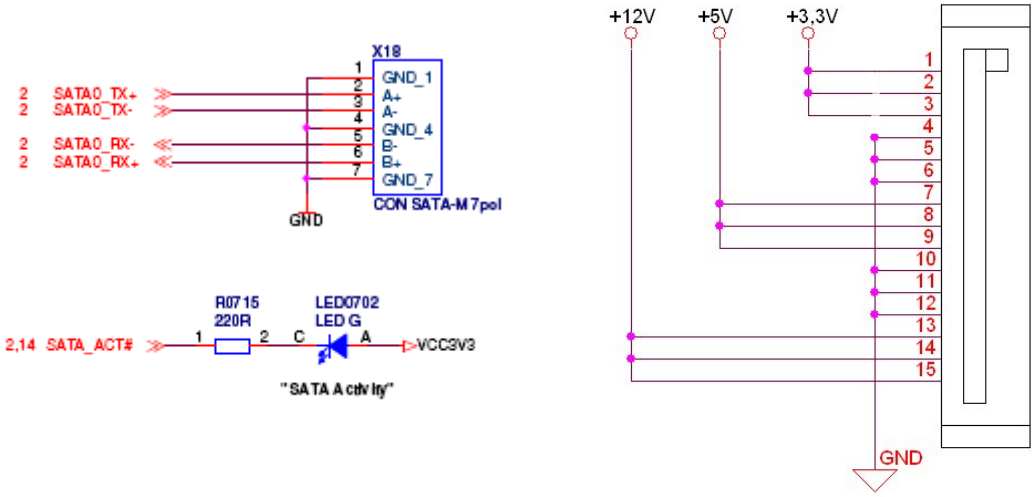


Table 3-14 Serial ATA Data Connector Pinout and Signal Description

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	5	RX-	Receiver differential pair negative signal
2	TX+	Transmitter differential pair positive signal	6	RX+	Receiver differential pair positive signal
3	TX-	Transmitter differential pair negative signal	7	GND	Ground
4	GND	Ground			

Table 3-15 Serial ATA Power Connector Pinout and Signal Description

Pins	Signal	Description	Pins	Signal	Description
1 2 3	+3.3V	3.3V power supply	10 11 12	GND	Ground
4 5 6	GND	Ground	13 14 15	+12V	12V power supply
7 8 9	+5V	5V power supply			

3.6.1 Routing Considerations for Serial ATA

See section 4 of this document for trace routing guidelines and the Qseven™ specification for more information about this subject.

3.7 USB Interface Signals

The Universal Serial Bus interface of the Qseven™ module is compliant to USB 1.1 as well as USB 2.0 specification. Qseven™ specifies a minimum configuration of 4 USB ports up to a maximum of 8 ports.

Note

Depending on the Qseven™ module's chipset, some USB ports may not support both USB 1.1 and USB 2.0.

Table 3-16 Signal Definition USB

Signal	Pin #	Description	I/O Type	I_{OL}/I_{IL}	I/O
USB_P0+ USB_P0-	96 94	Universal Serial Bus Port 0 differential pair.	USB		I/O
USB_P1+ USB_P1-	95 93	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	USB		I/O
USB_P2+ USB_P2-	90 88	Universal Serial Bus Port 2 differential pair.	USB		I/O
USB_P3+ USB_P3-	89 87	Universal Serial Bus Port 3 differential pair.	USB		I/O
USB_P4+ USB_P4-	84 82	Universal Serial Bus Port 4 differential pair.	USB		I/O
USB_P5+ USB_P5-	83 81	Universal Serial Bus Port 5 differential pair.	USB		I/O
USB_P6+ USB_P6-	78 76	Universal Serial Bus Port 6 differential pair.	USB		I/O
USB_P7+ USB_P7-	77 75	Universal Serial Bus Port 7 differential pair.	USB		I/O
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_HOST_PRES#	91	USB client present detect pin. The USB port 1 may operate as USB client or USB host. If USB port 1 is configured as client port then this pin indicates that an external USB host is connected to USB port 1.	CMOS 3.3V	≥ 5 mA	I
USB_HC_SEL	92	USB Host control select pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.			

3.7.1 USB Reference Schematics

The power distribution for the four USB ports in the example below is handled by a 'MIC2026' dual channel power distribution switch from Micrel (http://www.micrel.com). Some Qseven™ modules are capable of generating wake up events over the USB interface during S3 or S5 system state.

Note

In the example shown below the USB ports are powered by the 5V main power rail. For this reason the wake up functionality cannot be supported. If wake up functionality is required the USB ports must be powered by the 5V standby power rail.

Figure 3-12 USB Reference Circuitry

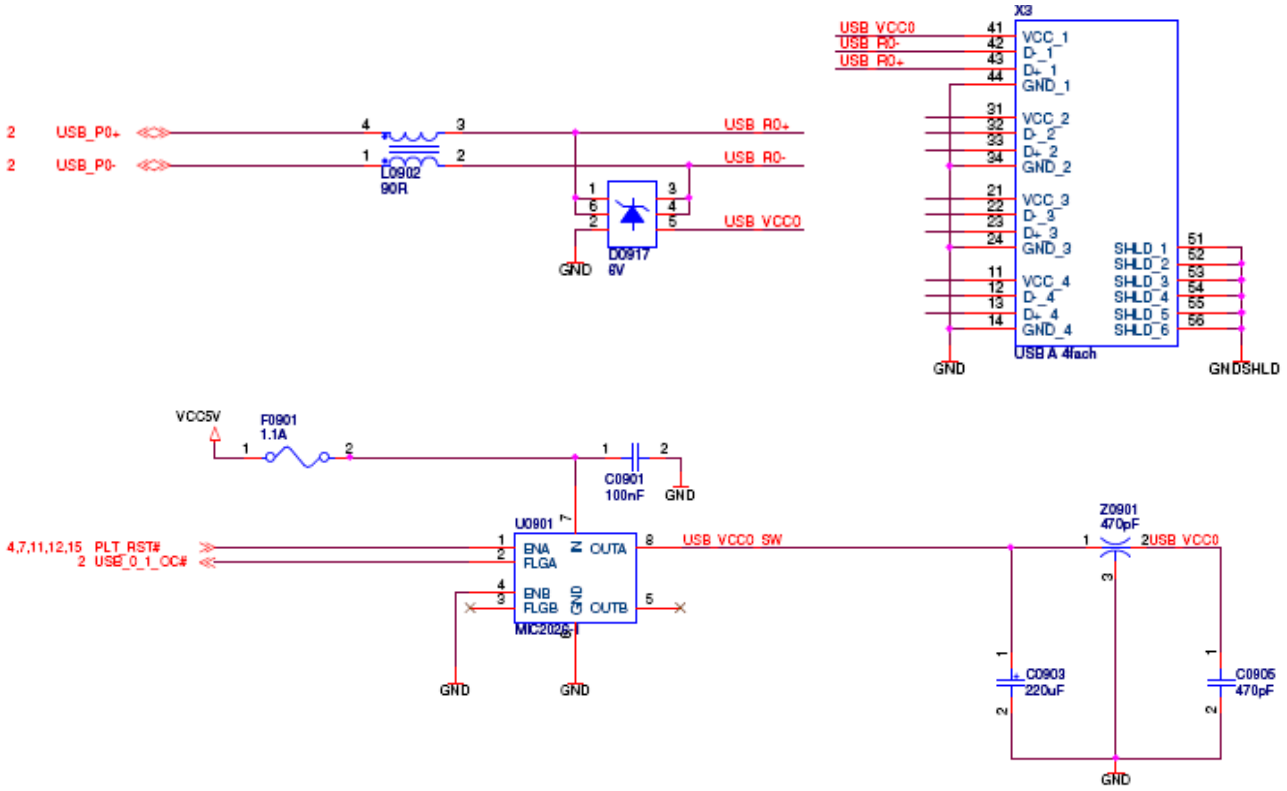


Table 3-17 USB Connector Pinout

Signal	Pin	Description	I/O	Comment
VCC	1	+5V Power Supply	P 5V	
-DATA	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
+DATA	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
GND	4	Ground	P	

3.7.2 USB Implementation Guidelines

3.7.2.1 USB Over-Current Protection

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the carrier board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found at http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the carrier board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered. Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding Qseven™ module's USB over-current sense signals.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB over-current protection and therefore can be used as a replacement for power distribution switches.

3.7.2.2 EMI/ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the carrier board design.

To protect the USB host interface of the module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), it is highly recommended to use low capacitance steering diodes and transient voltage suppression diodes that must be implemented on the carrier board (for example SR05 RailClamp®' surge rated diode arrays from Semtech, http://semtech.com).

3.7.3 Routing Considerations for USB

See section 4 of this document for trace routing guidelines and the Qseven™ specification for more information about this subject.

3.8 SDIO Interface Signals

SDIO (Secure Digital I/O) provides an easy to implement solution for high-speed data I/O combined with low power consumption. SDIO cards are fully compatible with SD memory cards. This includes mechanical, electrical, power, signaling and software compatibility. SDIO hosts are able to drive SD cards and MMC (MultiMediaCards) as well as SDIO cards that provide functions such as Ethernet or WLAN, GPS receivers, Bluetooth, modems etc.

The Qseven™ specification defines one optional 8-bit SDIO interface on the module.

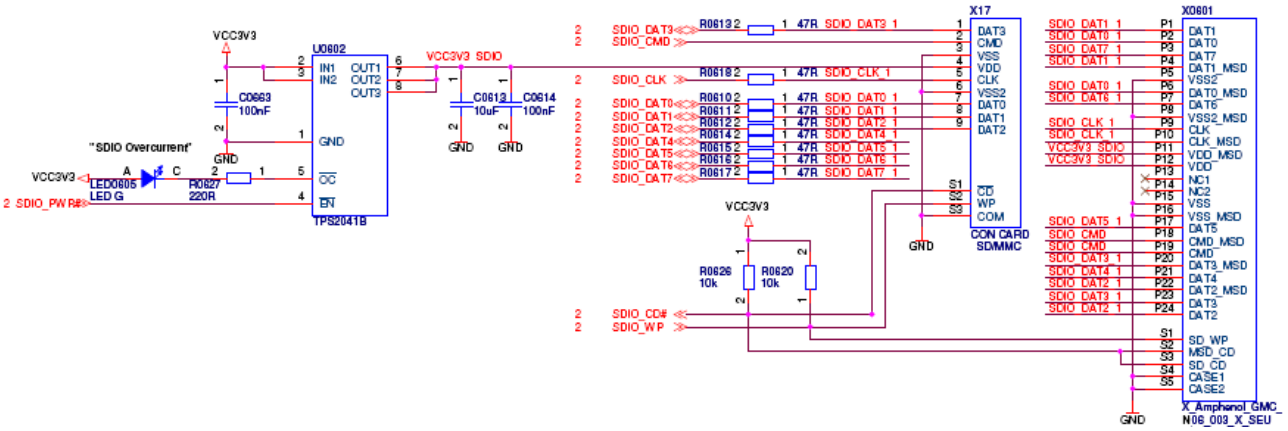
Table 3-18 Signal Definition SDIO

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	CMOS 3.3V		I/O
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	CMOS 3.3V		O
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	CMOS 3.3V OD/PP		I/O
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	CMOS 3.3V	max 1 mA	O
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	CMOS 3.3V		I/O
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	CMOS 3.3V		O
SDIO_DAT0-7	48 to 55	SDIO Data lines. These signals operate in push-pull mode.	CMOS 3.3V PP		I/O

3.8.1.1 SDIO Card Implementation Example

The example shown below is implemented on the Qseven™ evaluation carrier board. The over-current protection of the SDIO host is implemented with the current limited, power distribution switch TPS2041B from Texas Instruments (http://www.ti.com).

Figure 3-13 Example for SDIO Card Implementation



3.9 High Definition Audio Signals

All Qseven™ modules support the High Definition Audio (HDA) Digital Interface (AC-link), specifically designed for implementing audio and modem I/O functionality.

Table 3-19 Signal Definition HDA

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
HDA_RST#	61	HD Audio Codec Reset.	CMOS 3.3V		O
HDA_SYNC	59	Serial Bus Synchronization.	CMOS 3.3V		O
HDA_BITCLK	63	HD Audio 24 MHz Serial Bit Clock from Codec.	CMOS 3.3V		O
HDA_SDO	67	HD Audio Serial Data Output to Codec.	CMOS 3.3V		O
HDA_SDI	65	HD Audio Serial Data Input from Codec.	CMOS 3.3V		I

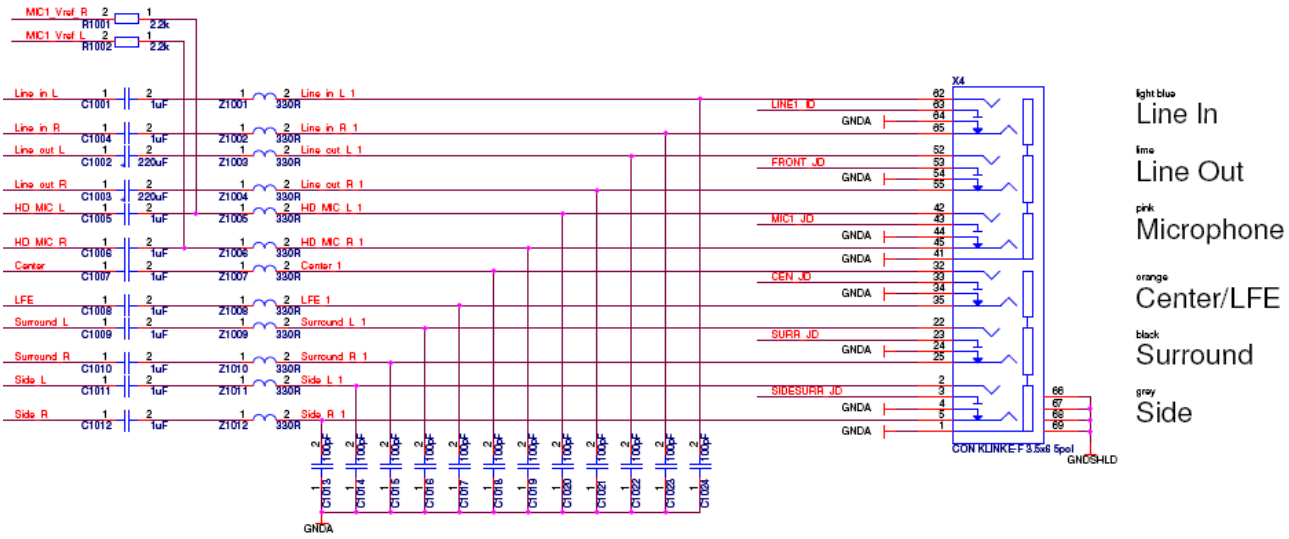
Note

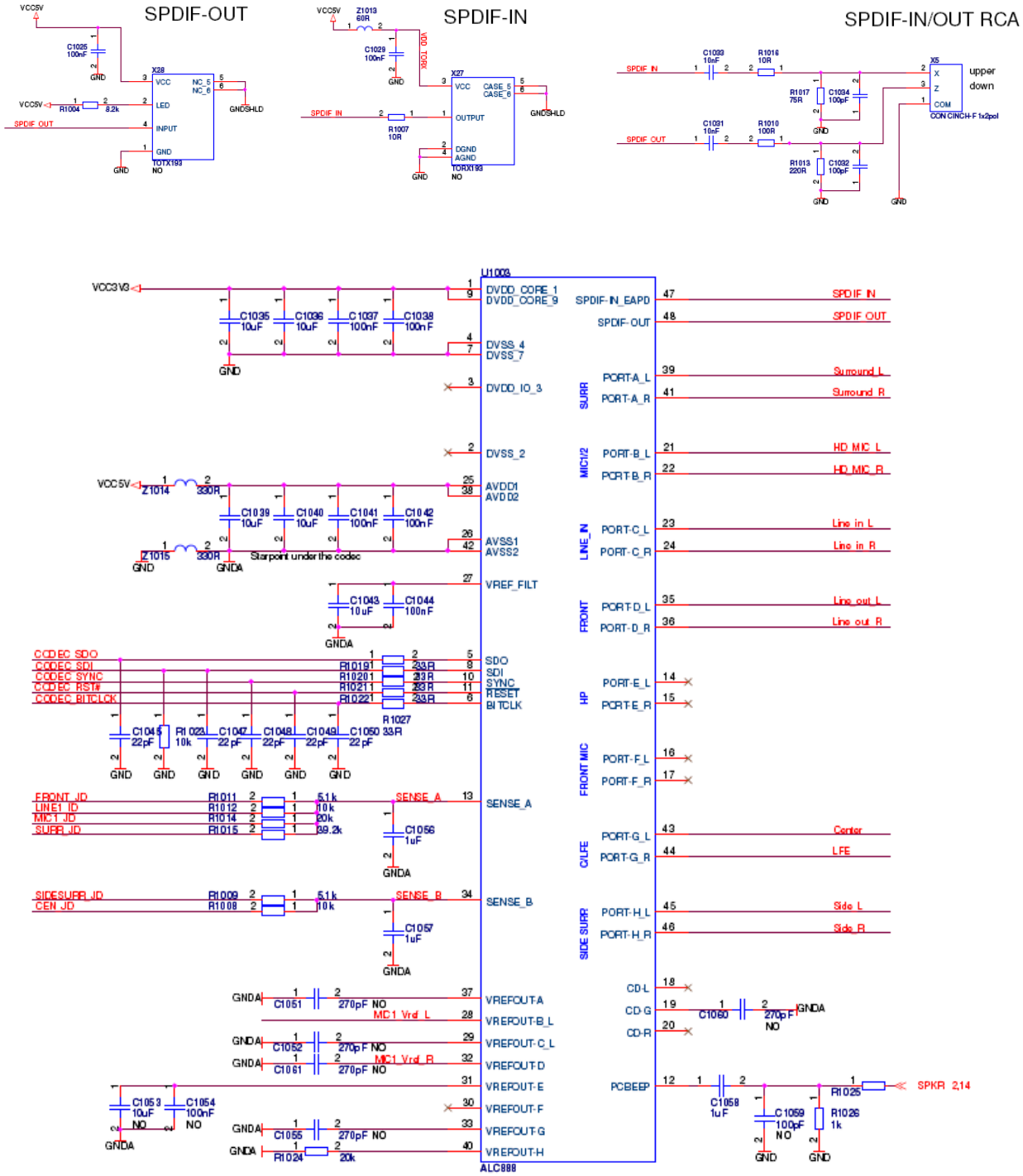
The High Definition Audio interface found on the Qseven™ module complies with Intel® High Definition Audio Specification 1.0.

3.9.1 HDA Implementation Example

The example in Figure 3-14 shows the implementation of the Realtek ALC888 HDA Codec (http://www.realtek.com.tw). This HDA Codec is used on the Qseven™ evaluation carrier board.

Figure 3-14 HDA Codec Reference Schematics





3.9.2 HDA Placement and Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the carrier board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

- Traces must be routed with a target impedance of 55Ω with an allowed tolerance of ± 15%.
- Ground return paths for the analog signals must be given special consideration.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.
- Partition the carrier board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Route analog power and signal traces over the analog ground plane.
- Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins, or position the capacitors for the shortest connections to pins, with wide traces to reduce impedance.
- Do not completely isolate the analog/audio ground plane from the rest of the carrier board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main carrier board ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

3.10 LVDS Flat Panel Signals

The Qseven™ specification defines a LVDS flat panel interface that optionally supports up to two 24-bit LVDS channels. It permits dual pixel, two channel data transmission between the host and flat panel display. Each LVDS channel consists of up to five LVDS signal pairs transmitting a serial bit stream directly to a LVDS flat panel or to an external LVDS receiver. Additional control signals, as well as a dedicated I²C bus interface, are specified to control flat panel attributes. This dedicated I²C bus can be used to connect an external I²C EEPROM containing the specific timing data of the flat panel. The applicable signals can be found on the Qseven™ module connector.

Table 3-20 LVDS Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
LVDS_PPEN	111	Controls panel power enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLEN	112	Controls panel backlight enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLT_CTRL	123	Controls the panel backlight brightness via pulse width modulation (PWM)	CMOS 3.3V		O
LVDS_A0+ LVDS_A0-	99 101	LVDS primary channel differential pair 0.	LVDS		O
LVDS_A1+ LVDS_A1-	103 105	LVDS primary channel differential pair 1.	LVDS		O
LVDS_A2+ LVDS_A2-	107 109	LVDS primary channel differential pair 2.	LVDS		O
LVDS_A3+ LVDS_A3-	113 115	LVDS primary channel differential pair 3.	LVDS		O
LVDS_A_CLK+ LVDS_A_CLK-	119 121	LVDS primary channel differential pair clock lines.	LVDS		O
LVDS_B0+ LVDS_B0-	100 102	LVDS secondary channel differential pair 0.	LVDS		O
LVDS_B1+ LVDS_B1-	104 106	LVDS secondary channel differential pair 1.	LVDS		O
LVDS_B2+ LVDS_B2-	108 110	LVDS secondary channel differential pair 2.	LVDS		O
LVDS_B3+ LVDS_B3-	114 116	LVDS secondary channel differential pair 3.	LVDS		O
LVDS_B_CLK+ LVDS_B_CLK-	120 122	LVDS secondary channel differential pair clock lines.	LVDS		O
LVDS_DID_CLK	127	DisplayID DDC clock line used for LVDS flat panel detection.	CMOS 3.3V OD		I/O
LVDS_DID_DAT	125	DisplayID DDC data line used for LVDS flat panel detection.	CMOS 3.3V OD		I/O
LVDS_BLC_CLK	128	Control clock signal for external SSC clock chip.	CMOS 3.3V OD		I/O
LVDS_BLC_DAT	126	Control data signal for external SSC clock chip.	CMOS 3.3V OD		I/O

Note

The LVDS flat panel configuration within the BIOS of the Qseven™ module shall be implemented in accordance to the DisplayID specification that is under development within the Video Electronics Standards Association (VESA). For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA).

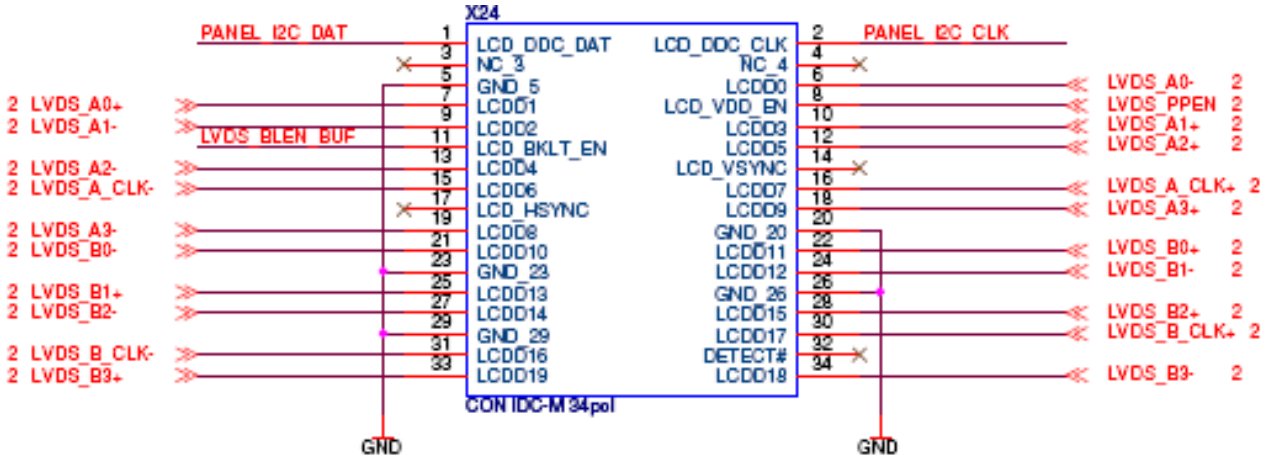
3.10.1 LVDS Implementation Guidelines

Many carrier board designs do not need the full range of LVDS performance offered by Qseven™ modules. It depends on the flat panel configuration of the Qseven™ module, as well as the carrier board design, as to how many LVDS signal pairs are supported. While the dual channel 24-bit LVDS configuration needs all 10 LVDS signal pairs, a single channel 18-bit LVDS configuration only requires 4 LVDS signal pairs. In this case all unused LVDS signal pairs should be left open on the carrier board.

If the LVDS display interface of the Qseven™ module is not implemented, all signals associated with this interface should be left open.

The Qseven™ Consortium doesn't define the connector layout for interfacing LVDS on the Qseven™ carrier board design. It is up to the system designer and the system requirements as to which connectors and which pinout will be used for the application. The following reference circuitry in Figure 3-15 should only be considered as an example of how to implement the LVDS interface on the carrier board.

Figure 3-15 LVDS Connector



3.10.1.1 Connector and Cable Considerations

When implementing LVDS signal pairs on a single-ended carrier board connector, the signals of a pair should be arranged so that the positive and negative signal are side by side. The trace lengths of the LVDS signal pairs between the Qseven™ module and the connector on the carrier board should be the same when possible. Additionally, one or more ground traces/pins must be placed between the LVDS pairs.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver.

Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Ribbon cables are a cost effective and easy solution. Even though they are not well suited for high-speed differential signaling they do work fine for very short runs. Most cables will work effectively for cable distances of <0.5m.

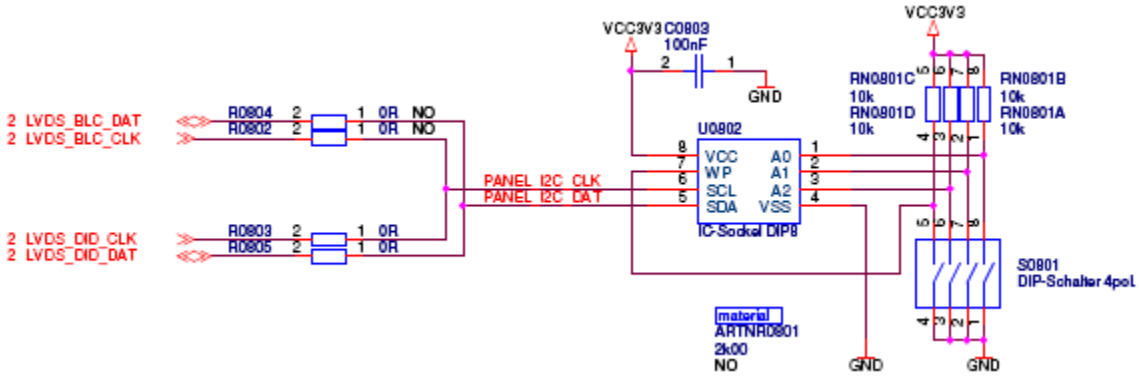
The cables and connectors that are to be utilized should have a differential impedance of 100Ω ±15%. They should not introduce major impedance discontinuities that cause signal reflections.

For more information about this subject refer to the 'LVDS Owners Manual Chapter 6' available from National Semiconductor (http://www.national.com).

3.10.1.2 Display Timing Configuration

Usually the timing parameters for the flat panel display are stored in an external EEPROM that is implemented on the Qseven™ carrier board. It is accessible through the dedicated LVDS I²C bus via the signals *'LVDS_DID_CLK'* and *'LVDS_DID_DAT',* which can be found on the module's connector. During POST the module's BIOS reads out the display timing data from the EEPROM and configures the module's graphics controller for proper flat panel operation. In order to be able to do this, the device address of the LVDS I²C EEPROM must be strapped to 0xA0. For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA) (http://www.vesa.org).

Figure 3-16 LVDS I²C EEPROM

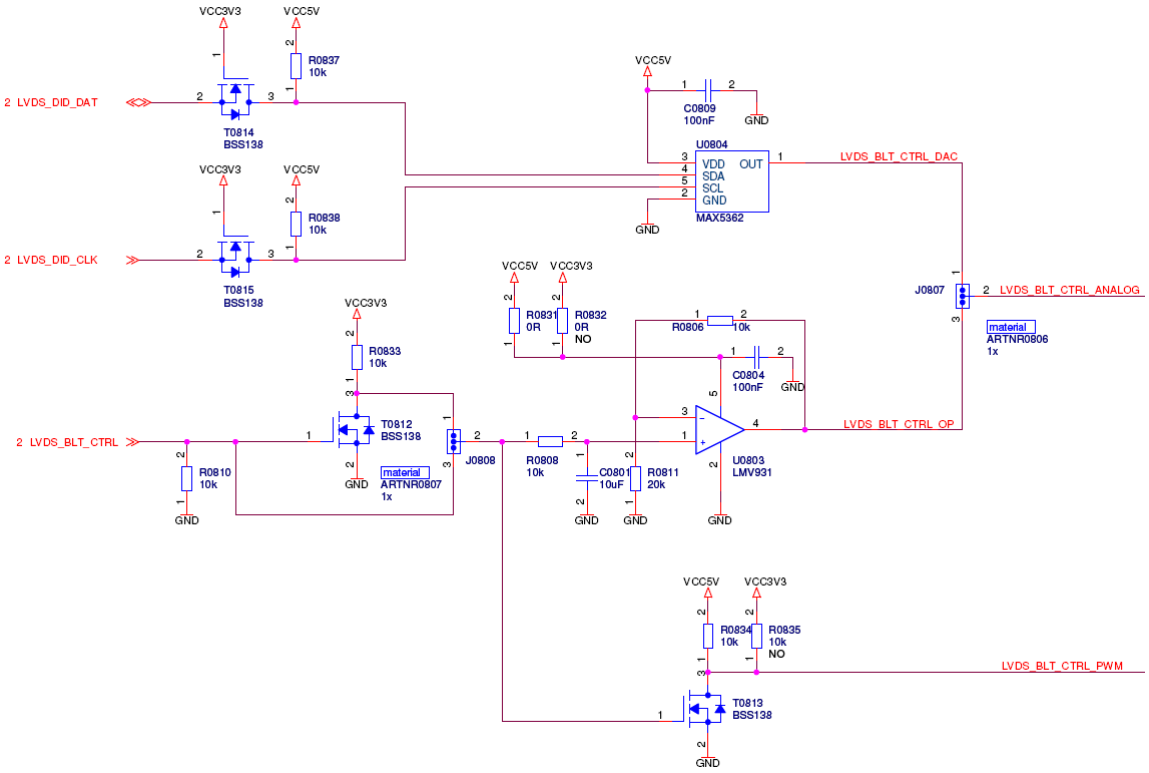


3.10.1.3 Backlight Control

The following LVDS reference circuitry shows a backlight control solution using the digital potentiometer MAX5362 from Maxim (www.maxim-ic.com). Usually common backlight inverters are either voltage or resistor controlled. Therefore digital potentiometers are a flexible solution to meet the requirements of most inverters. If a backlight inverter is resistance controlled, the digital potentiometer can be connected directly to the backlight control input of the inverter. Otherwise the potentiometer can be used to implement a simple voltage divider driving the backlight voltage control input pin of the inverter. In both cases the signal level of the Qseven™ signals must be adapted to the specified level of the used devices. In the example used on the Qseven evaluation carrier board the signals LVDS_BLT_CTRL , LVDS_DID_DAT and LVDS_DID_CLK have been level shifted from 3.3V to 5V by using the FET's T0812, T0814 and T0815.

Backlight control is part of the EASI (Embedded Application Software Interface) API and can be accessed by using the 32bit API functions. For more details about EASI refer to the Qseven™ specification and the EASI Programmers Guide.

Figure 3-17 LVDS Backlight Control



3.10.2 Routing Considerations for LVDS

See section 4 of this document for trace routing guidelines and the Qseven™ specification and the 'LVDS Owners Manual Chapter 3' from National Semiconductor (http://www.national.com) for more information about this subject.

3.11 SDVO Interface Signals

SDVO was developed by Intel® Corporation to interface third party SDVO compliant display controller devices that may have a variety of output formats, including DVI, LVDS, HDMI and TV-Out. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependent upon the active display resolution and timing.

Qseven™ modules optionally provide one SDVO port that consists of 7 pairs of low voltage differential pair signals and a dedicated I²C bus (*SDVO_CTRL_CLK* and *SDVO_CTRL_DAT)* that is used to control the external SDVO devices and to read out the display timing data from the connected display.

Table 3-21 Signal Definition SDVO

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SDVO_BCLK- SDVO_BCLK+	133 131	SDVO differential pair clock lines.	PCIE		O
SDVO_INT- SDVO_INT+	134 132	SDVO differential pair interrupt input lines.	PCIE		I
SDVO_GREEN- SDVO_GREEN+	139 137	SDVO differential pair green data lines.	PCIE		O
SDVO_BLUE- SDVO_BLUE+	145 143	SDVO differential pair blue data lines.	PCIE		O
SDVO_RED- SDVO_RED+	151 149	SDVO differential pair red data lines.	PCIE		O
SDVO_FLDSTALL- SDVO_FLDSTALL+	140 138	SDVO differential pair field stall lines.	PCIE		I
SDVO_TVCLKIN- SDVO_TVCLKIN+	146 144	SDVO differential pair TV-Out synchronization clock lines.	PCIE		I
SDVO_CTRL_CLK	152	I²C based control signal (clock) for SDVO device. ***Note:*** *If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	CMOS 3.3V OD		I/O
SDVO_CTRL_DAT	150	I²C based control signal (data) for SDVO device. ***Note:*** *If the control bus from the SDVO device has a different signaling voltage, then a level shifting device will be required on the carrier board to properly translate the voltage level for this signal.*	CMOS 3.3V OD		I/O

Note

Support of the SDVO interface is chipset dependent and therefore may not be available on all Qseven™ modules. The SDVO interface signals are shared with the signals for the DisplayPort interface and/or the TMDS interface.

3.11.1.1 SDVO Port Configuration

The SDVO port and device configuration is fixed within the Intel® Graphics Video BIOS implementation of the Qseven™ modules. All modules assume an I²C bus address 70h for SDVO devices implemented on the Qseven™ carrier board.

Table 3-22 SDVO Port Configuration

	SDVO Port
Device Type	Selectable in BIOS Setup Program.
I²C Address	70h
I²C Bus	SDVO I²C GPIO pins
DDC Bus	SDVO I²C GPIO pins

3.11.1.2 Supported SDVO Devices

Due to the fact that SDVO is an Intel® defined interface, the number of supported SDVO devices is limited to devices that are supported by the Intel® graphics video BIOS and graphics driver software.

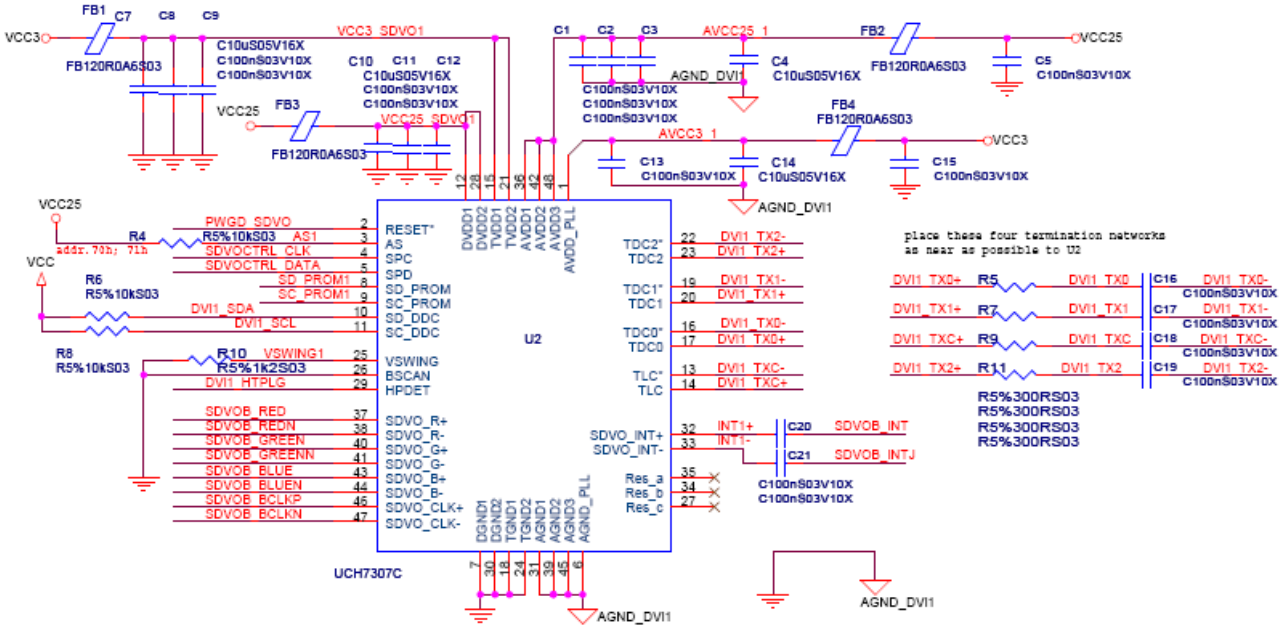
Table 3-23 Intel® SDVO Supported Device Descriptions

Device	Vendor	Type	Link
CH7021A	Chrontel	SDTV / HDTV	http://www.chrontel.com
CH7308A	Chrontel	LVDS	http://www.chrontel.com
CH7307C	Chrontel	DVI	http://www.chrontel.com
CH7312	Chrontel	DVI	http://www.chrontel.com
CX25905	Conexant	DVI-D / TV / CRT	http://www.conexant.com
SiL1362/1364	Silicon Image	DVI	http://www.siliconimage.com
SiL 1390	Silicon Image	HDMI	http://www.siliconimage.com

3.11.2 SDVO to DVI Transmitter Reference Circuitry

The following circuitry shows an example of how to connect a Chrontel CH7307C SDVO DVI transmitter (http://www.chrontel.com) directly to the SDVO channel of the Qseven™ module. When implementing a SDVO device on the carrier board, the I²C bus signals *'SDVO_CTRL_CLK'* and *'SDVO_CTRL_DAT'* should have a 5.6kΩ (±5%) pull-up resistor connected to the 2.5V supply voltage. These pull-up resistors allow the module's graphics controller to determine if the pins, which are shared between the PEG port and the SDVO channels B and C, are used for SDVO functionality. The configuration EEPROM for the Chrontel SDVO transmitter CH7307C is optional.

Figure 3-18 SDVO to DVI Transmitter Reference Circuitry



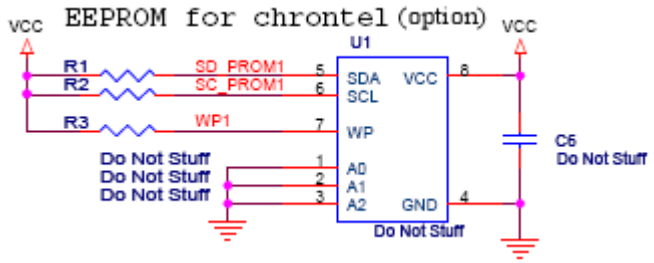
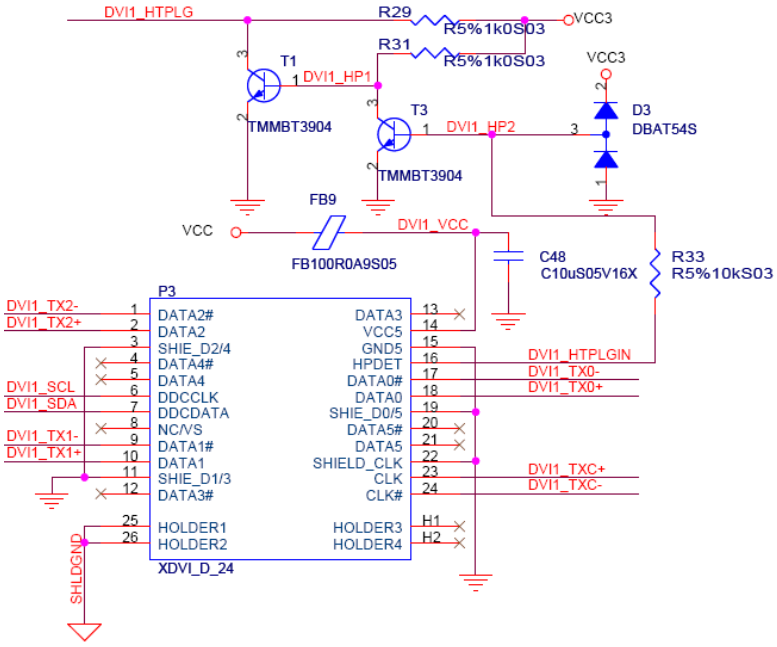


Figure 3-19 DVI Connector Reference Circuitry



3.11.3 Routing Considerations for SDVO

For the SDVO interconnection between the Qseven™ module and a third-party SDVO compliant device, refer to section 4 of this design guide and to the layout and routing considerations specified by the SDVO device manufacturer.

3.11.4 Routing Considerations for DVI

The Digital Video Interface (DVI) is based on the differential signaling method TDMS. To achieve the full performance and reliability of DVI, the TDMS differential signals between the SDVO to DVI transmitter and the DVI connector have to be routed in pairs with a differential impedance of 100Ω. The length of the differential signals must be kept as close to the same as possible. The maximum length difference must not exceed 100mils for any of the pairs relative to each other. Spacing between the differential pair traces should be more than 2x the trace width to reduce trace-to-trace couplings. For example, having wider gaps between differential pair DVI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DVI traces on the same layer. There should be a minimum distance of 30mils. For more information refer to the layout and routing considerations as specified by the manufacturer of the SDVO to DVI transmitter.

3.12 DisplayPort Interface Signals

Qseven™ modules optionally support one DisplayPort interface. This interface is shared with the SDVO and HDMI signals.

DisplayPort is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

The DisplayPort interface supports 1, 2, or 4 data pairs that carry the video signal, clock and optional audio signals. The video signal of the DisplayPort interface is not compatible with DVI or HDMI but a DisplayPort connector can pass these signals through. While DVI and HDMI require separate clock signals, DisplayPort embeds the clock in the data signal. Unlike the separate DVI/HDMI and LVDS standards, DisplayPort supports both external (monitor) or internal (LCD panel) display connections.

Table 3-24 Signal Definition DisplayPort

Signal	Shared With	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
DP_LANE3- DP_LANE3+	SDVO_BCLK- SDVO_BCLK+	133 131	DisplayPort differential pair lines lane 3.	PCIE		O
DP_LANE2- DP_LANE2+	SDVO_BLUE- SDVO_BLUE+	145 143	DisplayPort differential pair lines lane 2.	PCIE		O
DP_LANE1- DP_LANE1+	SDVO_GREEN- SDVO_GREEN+	139 137	DisplayPort differential pair lines lane 1.	PCIE		O
DP_LANE0- DP_LANE0+	SDVO_RED- SDVO_RED+	151 149	DisplayPort differential pair lines lane 0.	PCIE		O
DP_AUX- DP_AUX+	SDVO_FLDSTALL- SDVO_FLDSTALL+	140 138	Auxiliary channel used for link management and device control. Differential pair lines.	PCIE		I/O
DP_HPD#		154	Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Note

Support of the DisplayPort interface is chipset dependent and therefore may not be available on all Qseven™ modules. The DisplayPort interface signals are shared with the signals for the SDVO interface and/or the TMDS interface.

Figure 3-20 DisplayPort Connector

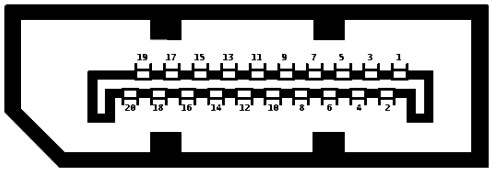


Table 3-25 Pinout DisplayPort Connector

Pin#	Signal	Description	Pin#	Signal	Description
1	DP_LANE0+	DisplayPort Lane 0 (positive)	2	GND	Ground
3	DP_LANE0-	DisplayPort Lane 0 (negative)	4	DP_LANE1+	DisplayPort Lane 1 (positive)
5	GND	Ground	6	DP_LANE1-	DisplayPort Lane 1 (negative)
7	DP_LANE2+	DisplayPort Lane 2 (positive)	8	GND	Ground
9	DP_LANE2-	DisplayPort Lane 2 (negative)	10	DP_LANE3+	DisplayPort Lane 3 (positive)
11	GND	Ground	12	DP_LANE3-	DisplayPort Lane 3 (negative)
13	CONFIG1	Configuration Pin 1 (connected to Ground)	14	CONFIG2	Configuration Pin 2 (connected to Ground)
15	DP_AUX+	Auxiliary Channel (positive)	16	GND	Ground
17	DP_AUX-	Auxiliary Channel (negative)	18	DP_HPD#	Hot Plug Detect
19	RETURN	Return For Power	20	DP_PWR	Power For Connector

3.13 HDMI Interface Signals

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TDMS video stream.

The Qseven™ specification defines a single-link HDMI interface with a pixel clock rate of up to 165MHz. The appropriate TDMS receive and transmit differential signal pair, as well as additional control signals, can be found on the Qseven™ module edge connector. This interface is shared with the SDVO and DisplayPort signals.

Table 3-26 Signal Definition HDMI

Signal	Shared With	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
TMDS_CLK- TMDS_CLK+	SDVO_BCLK- SDVO_BCLK+	133 131	TMDS differential pair clock lines.	TMDS		O
TMDS_LANE0- TMDS_LANE0+	SDVO_BLUE- SDVO_BLUE+	145 143	TMDS differential pair lines lane 0.	TMDS		O
TMDS_LANE1- TMDS_LANE1+	SDVO_GREEN- SDVO_GREEN+	139 137	TMDS differential pair lines lane 1.	TMDS		O
TMDS_LANE2- TMDS_LANE2+	SDVO_RED- SDVO_RED+	151 149	TMDS differential pair lines lane 2.	TMDS		O
HDMI_CTRL_CLK	SDVO_CTRL_CLK	152	DDC based control signal (clock) for HDMI device.	CMOS 3.3V OD		I/O
HDMI_CTRL_DAT	SDVO_CTRL_DAT	150	DDC based control signal (data) for HDMI device.	CMOS 3.3V OD		I/O
HDMI_HPD#		153	Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Note

Level shifters must be implemented on the carrier board for HDMI interface signals in order to be compliant with the HDMI Specification (see chapter 3.13.1).

Note

Support of the TMDS interface is chipset dependent and therefore may not be available on all Qseven™ modules. The TMDS interface signals are shared with the signals for the SDVO interface and/or the DisplayPort interface. The TDMS interface enables Qseven™ modules to support DVI or HDMI

3.13.1 HDMI Implementation

The HDMI interface on Qseven™ modules is provided by the internal graphics chipset. Usually this integrated HDMI interface is multiplexed with the PCI Express Graphics or SDVO interface. Since both of these interfaces are low-swing AC coupled differential inputs, high speed HDMI level shifters are required to translate the signals to the HDMI compliant open-drain current steering Rx terminated differential output.

HDMI level shifters are available from different manufacturers such as:

Chrontel CH7318 (http://www.chrontel.com)
Parade Technologies PS101QFN48G (http://www.paradetech.com)
Pericom Semiconductor PI3VDV411LSZDE (http://www.pericom.com).

Figure 3-21 HDMI Connector

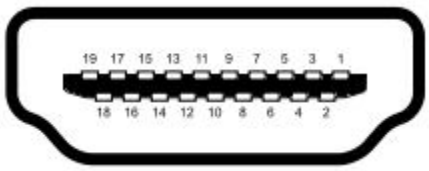


Table 3-27 Pinout HDMI Connector

Pin#	Signal	Description	Pin#	Signal	Description
1	TMDS Data 2+	HDMI Lane 2 (positive)	2	TMDS Data 2 Shield	Shield of Data 2 pair
3	TMDS Data 2-	HDMI Lane 2 (negative)	4	TMDS Data 1+	HDMI Lane 1 (positive)
5	TMDS Data 1 Shield	Shield of Data 1 pair	6	TMDS Data 1-	HDMI Lane 1 (negative)
7	TMDS Data 0+	HDMI Lane 0 (positive)	8	TMDS Data0 Shield	Shield of Data 0 pair
9	TMDS Data 0-	HDMI Lane 0 (negative)	10	TMDS Clock-	HDMI Clock (positive)
11	TMDS Clock Shield	Shield of Clock pair	12	TMDS Clock-	HDMI Clock (negative)
13	CEC	Consumer Electronics Control Interface	14	Reserved	N.C.
15	DDC Clock	DDC based control signal (clock)	16	DDC Data	DDC based control signal (data)
17	GND	Ground	18	+5V	+5V Power Supply
19	HPD	Hot plug detect			

3.14 LPC Interface Signals

The Low Pin Count Interface was defined by Intel® Corporation to facilitate the industry's transition towards legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface firmware hubs, Trusted Platform Module (TPM) devices and embedded controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. For more information about LPC bus refer to the 'Intel® Low Pin Count Interface Specification Revision 1.1'.

Since Qseven™ is designed to be a legacy free standard for embedded modules, it does not support legacy functionality such as PS/2 keyboard/mouse, serial and parallel ports. Instead it provides an LPC interface that can be used to add peripheral devices to the carrier board design. The reduced pin count of the LPC interface makes it easy to implement such devices. All corresponding signals can be found on the module connector.

Table 3-28 Signal Definition LPC

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
LPC_AD[0..3]	185 to 188	Multiplexed Command, Address and Data.	CMOS 3.3V		I/O
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	CMOS 3.3V		O
LPC_LDRQ#	192	LPC DMA request.	CMOS 3.3V		I
LPC_CLK	189	LPC clock.	CMOS 3.3V		O
SERIRQ	191	Serialized Interrupt.	CMOS 3.3V		I/O

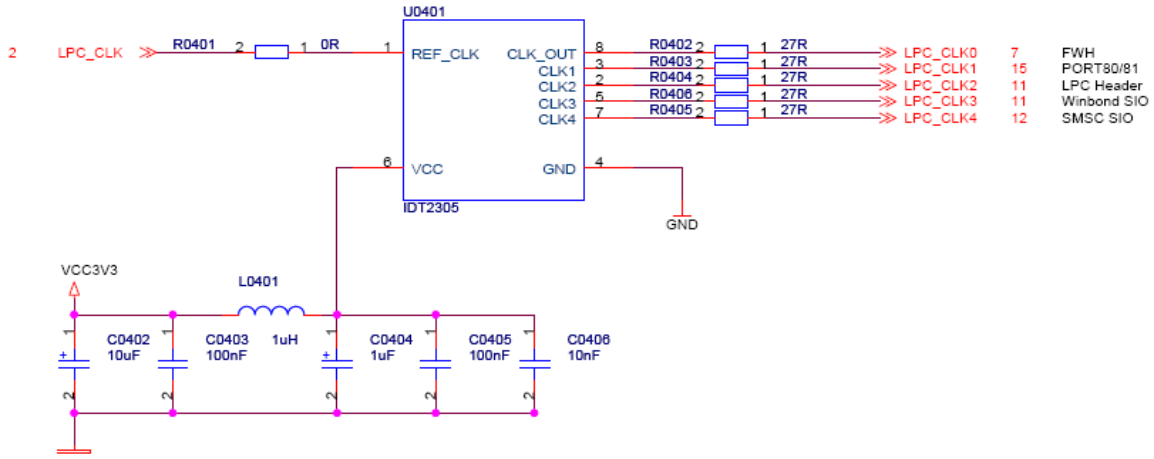
Note

Implementing external LPC devices on the Qseven™ carrier board always requires customization of the Qseven™ module's BIOS in order to support basic initialization for the LPC device. Otherwise the functionality of LPC device will not be supported by a Plug&Play or ACPI capable system.

3.14.1 LPC Bus Clock Signal

Qseven™ specifies a single LPC reference clock signal called *'LPC_CLK'* on the modules connector on pin 189. If more than one LPC clock signal is required on the carrier board to supply several LPC devices, a zero delay buffer must be used to expand the number of LPC clock lines. Figure 3-22 shows an example of how to implement a Integrated Device Technology IDT2305 zero delay clock buffer (http://www.idt.com). This circuitry is also used on the Qseven™ consortium carrier board.

Figure 3-22 LPC Clock Buffer Reference Circuitry



3.14.1.1 Routing Considerations for LPC Clock

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the 'PCI Local Bus Specification Revision 2.3'.

Note

Qseven™ modules based on the Intel® Atom™ Processor and Intel® System Controller Hub US15W can not be booted from external BIOS Firmware Hubs (FWH) that are clocked by a buffered or delayed clock signal.

3.14.2 LPC Reset Signal

The LPC interface should use a reset signal that is generated by splitting the PCI Express reset (PCIE_RST#, pin 158 of the Qseven™ connector) signal with a zero delay buffer. An example can be found in Figure 3-3 of this document. This solution is also used on the Qseven™ consortium evaluation carrier board. Here the LPC reset signal is called *'PLT_RESET#'*. If the carrier board implements more than one LPC device, it is recommended that the LPC reset signal be split so that each LPC device will be provided with a separate reset signal.

3.14.3 LPC Super I/O Support

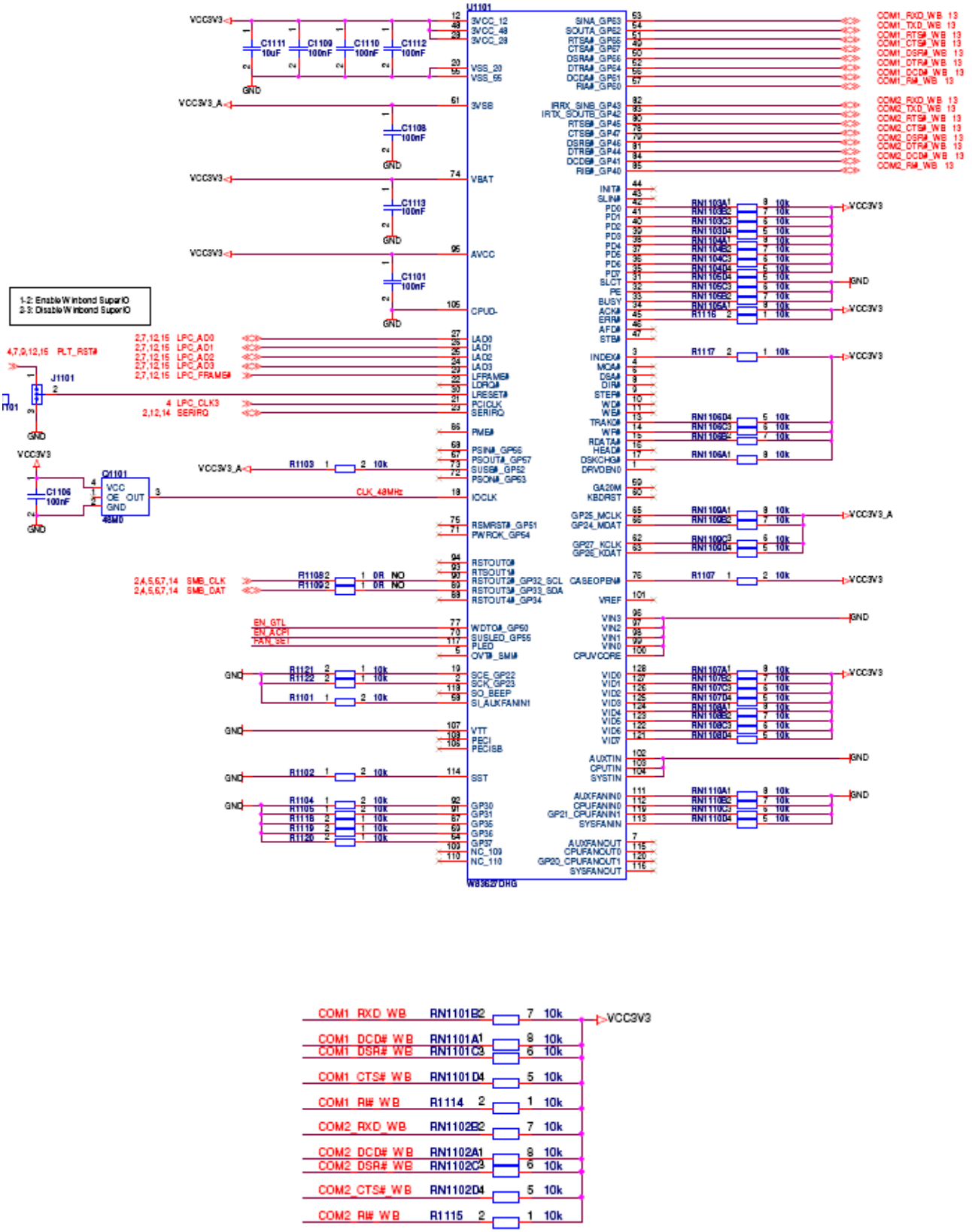
The Qseven™ BIOS firmware includes integrated support for the following external LPC Super I/O controllers in order to provide additional legacy COM ports:

- Nuvoton W83627DHG LPC Super I/O with 2 COM ports (http://www.nuvoton.com)
- SMSC SCH3114 LPC Super I/O with 4 COM ports (http://www.smsc.com)

If any of the additional functionality of the Super I/O is required by the application, then it may be implemented via the application's software program. There are Super I/O functions that can be configured by hardware straps, which is defined within the datasheet of that particular Super I/O (for example PS/2 keyboard functionality).

The base address for these Super I/O controllers shall be 0x2E to be sure that the legacy COM port devices of the Super I/O controller can be initialized by the BIOS.

Figure 3-23 LPC Super I/O Winbond W83627DHG Reference Circuitry



3.14.3.1 Boot Up Configuration for Nuvoton W83627DHG

The default configuration of the Nuvoton W83627DHG LPC Super I/O controller during power-on can be implemented by hardware strap options. The hardware strap pins are located on the serial port interface of the Super I/O controller. They can be enabled by placing a 10kΩ pull-up resistor between +3.3V supply voltage and one of the dedicated hardware strap pins. Figure 3-24 shows the boot strap configuration options for the Nuvoton W83627DHG LPC Super I/O controller.

Figure 3-24 Nuvoton W83627DHG Boot Strap Configuration

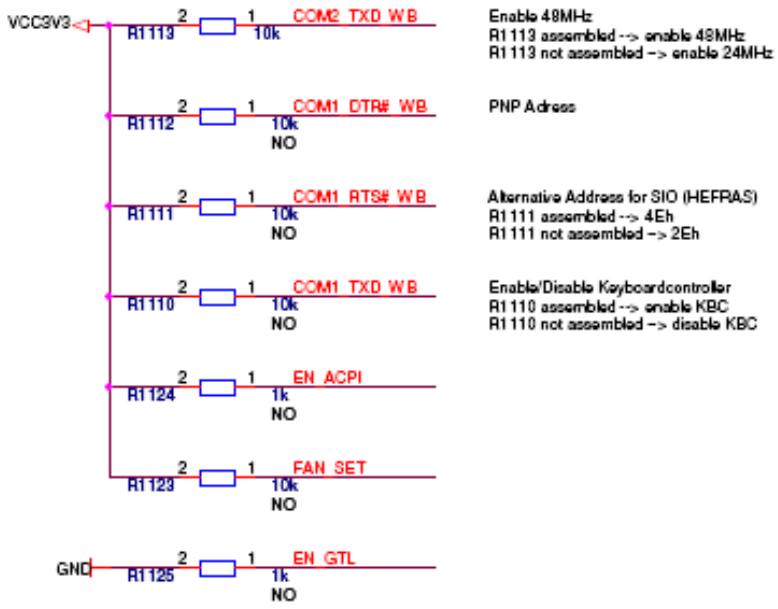
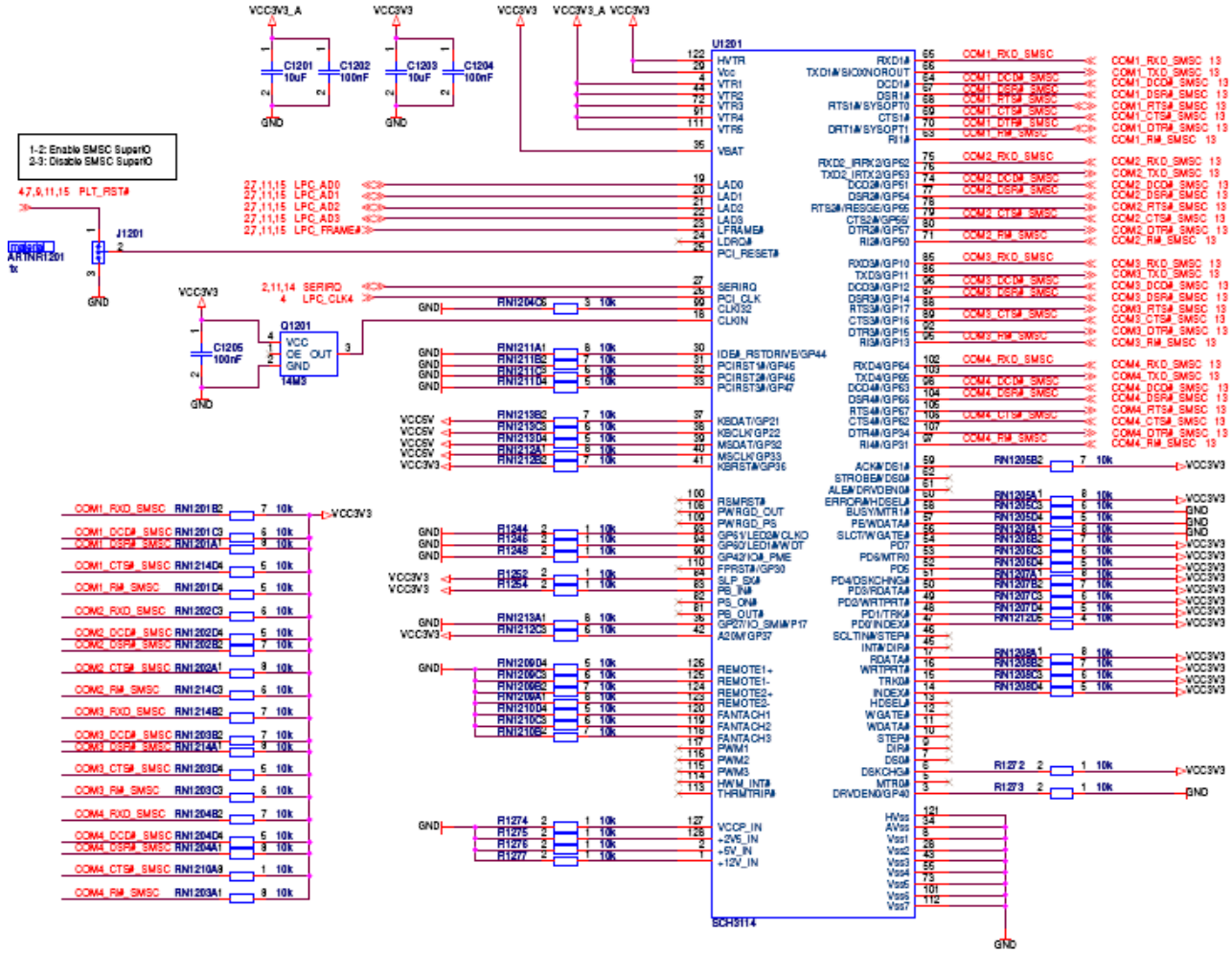


Figure 3-25 LPC Super I/O SMSC SCH3114 Reference Circuitry

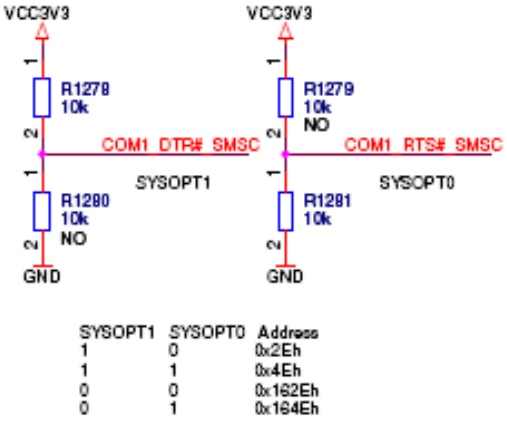


3.14.3.2 Boot Up Configuration for SMSC SCH3114

The default configuration of the SMSC SCH3114 LPC Super I/O controller during power-on can be implemented by hardware strap options. The hardware strap pins are located on the serial port interface of the Super I/O controller. They can be enabled by placing a 4.7kΩ pull-up resistor between +3.3V supply voltage and one of the dedicated hardware strap pins.

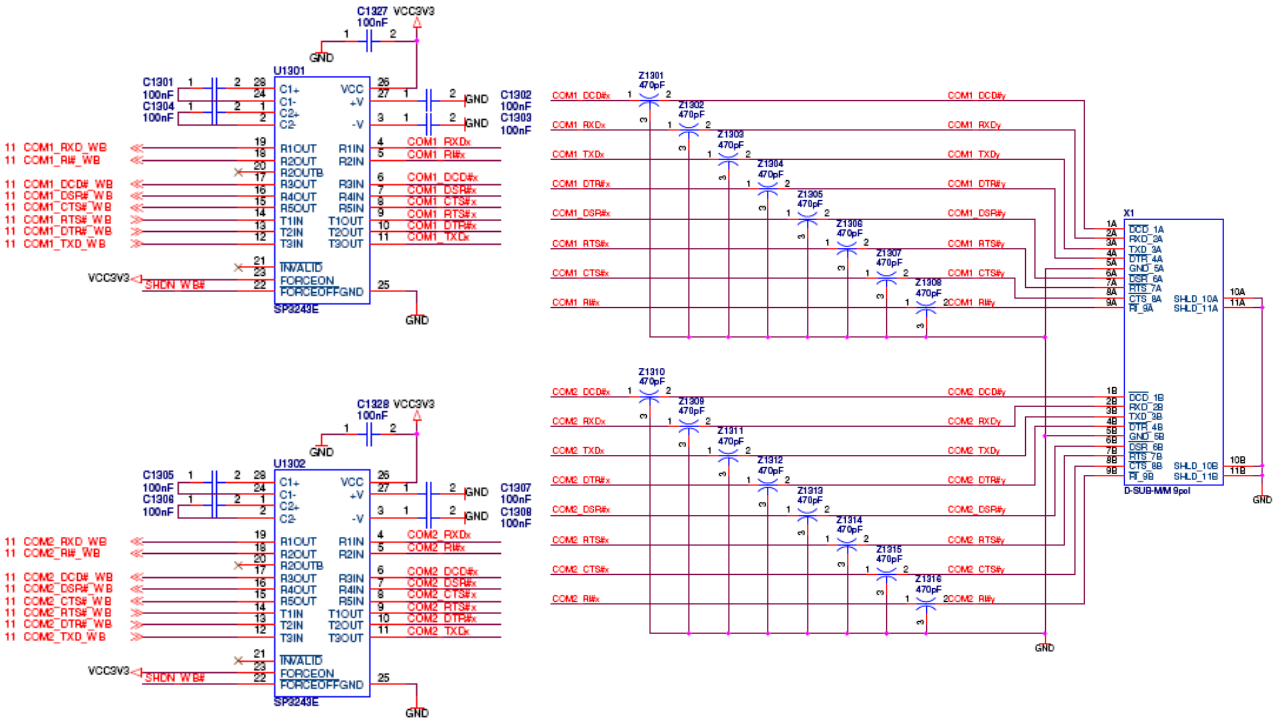
Figure 3-26 shows the boot strap configuration options for the SMSC SCH3114 LPC Super I/O controller.

Figure 3-26 SMSC SCH3114 Boot Strap Configuration



3.14.3.3 RS232 Serial Port Reference Circuitry

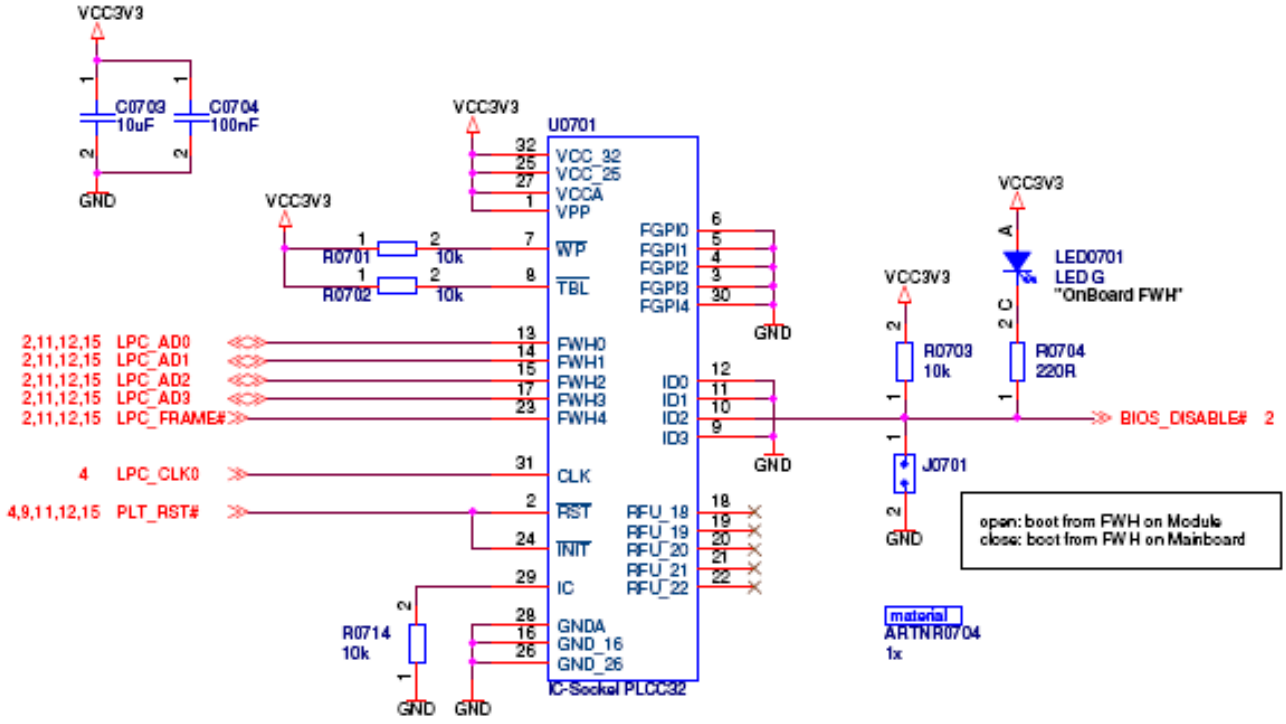
Figure 3-27 COM Port Reference Circuit (RS-232)



3.14.4 LPC Firmware Hub

The LPC bus interface on Qseven™ modules offers the possibility to boot the module using BIOS code programmed into an external firmware hub (FWH). The external FWH can be implemented on the carrier board. A hardware jumper must be provided on the carrier board to disable the module's onboard FWH and to enable the external FWH. The corresponding signal '*BIOS_DISABLE#*' can be found on pin 41 of the Qseven™ connector. Figure 3-28 shows a reference circuitry for an external 32-pin PLCC FWH socket.

Figure 3-28 LPC Firmware Hub Reference Circuitry



Note

Qseven™ modules based on the Intel® Atom™ Processor and Intel® System Controller Hub US15W can not be booted from external BIOS Firmware Hubs (FWH) that are clocked by a buffered or delayed clock signal.

3.15 Input Power

Qseven™ modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by Qseven™ to provide a +5V standby voltage on the Qseven™ module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. In this case the VCC_5V_SB pins must be connected to the +5V input power rail. The same applies to the +3V RTC battery voltage rail. If no RTC/CMOS backup functionality is required by the system during power-off, then the +3V RTC supply battery voltage can be omitted. During standby and power-on the RTC/CMOS

should be supplied by the 3.3V standby rail (see Figure 3-30).

For more information about the power input and ripple tolerances, as well as input power sequencing, refer to the Qseven™ Specification.

Table 3-29 Signal Definition Input Power

Signal	Pin#	Description	I/O
VCC	211 to 230	Power Supply +5VDC ±5%.	P
VCC_5V_SB	205, 206	Standby Power Supply +5VDC ±5%.	P
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P
GND	1, 2, 23, 24, 25, 26, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197, 198	Power Ground.	P

Note

If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then all pins must be connected together with the standard 5V power rail 'VCC'.

3.15.1 ATX Power Supply

ATX power supplies are widely used for consumer PC motherboards and they are also a cost effective and reliable solution for embedded designs. ATX power supplies provide all the necessary power rails required for a carrier board design. Table 3-30 and Table 3-31 describe the signals provided by the ATX power supply connectors.

3.15.1.1 ATX Power Connector

Table 3-30 ATX Connector

Signal	Pin	Description	Signal	Pin	Description
3.3V	1	+3.3V Power Supply	3.3V	13	+3.3V Power Supply
3.3V	2	+3.3V Power Supply	-12V	14	-12V Power Supply
COM	3	Ground	COM	15	Ground
5V	4	+5V Power Supply	PS_ON#	16	Active low signal, which is controlled by the Qseven™ module to turn on or off the ATX power supply.
COM	5	Ground	COM	17	Ground
5V	6	+5V Power Supply	COM	18	Ground
COM	7	Ground	COM	19	Ground
PWR_OK	8	Status signal generated by the ATX power supply to notify the Qseven™ module that the DC operating voltages are within the ranges required for proper operation.	Reserved	20	N.C.
5VSB	9	+5V Standby Voltage	+5V	21	+5V Power Supply
+12V	10	+12V Power Supply	+5V	22	+5V Power Supply
+12V	11	+12V Power Supply	+5V	23	+5V Power Supply
+3.3V	12	+3.3V Power Supply	COM	24	Ground

Note

The above table describes the pinout of a 24-pin ATX connector. When using a 20-pin ATX connector omit the following four pins: 11, 12, 23 and 24.

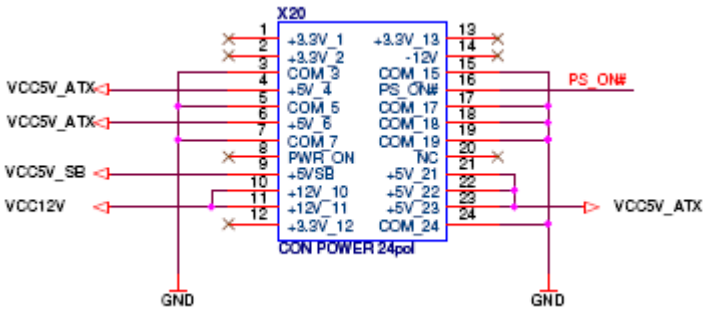
Table 3-31 +12V Power Connector

Signal	Pin	Description	Signal	Pin	Description
GND	1	Ground	GND	2	Ground
+12V	3	+12V Power Supply	+12V	4	+12V Power Supply

Note

For more information about the ATX Specification and the ATX12V Power Supply Specification refer to the Intel® 'ATX12V Power Supply Design Guide'. These documents can be found at the following website http://www.formfactors.org.

Figure 3-29 Schematics of ATX Power Connectors



3.15.2 RTC Battery

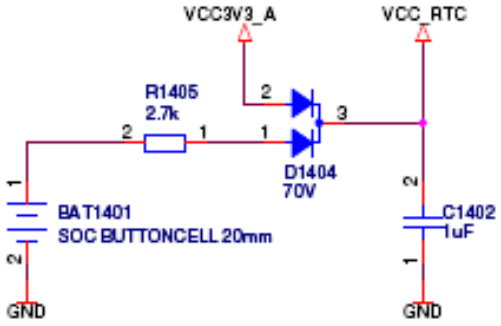
The Real Time Clock (RTC) is responsible for maintaining the time and date even when the Qseven™ module is not connected to a main power supply. Usually a +3V lithium battery cell is used to supply the internal RTC of the module. The Qseven™ specification defines an extra power pin *'VCC_RTC',* which connects the RTC of the module to the external battery. The specified input voltage range of the battery is defined between +2.4V and +3.3V. The signal *'VCC_RTC'* can be found on the module's connector pin 193.

3.15.2.1 RTC Battery Reference Circuitry

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series Schottky diode or a series resistor. The safest way, and the one recommended by the Qseven™ Consortium, is to implement a RTC battery circuitry using a Schottky diode (D1404) as shown in Figure 3-30.

This method offers protection against a possible explosion hazard as a result of reverse current flowing to the battery. Moreover, this implementation offers more flexibility when choosing battery type and manufacturer. Lithium batteries are the most common form of battery used in this scenario.

Figure 3-30 RTC Battery Circuitry with Serial Schottky Diode



Note

The Qseven™ Consortium recommends that a warning label be placed on or near the carrier board battery socket to indicate the appropriate manufacturer and model of battery that must be used to avoid creating an explosion hazard. This applies regardless of which RTC battery circuitry method has been implemented on the carrier board.

3.15.2.2 RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the carrier board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current it should be measured when the complete system is disconnected from AC power.

3.16 Power Control Signals

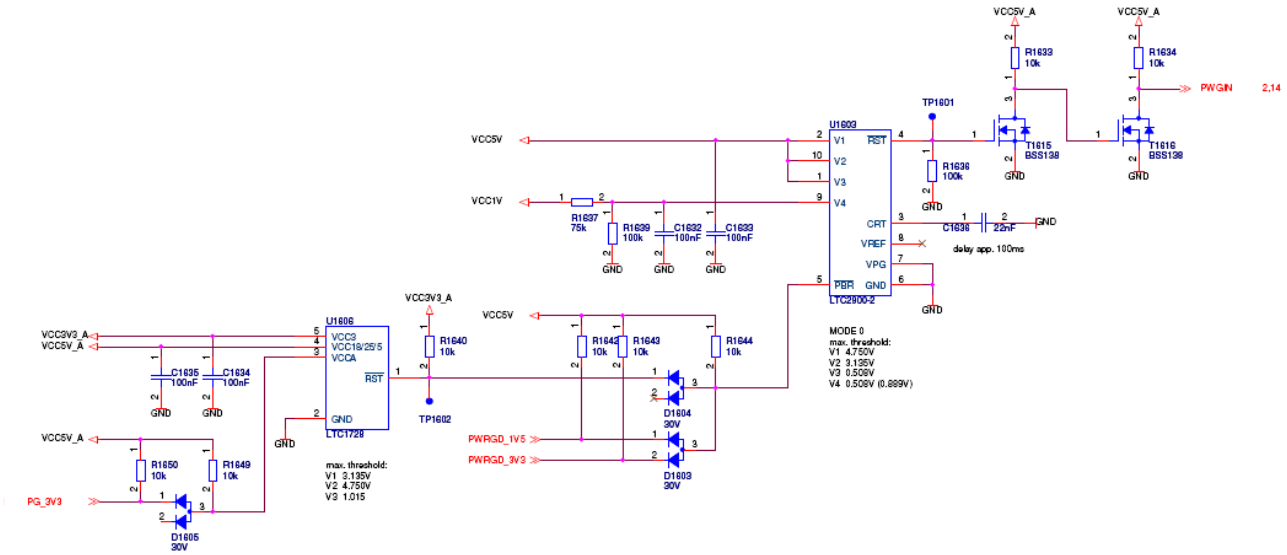
Table 3-32 Signal Definition Power Control

Signal	Pin#	Description of Power Control signals	I/O Type	I_{OL}/I_{IL}	I/O
PWGIN	26	High active input for the Qseven™ module indicates that power from the power supply is ready.	CMOS 5V	≥ 4 mA	I
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	CMOS OD 3.3V Standby	≥ 10 mA	I

3.16.1 Power Good Input Signal PWGIN

This signal is generated by the power supply circuitry and indicates that the operating voltages are within the ranges required for proper operation of the Qseven™ module and carrier board components. The voltage monitor used in the example shown in Figure 3-31 can monitor up to four voltages simultaneously. The voltage monitor LTC2900 from Linear Technologies (http://www.linear.com) has also been used on the Qseven™ evaluation carrier board.

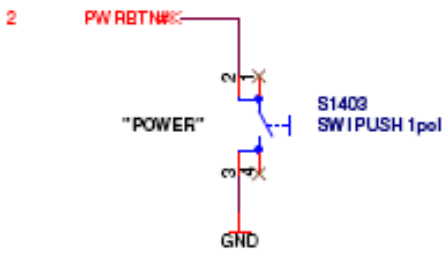
Figure 3-31 PWGIN Generation



3.16.2 Power Button Signal PWRBTN#

The power button signal is used to turn on the Qseven™ based system when using an ATX power supply or to wake up the system from ACPI power states S3 and S5.

Figure 3-32 Power Button Implementation Example



In a case where the system does not require a power button (system boots automatically when the power is supplied) the PS_ON# signal of the ATX power supply must be pulled to ground (see Figure 3-33 jumper J1603).

3.16.3 Power Up Control

The power up control is responsible for switching the ATX power supply on or off when a power-up or a power-down event occurs. A power event can be generated by pressing the power button or by another system event, which can originate from or be detected by the Qseven™ module's chipset.

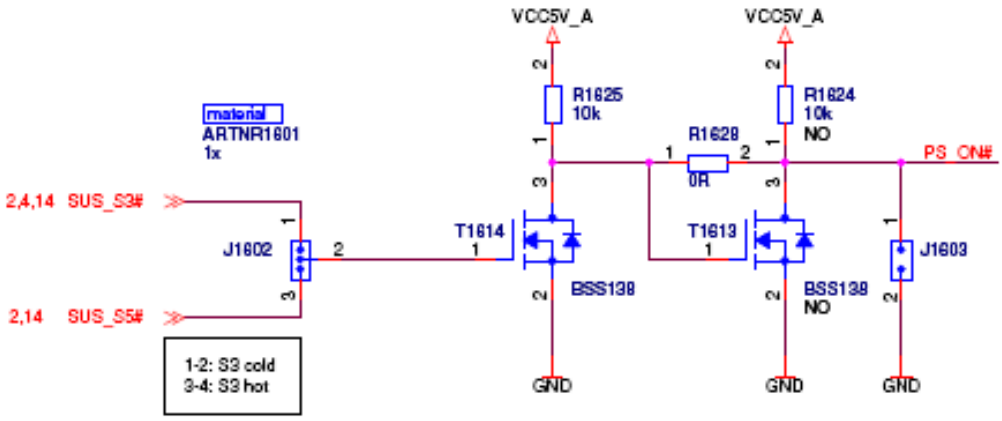
The native system power-up support of Qseven™ modules utilize the *'SUS_S3#'* signal to control the *'PS_ON#'* signal, which is used to switch the ATX power supply on or off. When using the *SUS_S3#'* signal, Qseven™ modules are capable of supporting Suspend to RAM (S3).

When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through the use of an inverter, the low active

'PS_ON#' signal goes high and switches off the ATX power supply. Vice versa, if the system resides in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the *'SUS_S3#'* signal. This results in a system transition to Full-On (S0).

The way Suspend to RAM is implemented on a Qseven™ module may differ depending on the module manufacturer. For this reason it is recommended that a hardware jumper be implemented on the carrier board in order to provide the ability to choose if the *'PS_ON#'* signal should be controlled either by the *'SUS_S3#'* signal or '*SUS_S5#'* signal.

Figure 3-33 Power Up Control Circuitry



When the Qseven™ based system uses an AT power supply (with no standby voltage present), the circuit shown in Figure 3-33 is not required. The Qseven™ module will automatically boot up after the AT power supply is switched on.

3.17 Power Management Signals

Qseven™ specifies a set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states from S0 to S5. The minimum hardware requirements for an ACPI compliant system is an ATX conforming power supply and a power button.

The following table provides a short description of the ACPI defined system states S0 to S5, including the corresponding power rail state. For more information about ACPI and the several system power states, refer to the 'Advanced Configuration and Power Interface Specification Revision 3.0'.

Table 5-36 System States S0-S5 Definitions

System State	Description	Power Rail State
S0 Full On	During S0 state, all components are powered and the system is fully functional.	Full power on all power rails.
S1 Power-on Standby (POS)	In S1 sleep state, no system context is lost, hardware maintains all system context. During S1 operation some system components are set into low power state.	Full power on all power rails.

System State	Description	Power Rail State
S2	Not supported.	
S3 Suspend to RAM (STR)	In S3 state, the current system state and context is stored in main memory and all unnecessary system logic is turned off.	Only main memory and logic required to wake-up the system remain powered by the standby voltages. All other power rails are switched off.
S4* Suspend to Disk (STD)	In S4 state the contents of the main memory are written to non-volatile storage such as a hard disk, as a file or on a separate partition, before powering off the computer.	See note below.
S5 Soft Off	In S5 state the system is switched off. Restart is only possible with the power button or by a system wake-up event such as 'Wake On LAN' or RTC alarm.	Standby power rails may or may not be powered, depending on if system wake-up is supported.

Note *

S4 (Suspend to Disk) might be not supported by all Qseven BIOSes (S4_BIOS) but it is supported by newer operating systems (S4_OS = Hibernate).

Table 3-33 Signal Definition Power Management

Signal	Pin#	Description of Power Management signals	I/O Type	I_{OL}/I_{IL}	I/O
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven™ module.	CMOS OD 3.3V	≥ 10 mA	I
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	CMOS OD 3.3V Suspend	≥ 10 mA	I
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	CMOS OD 3.3V Suspend	≥ 10 mA	I
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to RAM), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	CMOS 3.3V Suspend	max. 1 mA	O
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	CMOS OD 3.3V Suspend	≥ 10 mA	I
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. TBD: Open/Close state.	CMOS OD 3.3V Suspend	≥ 10 mA	I

Note

It must be guaranteed that all the carrier board power rails, that are generated out of the VCC power rail, will be enabled by the SUS_S3# signal.

3.18 I²C Bus

Due to the simple two-wire serial bus protocol and the high availability of devices, the I²C Bus is a frequently used low speed bus interface for connecting embedded devices such as sensors, converters or data storage. Qseven™ modules provide one I²C bus on the module's connectors.

Table 3-34 I²C bus Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
I2C_CLK	66	Clock line of I²C bus.	CMOS 3.3V OD		I/O
I2C_DAT	68	Data line of I²C bus.	CMOS 3.3V OD		I/O

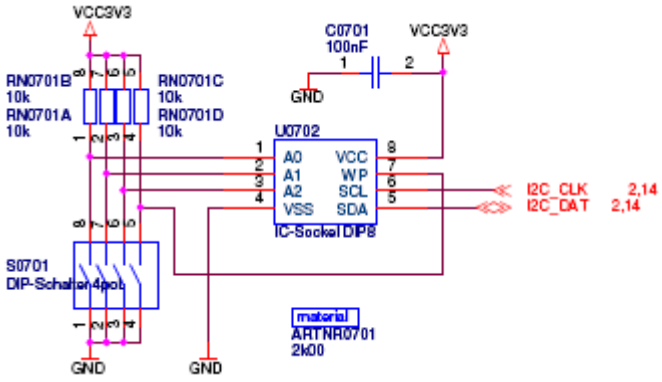
Note

The I²C Bus of the Qseven™ module can be accessed and programmed by using the API (Application Program Interface) called Embedded Application Software Interface (EASI). For more details about EASI, refer to the Qseven™ specification and the EASI Programmers Guide.

3.18.1 I²C Implementation Example

The example below shows the implementation of an an I²C EEPROM (DIP8 Socket) on the Qseven™ carrier board. In this example, the I²C address of the EEPROM can be set by a DIP switch.

Figure 3-34 I²C Implementation Example



3.19 Miscellaneous Signals

Table 3-35 Miscellaneous Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven™ module on the falling edge of a low active pulse.	CMOS OD 3.3V	≥ 10 mA	I
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	CMOS 3.3V	max. 5 mA	O
SMB_CLK	60	Clock line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_DAT	62	Data line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	CMOS 3.3V OD Suspend		I/O
SPKR	194	Output for audio enunciator, the “speaker” in PC AT systems	CMOS 3.3V		O
BIOS_DISABLE#	41	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations.	CMOS 3.3V		I
MFG_NC0 MFG_NC1 MFG_NC2 MFG_NC3	207, 209, 208, 210	Do not connect on the carrier board. These pins are reserved for manufacturing purposes.	n.a.	n.a.	NC
RSVD	56, 124, 129, 130, 199, 200, 201, 202, 203	Reserved. Do not connect.	n.a.	n.a.	NC

3.19.1 Watchdog Control Signals

The Watchdog on Qseven™ modules can be initialized and controlled by the API (Application Program Interface) called Embedded Application Software Interface (EASI). For more details about EASI, refer to the Qseven™ specification and the EASI Programmers Guide.

In addition to the software trigger available via EASI, the Watchdog on a Qseven™ module can be hardware-triggered by an external control circuitry. When generating a low level pulse on the Qseven™ module's *'WDTRIG#'* (Watchdog trigger signal) signal, the Watchdog timer will be reset and restarted.

If the Watchdog timer has expired without a software or hardware trigger occurrence, the Qseven™ module will signal this with a high level output on the *'WDOUT'* (Watchdog event indicator) signal.

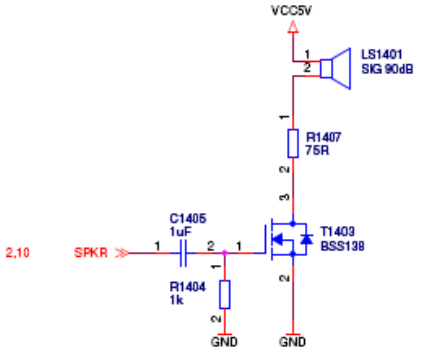
3.19.2 PC Speaker Output

The Qseven™ module provides a speaker output signal called *'SPKR',* which is intended to drive an external FET or a logic gate to connect a PC speaker. The *'SPKR'* signal can be found on the module's pin 194.

The *'SPKR'* signal is often used as a configuration strap for the module's chipset. It should not be connected to a pull-up or pull-down resistor, which could overwrite the internal chipset configuration and result in a malfunction of the module.

The following reference schematics illustrates a circuitry for an active piezoelectric speaker 'HY-05' from HYCOM (http://www.hycomdevice.com.tw).

Figure 3-35 PC Speaker Implementation Example



3.19.3 External Firmware Hub Enable Signal BIOS_DISABLE

Refer to section 3.14.4 of this document for more information about this signal.

3.20 Thermal Management Signals

Qseven™ modules provide the *'THRM#'* and *'THRMTRIP#'* signals, which are used for system thermal management. In most current system platforms, thermal management is closely associated with system power management. For more detailed information about the thermal management capabilities of the Qseven™ module refer to the module's user's guide.

Table 3-36 Signal Definition Thermal Management

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	CMOS 3.3V		I
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	CMOS 3.3V OD		O

3.21 Fan Control Implementation

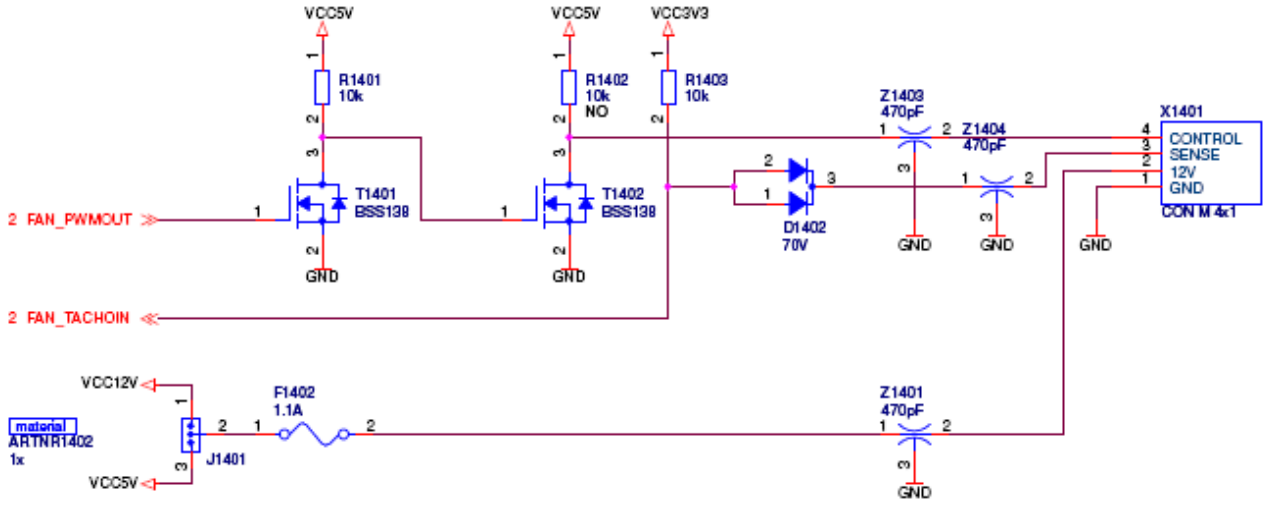
Qseven™ modules provide additional support for fan speed control through the use of two signals named *'FAN_TACHOIN'* and *'FAN_PWMOUT'.* In order to easily implement fan speed control in customer specific application software, an API will be available. This API supports most of the current operating systems available. For more information about this subject refer to the software section of this document.

Table 3-37 Signal Definition Fan Control

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
FAN_PWMOUT	196	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature.	CMOS 3.3V OC		O
FAN_TACHOIN	195	Fan tachometer input.	CMOS 3.3V		I

3.21.1 Fan Control Reference Schematics

Figure 3-36 Fan speed control circuitry



4 Layout and Design Constraints

This chapter provides routing guidelines for layout and design of a printed circuit board using high-speed interfaces such as PCI Express, Serial ATA, LVDS, Gigabit Ethernet and USB 2.0. The signal integrity rules for high-speed interfaces need to be considered. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity and quality.

Keep in mind that this document can only highlight the most important issues that should be considered when designing an Qseven™ carrier board. The designer has to take into account the corresponding information (specification, design guidelines, etc.) contained in the documentation for each interface that is to be implemented on their carrier board.

Note

For more information about PCB design considerations we recommend you refer to the book "PCI Express Electrical Interconnect Design" available from Intel (http://www.intel.com/intelpress/) ISBN 0-9743649-9-1.

4.1 Microstrip or Stripline

Either edge-coupled microstrip, edge-coupled stripline, or broad-side striplines are recommended for designs with differential signals.

Designs with microstrip lines offer the advantage that a lower number of layers can be used. Also, with microstrip lines it may be possible to route from a connector pad to the device pad without any via. This provides better signal quality on the signal path that connects devices. A limitation of microstrip lines is that they can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

Stripline may be either edge-coupled or broad-side coupled lines. Stripline designs provide additional shielding since they are embedded in the board stack and are typically sandwiched between ground and power planes. This reduces radiation and coupling of noise onto the lines. Striplines have the disadvantage that they require the use of vias to connect to them.

4.2 Printed Circuit Board Stackup Example

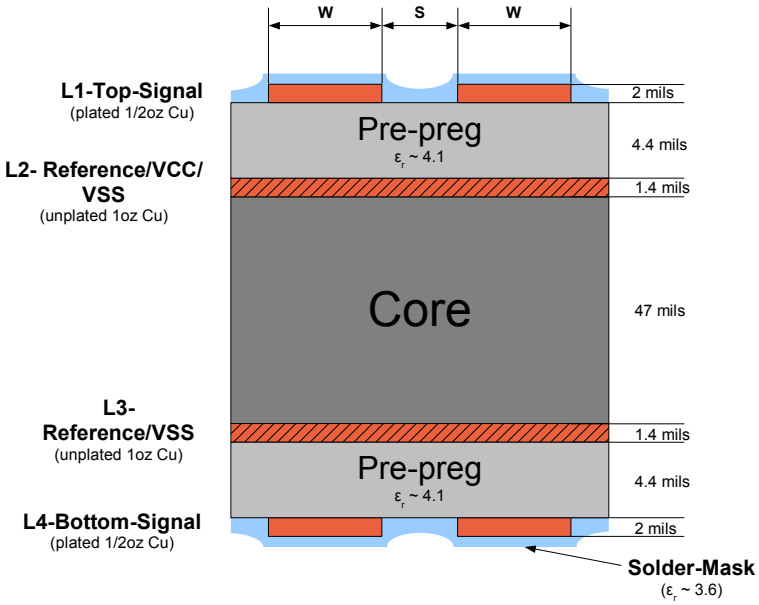
It is recommended to use PCBs with at least a 4 layer stackup where the impedance controlled layer 1 (top layer) is used for differential signals and layer 4 (bottom layer) for other periodic signals (CMOS/TTL). The dedicated power planes (layer 2 - GND and layer 3 - VCC) are typically required for high-speed designs. The solid ground plane is necessary to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground planes will additionally create an excellent high frequency bypass capacitance.

The example in Figure 4-1 shows a four layer PCB stackup using microstrip trace routing.

A good rule to follow for microstrip designs is to keep S < W and S < H ("H" = space between differential signal layers and the reference plane). The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W,"

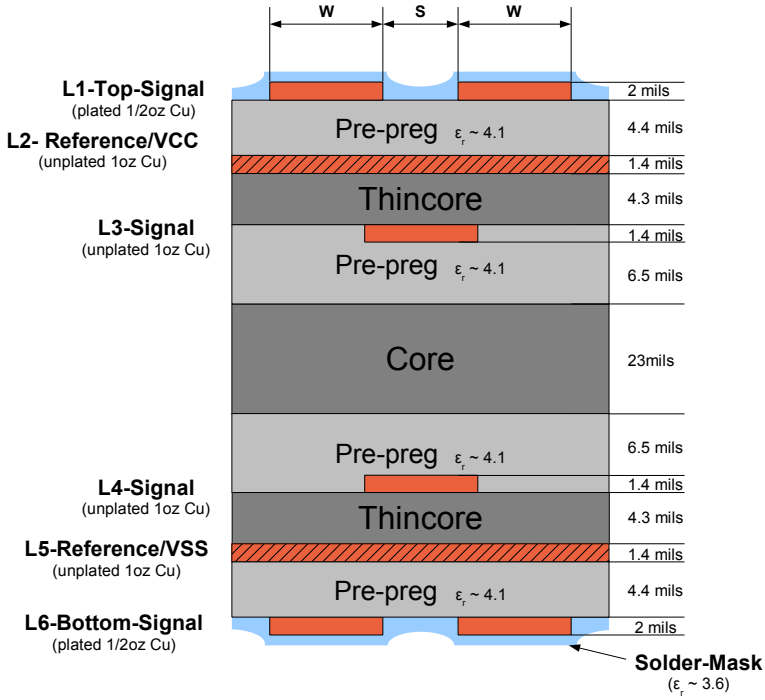
to control differential impedance.

Figure 4-1 4 Layer PCB Microstrip Routing



For stripline routing, a PCB stackup of at least 6 layers is necessary. The internal layers (L3 and L4) can be used for routing differential signals as stripline traces while the outer layers (L1 and L6) can be used for microstrip routing.

Figure 4-2 6 Layer PCB Stripline and Microstrip Routing

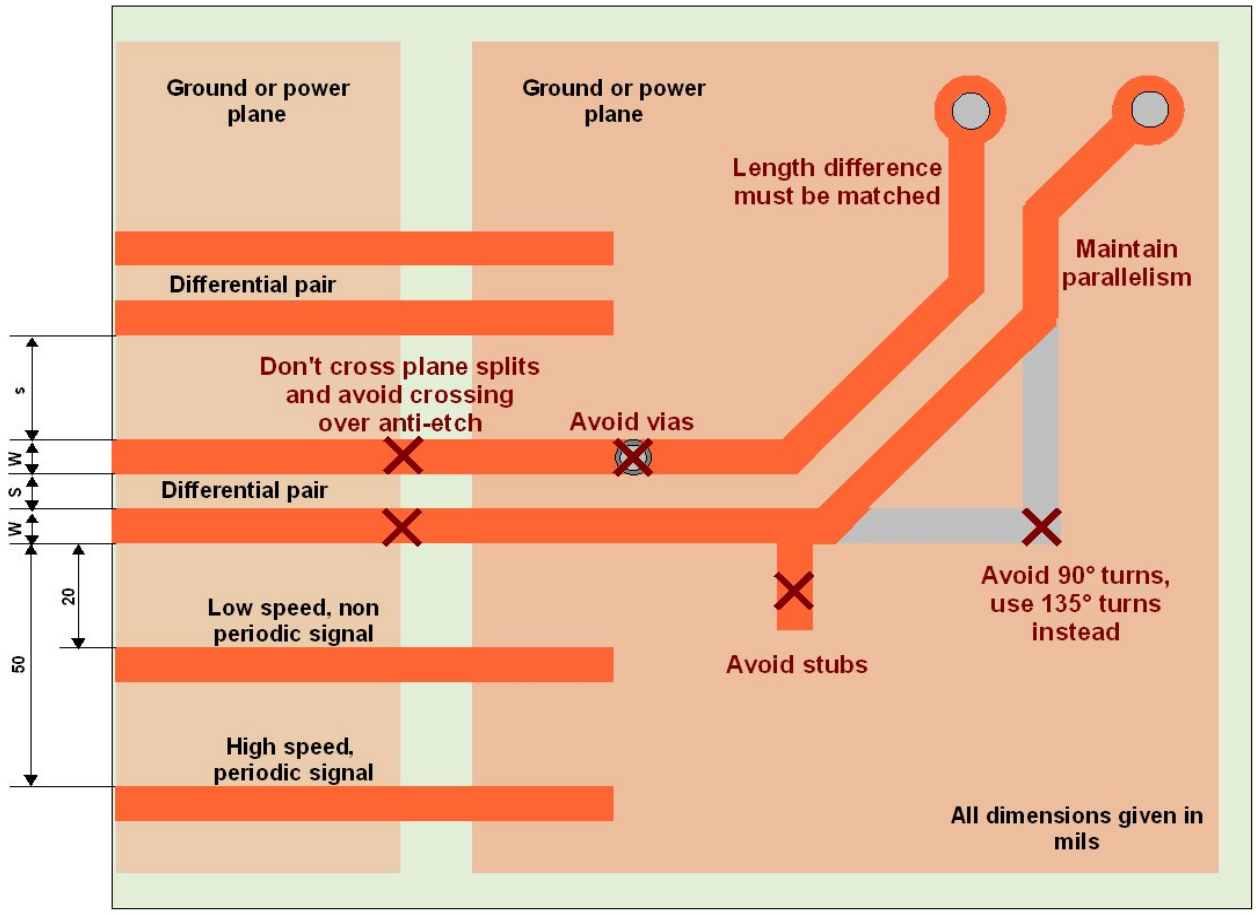


4.3 General Considerations for High-Speed Differential Interfaces

The following is a list of suggestions for designing with high-speed differential signals. This should help implement these interfaces while providing maximum Qseven™ carrier board performance.

- Use controlled impedance PCB traces that match the specified differential impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing needed to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs and any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- It is best to put CMOS/TTL and differential signals on a different layer(s), which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate, clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.
- Use a minimum of 20mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.

Figure 4-3 Layout Considerations



Note

In order to determine the necessary trace width, trace height and spacing needed to fulfill the requirements of the interface specification, it's necessary to use an impedance calculator.

4.4 PCI Express Trace Routing Guidelines

Table 4-1 PCI Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate / PCIe Lane	2.5 Gbits/sec
Signal length allowance on the Qseven™ carrier board	TX path: 14.5 inches to PCIe device 7.7 inches to PCIe slot RX path: 15.7 inches to PCIe device 7.7 inches to PCIe slot Valid for a damping value of the PCB trace of 0.35dB/inch @ 1,25GHz (common value for FR-4 based material)
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 4 vias per TX trace Max. 2 vias per RX trace
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the Qseven™ module. The AC coupling capacitors for RX signal lines have to be implemented on the customer Qseven™ carrier board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

4.5 USB Trace Routing Guidelines

Table 4-2 USB Trace Routing Guidelines

Parameter	Trace Routing
Transfer rate / Port	480 Mbit/s
Signal length allowance for the Qseven™ carrier board	14.0 inches Valid for a damping value of the PCB trace of 0.11dB/inch @ 0.4GHz (common value for FR-4 based material)
Differential Impedance	90 Ohms +/-15%
Single-ended Impedance	45 Ohms +/-10%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	6mils (microstrip routing) (*)
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils
Reference plain	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

4.6 SDVO Trace Routing Guidelines

Table 4-3 SDVO Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate / SDVO Lane	Up to 2.0 Gbits/sec
Signal length allowance for the Qseven™ carrier board	TBD
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7 mils (microstrip routing) (*)
Spacing between pairs-to-pair	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between differential pairs (inter-pair)	Keep difference within a 2.0 inch delta.
Length matching between differential signal pair and differential clock pair	Max. 5mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 4 vias per differential signal trace
AC coupling capacitors	AC Coupling capacitors on the signals *'SDVO_INT+'* and *'SDVOINT-'* have to be implemented on the customer Qseven™ carrier board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

4.7 LAN Trace Routing Guidelines

Table 4-4 LAN Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	1.0 Gbits/sec
Signal length allowance for the Qseven™ carrier board	4.0 inches to the magnetics module Valid for a damping value of the PCB trace of 0.03dB/inch @ 0.1GHz (common value for FR-4 based material)
Maximum signal length between isolation magnetics module and RJ45 connector on the carrier board	1.0 inch
Differential Impedance	95 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics module and RJ45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

4.8 Serial ATA Trace Routing Guidelines

Table 4-5 Serial ATA Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	3.0 Gbits/sec
Maximum signal line length (coupled traces)	7.0 inches (Qseven™ module and carrier board). The length of the SATA cable is specified between 0 and 40 inches
Signal length used on Qseven™ module (including the Qseven™ carrier board connector)	2.5 inches
Signal length available for the Qseven™ carrier board	4.5 inches Valid for a damping value of the PCB trace of 0.42dB/inch @ 1,5GHz (common value for FR-4 based material)
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency. Do not serpentine to meet trace length guidelines for the RX and TX path.
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the Qseven™ module.

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

4.9 LVDS Trace Routing Guidelines

Table 4-6 LVDS Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	5.38 Gbits/sec
Signal length to the LVDS connector available for the Qseven™ carrier board	TBD
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	4mils (microstrip routing) (*)
Spacing between differential pair signals (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between pair to pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	+/- 20mils
Length matching between clock and data pairs (inter-pair)	+/- 20mils
Length matching between data pairs (inter-pair)	+/- 40mils
Spacing from edge of plane	+/- 40mils
Reference plain	GND referenced preferred
Via Usage	Max. of 2 vias per line

Note

(*) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB, it's necessary to use a suitable impedance calculator.

5 Industry Specifications

The list below provides links to industry specifications used to define the Qseven™ interface specification.

Table 5-1 Industry Specifications

Specification	Description	Link
1000BASE T	IEEE standard 802.3ab 1000BASE T Ethernet	www.ieee.org/portal/site
ACPI	Advanced Configuration and Power Interface Specification Rev. 3.0a	www.acpi.info
DisplayID	Display Identification Data (DisplayID) Structure, Version 1.0	www.vesa.org
DisplayPort	DisplayPort Standard - Version 1.1a	www.vesa.org
DVI	Digital Visual Interface, Rev 1.0, April 2, 1999, Digital Display Working Group	www.ddwg.org
ExpressCard	ExpressCard Standard Release 1.0	www.expresscard.org
HDA	High Definition Audio Specification, Rev. 1.0	www.intel.com/standards/hdaudio
I2C	The I2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1	www.semiconductors.philips.com
IEEE 802.3-2002	IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications	www.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.0 (LPC)	developer.intel.com/design/chipsets/industry/lpc.htm
LVDS	Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor	www.national.com
LVDS	LVDS Owner's Manual	www.national.com
LVDS	ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001.	www.ansi.org
PCI Express	PCI Express Base Specification, Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group.	www.pcisig.com
PCI Express	PCI Express Base Specification, Revision 1.1 PCI Express Card Electromechanical Specification, Revision 1.1	www.pcisig.com/specifications
SATA	Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved	www.sata-io.org
SATA	Serial ATA Specification, Revision 1.0a	www.serialata.org
SDVO	SDVO (Serial Digital Video Out) is a proprietary Intel technology introduced with their 9xx-series of chipsets.	en.wikipedia.org/wiki/SDVO
Smart Battery	Smart Battery Data Specification, Revision 1.1, December 11, 1998	www.sbs-forum.org
SMBUS	System Management Bus (SMBUS) Specification, Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc.	www.smbus.org
USB	Universal Serial Bus (USB) Specification, Revision 2.0	www.usb.org/home