TMDXEVM6614LXE EVM

Technical Reference Manual

Version 1.0

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ADVANTECH

Texas Instruments

EVALUATION BOARD / KIT / MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all, or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

Your Obligations and Responsibilities

Please consult the EVM documentation, including but not limited to any user guides, setup guides or getting started guides, and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of, or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Warning

The EVM board may get very hot during use. Specifically, the heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

Preface

About this Document

This document is a Technical Reference Manual for the TMS320TCI6614 Evaluation Module (TMDXEVM6614LXE) designed and developed by Advantech Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono spaced font. Examples use bold for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

Release	Chapter	Description of Change
1.0	All	The first release for Alhpa 1 and Alhpa 2 EVMs

Acronyms

Acronym	Description
AMC or *Advanced*MC	Advanced Mezzanine Card
AIF2	Antenna Interface 2
CCS	Code Composer Studio
DDR3	Double Data Rate 3 Interface
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
FPGA	Field Programmable Gate Array
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MCH	MicroTCA Carrier Hub
MTCA or *Micro*TCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PICMG®	PCI Industrial Computer Manufacturers Group
RFU	Reserved for Future Use
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XDS560v2	Texas Instruments' System Trace Emulator
USIM	Universal Subscriber Identity Module
SFP	SMALL FORM PLUGGABLE

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1. Overview

This chapter provides an overview of the TMDXEVM6614LXE along with the key features and block diagram.

1.1 Key Features

The TMDXEVM6614LXE is a high-performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments TMS320TCI6614 Communications Infrastructure KeyStone SoC. The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320TCI6614 SoC.

Schematics, code examples, and application notes are available to ease the hardware development process and to reduce the time to market.

The key features of the TMDXEVM6614LXE EVM are:

- Texas Instruments Communications Infrastructure KeyStone SoC– TMS320TCI6614
- 1G bytes of DDR3-1600 memory
- 128M bytes of NAND Flash
- 4M bytes of SPI NOR FLASH
- Two Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – one on AMC connector and one RJ-45 connector
- 170-pin B+ style AMC interface
- On board GPS module – TC6000G
- One SMA connector for external GPS antenna
- High Performance connector for the HyperLink interface
- One SFP connector with 4 ports of AIF
- One USIM connector
- 128K-byte I2C EEPROM
- 2 User LEDs, one LED for system power good indicator, 21 sliding DIP switches and 4

Software-controlled LEDs

- RS232 Serial interface on 3-pin header
- Timer, SPI, GPIO, EMIF16, I2C and UART signals on the 100-pin expansion header
- TI 60-Pin JTAG header to support all external emulator types
- XDS560v2 System Trace Emulation Mezzanine Card
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12 V/3.0 A) or AMC carrier backplane

1.2 Functional Overview

The TMS320TCI6614 Communications Infrastructure KeyStone SoC is a member of the C66xx SoC family based on TI's new KeyStone Multicore SoC Architecture designed specifically for high performance wireless infrastructure applications. The TCI6614 provides a very high performance Pico/Micro basestation platform for developing all wireless standards including WCDMA/HSPA/HSPA+, TD-SCDMA, GSM, TDD-LTE, FDD-LTE, and WiMAX. Even with aggregate data rates for 20-MHz LTE systems above 400 Mbps per sector, the TCI6614 can support two sectors running at full rate. The TCI6614 also sets a new standard for clock speed with operating frequencies up to 1.2GHz.

The TCI6614 supports a high performance dual mode of operation for simultaneous support of WCDMA and LTE. There is also capability of supporting advanced algorithms such as Turbo SIC/PIC, IRC, 2 × 4 MIMO, and 4 × 4 MIMO

TI's SoC architecture provides a programmable platform integrating various subsystems (C66x cores, IP network, radio layers 1 and 2, and transport processing) and uses a queue-based communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet Switch that enables the wide mix of system elements, from programmable cores to dedicated coprocessors and high speed IO, to each operate at maximum efficiency with no blocking or stalling.

The addition of the ARM Cortex-A8 microprocessor in the TCI6614 enables the ability for layer 3 processing on-chip. Operations such as Traffic Control, Local O&M, NBAP, and SCTP processing can all be performed with the ARM Cortex-A8.

The functional block diagram of TMDXEVM6614LXE is shown in the figure below:

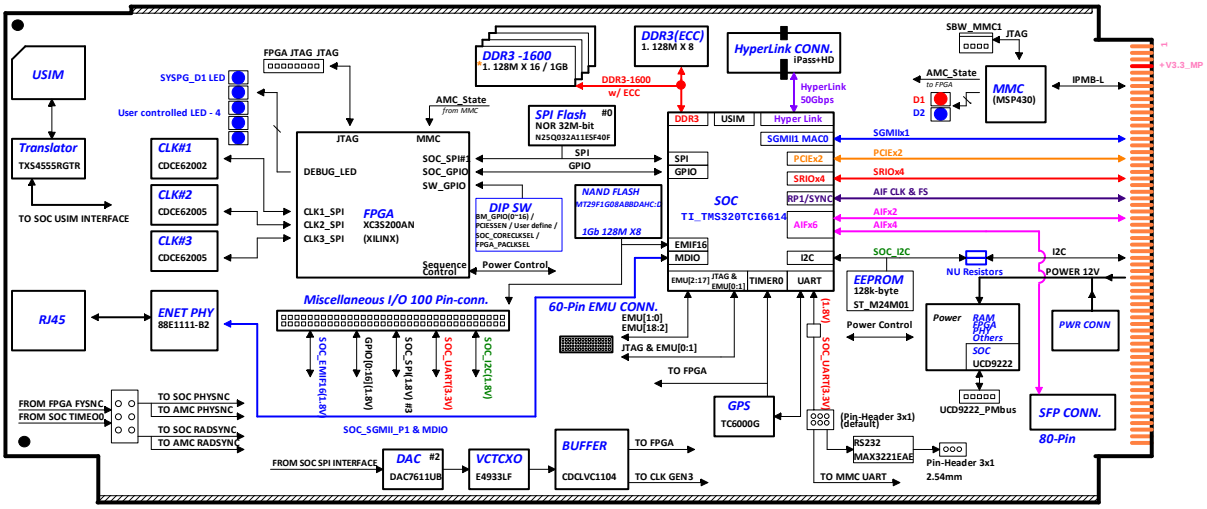


Figure 1.1: Block Diagram of TMDXEVM6614LXE EVM

1.3 Basic Operation

The TMDXEVM6614LXE platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interface with the board through the XDS560v2 mezzanine emulator attached on the EVM.

The EVM comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. The MCSDK also includes an out-of-box demonstration; see the "MCSDK Getting Started Guide".

To start operating the board, follow instructions in the Quick Start Guide. This guide provides instruction for proper connections and configuration for running the POST and OOB Demos. After completing the POST and OOB Demos, proceed with installing CCS and the EVM support files by following the instructions on the DVD. This process will install all the necessary development tools, drivers and documentation.

After the installation has completed, follow the steps below to run Code Composer Studio.

1. Power-on the board using the power brick adaptor (12 V/3.0 A) supplied with this EVM or insert this EVM board into AMC carrier backplane without the chassis.

2. Connect the USB cable from host PC to the XDS560v2 Mezzanine Card on EVM board.

3. Launch Code Composer Studio from the host PC by double clicking on its icon on the PC desktop.

Detailed information about the EVM including examples and reference materials are available in the DVD included with this EVM kit.

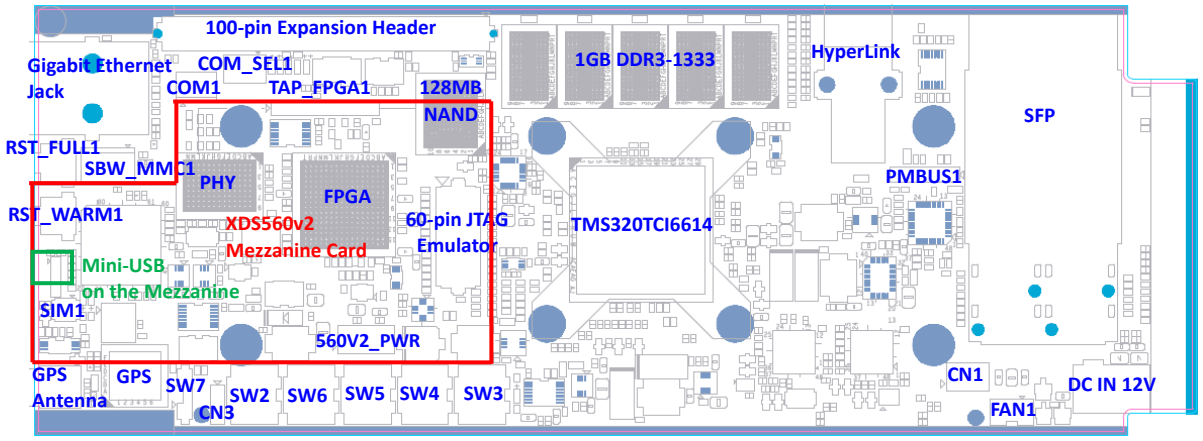


Figure 1.2: TMDXEVM6614LXE EVM Layout

1.4 Boot Mode and Boot Configuration Switch Setting

The TMDXEVM6614LXE has 21 sliding DIP switches (Board Ref. SW2 to SW6) to determine boot mode, boot configuration, device number, endian mode, PLL clock selection, and PCIe Mode selection options at the POR stage of the SoC.

1.5 Power Supply

The TMDXEVM6614LXE can be powered from a single +12V / 3.0A DC (36W) external power supply connected to the DC power jack (DC_IN1). Internally, +12-V input is converted into required voltage levels using local DC-DC converters.

- CVDD (+0.70 V~+1.10 V) is used for the SoC core logic
- +1.0 V is used for internal memory and HyperLink / SRIO / SGMII / PCIe / AIF2 termination of SoC
- +1.5 V is used for DDR3 of SoC, Supplying HyperLink / SRIO / SGMII / PCIe / AIF2 regulators in SoC and RAM chips
- +1.8 V is used for the SoC PLLs, SoC LVCMOS I/Os, FPGA I/Os driving the SoC and GPS module
- +2.5 V is used for the Gigabit Ethernet PHY core
- +1.2 V is used for FPGA core and Gigabit Ethernet PHY core
- +3.3 V is used for the FPGA I/Os
- +5 V and +3.3 V is used to power the XDS560v2 mezzanine card
- The DC power jack connector is a 2.5mm barrel-type plug with positive polarity on the center tip

The TMDXEVM6614LXE can also draw power from the AMC edge connector (AMC1). If the board is inserted into an AMC carrier backplane which can provide 12V power to the EVM, the external +12V supply from DC jack (DC-IN1) isn't required.

2. Introduction to the TMDXEVM6614LXE board

This chapter provides an introduction and details of interfaces for the TMDXEVM6614LXE board. It contains:

2.1 Memory Map

For the memory map of the TMS320TCI6614 device, please refer to the TMS320TCI6614 Data manual.

2.2 EVM Boot Mode and Boot Configuration Switch Settings

The TMDXEVM6614LXE has five configuration switches: SW2, SW3, SW4, SW5, and SW6 that contain 17 individual values latched when reset is released. This occurs when power is applied on the board, after the user presses the FULL_RESET push button or after a POR reset is requested from the MMC.

These configuration switches determines the boot master (CorePac or ARM), general configuration, Little or Big Endian mode, boot device selection and boot device configuration.

More information about using these DIP switches is contained in Section 3.3 of this document. For more information on TMS320TCI6614 supported Boot Modes, please refer to TMS320TCI6614 Data Manual and C66x Bootloader User Guide.

2.3 JTAG - Emulation Overview

The TMDXEVM6614LXE uses the XDS560v2 mezzanine on the 60-pin JTAG header to connect the EVM with Code Composer Studio. Users can connect CCS with the target SoC in the EVM through the TI 60-pin JTAG header (EMU1) on the EVM.

The TI 60-pin JTAG header (EMU1) is provided for high speed real-time emulation. The TI 60-pin JTAG supports all standard TI system trace emulators. An adapter will be required for use with some emulators.

The second way of accessing the SoC is through the JTAG port on the AMC edge connector, users can connect the SoC through the AMC backplane if they don't use the 60-pin header with the XDS560v2 mezzanine. If the XDS560v2 mezzanine plug into the 60-pin header, the board circuitry automatically to give emulation control to the XDS560v2 mezzanine and disconnect the path from AMC edge connector to TMSTCI6614.

The JTAG interface among the TMS320TCI6614, external emulator and the AMC edge connector is shown in the below figure:

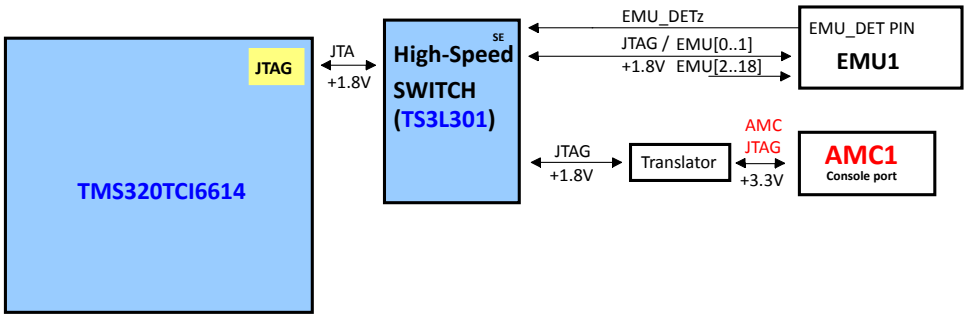


Figure 2.1: TMDXEVM6614LXE EVM JTAG emulation

2.4 Clock Domains

The EVM incorporates a variety of clocks to the TMS320TCI6614 as well as other devices that are configured automatically during the power up configuration sequence. The figure below illustrates clocking for the system in the EVM module.

The EVM supports external clock references. This is needed for some applications using the AIF and HyperLink SERDES interfaces. The external reference clock is driven into the clock generation device rather than using the local crystal. For AIF, a common 30.72MHz timing source is needed for the clock generator, CLK3, that drives the CORE_CLK and SYS_CLK inputs. It is supplied on the AMC connector at the TCLKD input. For HyperLink, a common 25MHz timing source is needed for the clock generator, CLK2, that drives the MCM_CLK input. It is supplied on the AMC connector at the TCLKB input.

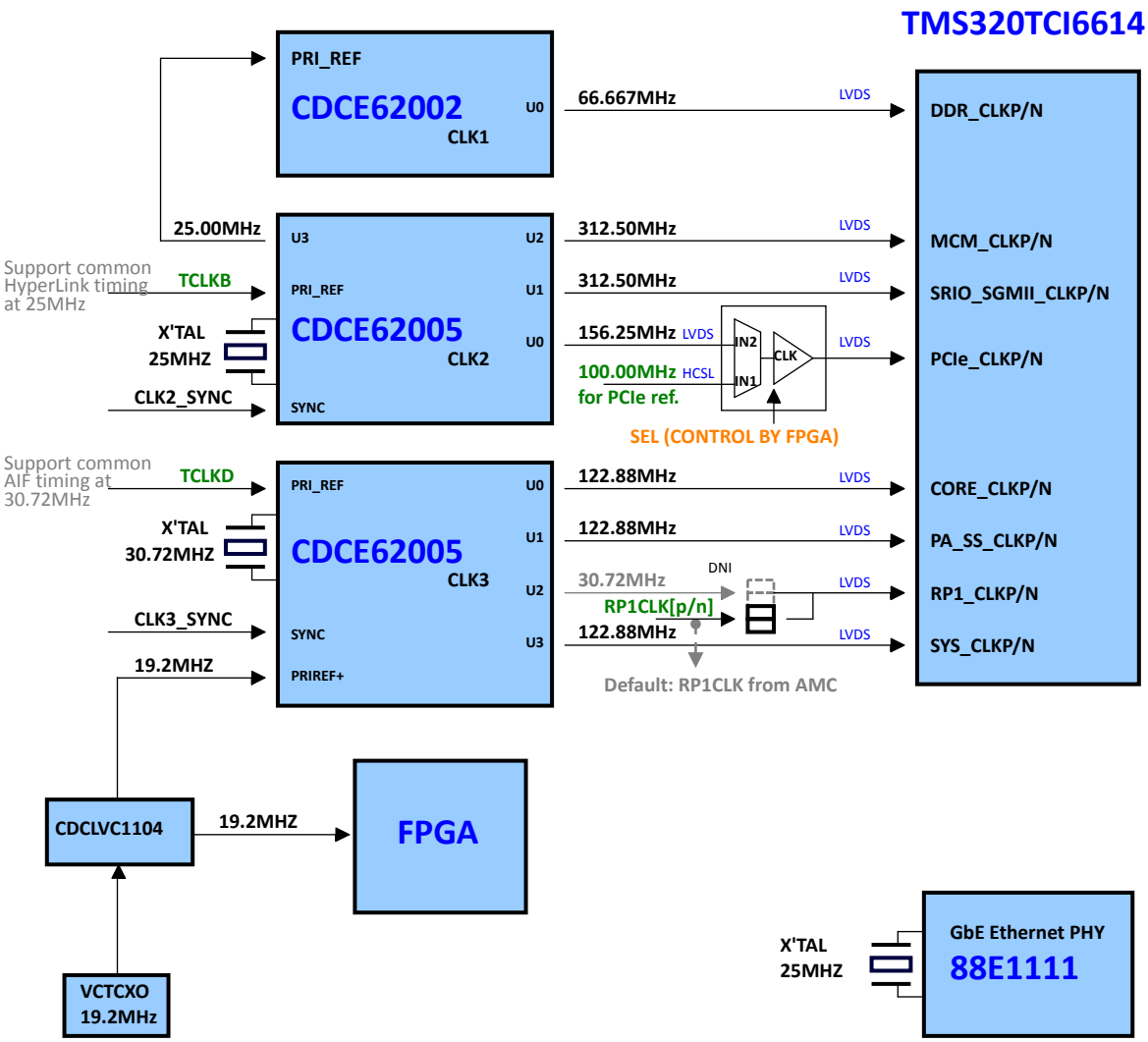


Figure 2.2: TMDXEVM6614LXE EVM Clock Domains

2.5 Non-Volatile Memories (SEEPROM / SPI NOR Flash / NAND flash)

The I2C modules on the SoC may be used to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one SEEPROM and to the 100-pin expansion header (TEST_PH1). There are two banks in the I2C SEEPROM which respond separately at addresses 0x50 and 0x51. These banks can be loaded with demonstration programs. Currently, the bank at 0x50 contains the I2C boot code and PLL initialization procedure and the bank at 0x51 contains the second level boot-loader program. The second level boot-loader can be used to run the POST program or launch the OOB demonstration from NOR flash memory.

The Serial Peripheral Pnterconnect (SPI) module provides an interface between the SoC and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on SoC is supported only in Master mode.

The NOR FLASH attached to CS0z on the SoC is a NUMONYX N25Q032A11ESE40F. This NOR FLASH size is 4 M bytes. It can contain demonstration programs such as POST or the OOB demonstration. The CS1z of the SPI is used by the SoC to access registers within the FPGA. The CS2z of the SPI is used for setting the DAC1, DAC7611. The CS3z of the SPI is routed to 100-pin header.

The TMS320tci6614 EMIF16 bus contains a 128Mbyte NAND flash device, Micron MT29F1G08ABBDAHC, to be the storage for a linux kernel.

2.6 FPGA Functions

The FPGA (Xilinx XC3S200AN) controls the reset mechanism of the SoC and provides boot mode and boot configuration data to the SoC through SW2, SW3, SW4, SW5, and SW6. The FPGA also provides the transformation of TCLK[A:D] from AMC connector for the Timer of the SoC, user LEDs control, and one user switch through control registers. All FPGA registers are accessible over the SPI interface.

The figure below shows the interface between TMS320TCI6614 SoC and FPGA.

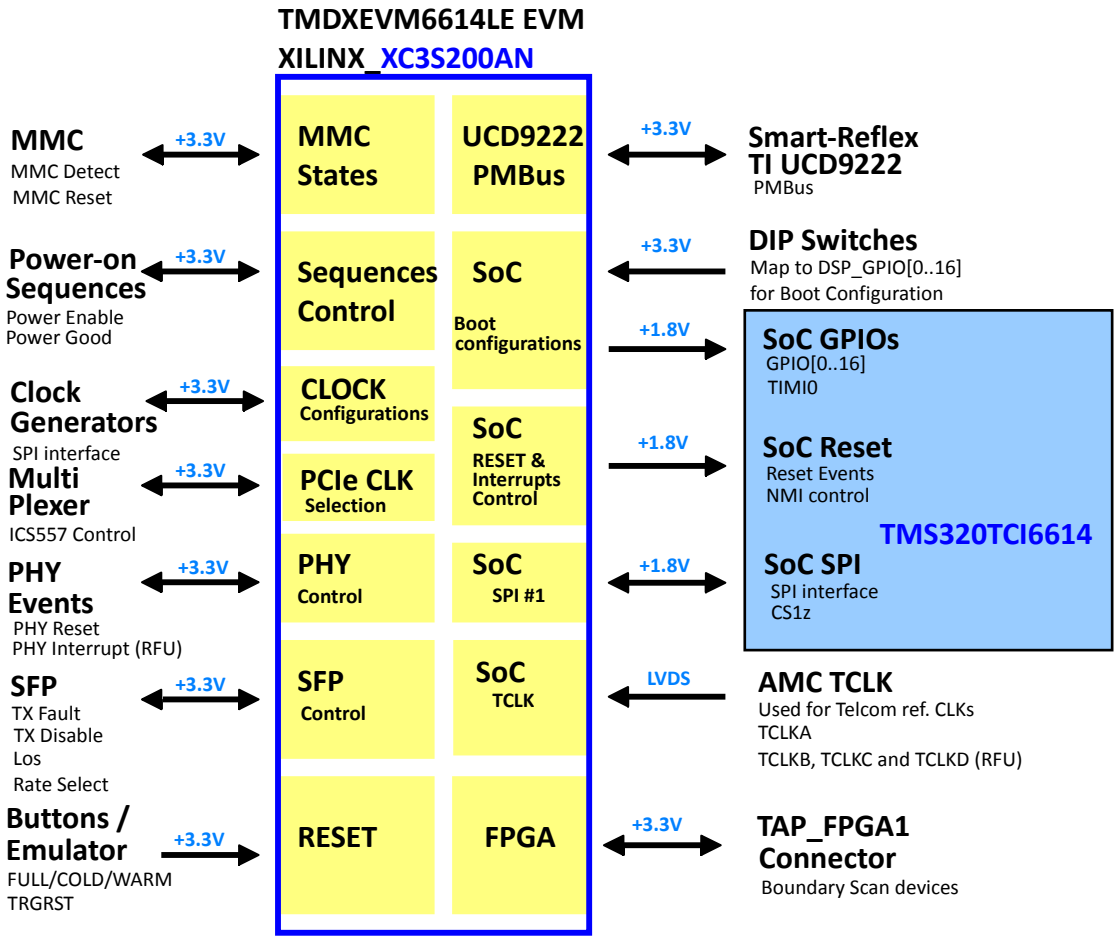


Figure 2.3: TMDXEVM6614LXE EVM FPGA Connections

2.7 Gigabit Ethernet Connections

The TMDXEVM6614LXE provides connectivity for both SGMII Gigabit Ethernet ports on the EVM. These are shown in figure below:

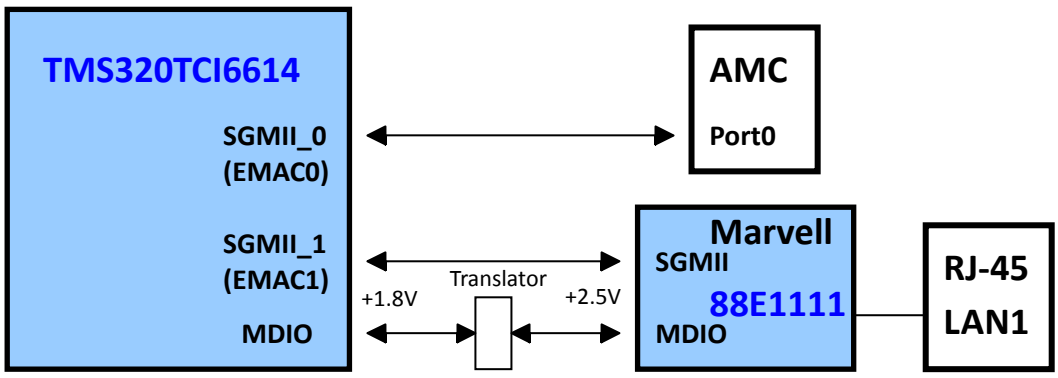


Figure 2.4: TMDXEVM6614LXE EVM Ethernet Routing

The Ethernet PHY (PHY1) is connected to SoC EMAC1 to provide a copper interface and routed to a Gigabit RJ-45 connector (LAN1). The EMAC0 of SoC is routed to Port0 of the AMC edge connector backplane interface.

2.8 Serial RapidIO (SRIO) Interface

The TMDXEVM6614LXE supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total 4 RapidIO ports available on TMS320TCI6614. All SRIO ports are routed to AMC edge connector on board. Below figure shows RapidIO connections between the SoC and AMC edge connector.

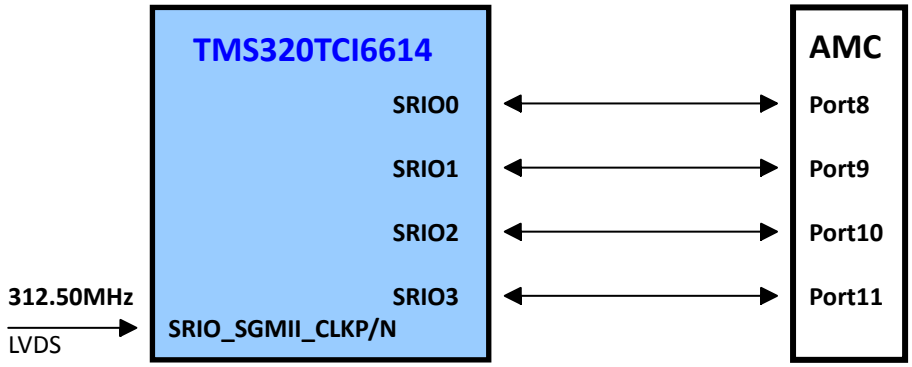


Figure 2.5: TMDXEVM6614LXE EVM SRIO Port Connections

2.9 DDR3 External Memory Interface

The TMS320TCI6614 DDR3 interface connects to four 2Gbit (128Mega x 16) DDR3 1600 devices. This configuration allows the use of both “narrow (16-bit)”, “normal (32-bit)”, and “wide (64-bit)” modes of the DDR3 EMIF.

SAMSUNG DDR3 SDRAMs (128Mx16-bit; 1600MT/s) are used on the DDR3 EMIF.

Below figure illustrates the implementation for the DDR3 SDRAM memory.

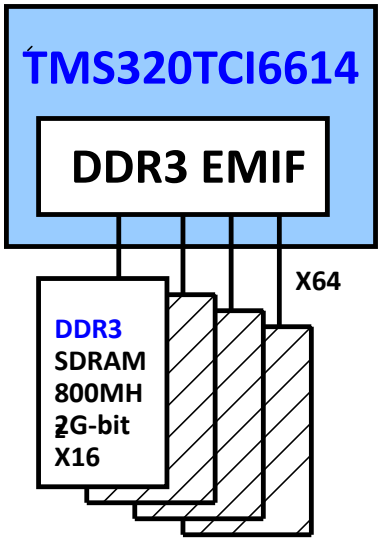


Figure 2.6: TMDXEVM6614LXE EVM SDRAM

2.10 HyperLink interface

The TMS320TCI6614 provides the HyperLink bus for companion chip/die interfaces. This is a four-lane SerDes interface designed to operate at 12.5 Gbps per lane. The interface is used to connect with external accelerators.

The interface includes the Serial Station Management Interfaces used to send power management and flow messages between devices. This consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire output buses and two 2-wire input buses. Each 2-wire bus includes a data signal and a clock signal.

Below figure illustrates the HyperLink bus connections on the TMDXEVM6614LXE EVM.

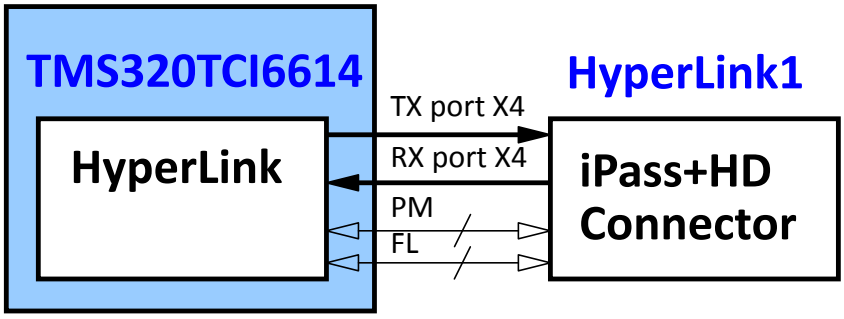


Figure 2.7: TMDXEVM6614LXE EVM HyperLink connections

2.11 PCI express interface

The 2 lane PCI express (PCIe) interface on TMDXEVM6614LXE provides a connection between the SoC and AMC edge connector. The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide (literature number SPRUGS6).

The TMDXEVM6614LXE provides the PCIe connectivity to AMC backplane on the EVM, this is shown in below figure.

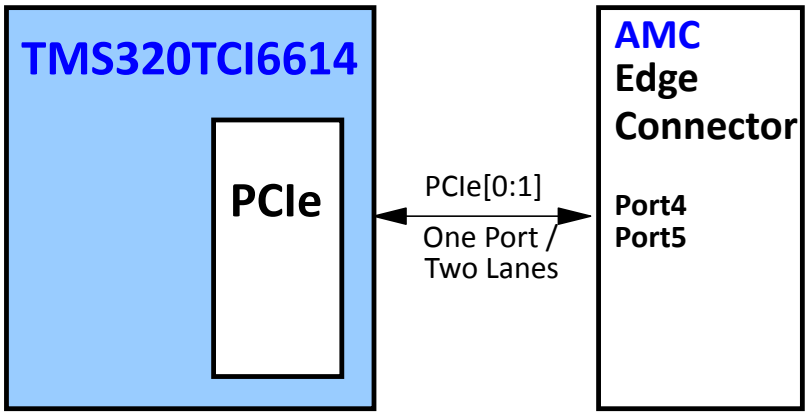


Figure 2.8: TMDXEVM6614LXE EVM PCIE Port Connections

2.12 Antenna Interface (AIF2)

The TMS320TCI6614 supports a high-speed SERDES-based Antenna Interface (AIF2) that operates up to 6.144Gbps. A six-lane SerDes-based Antenna Interface is available on the TMDXEVM6614LXE. Two Antenna Interface ports are routed to the AMC edge connector on the board and four Antenna interface ports are routed to the SFP connector.

Below figure shows the AIF connections on the TMDXEVM6614LXE EVM.

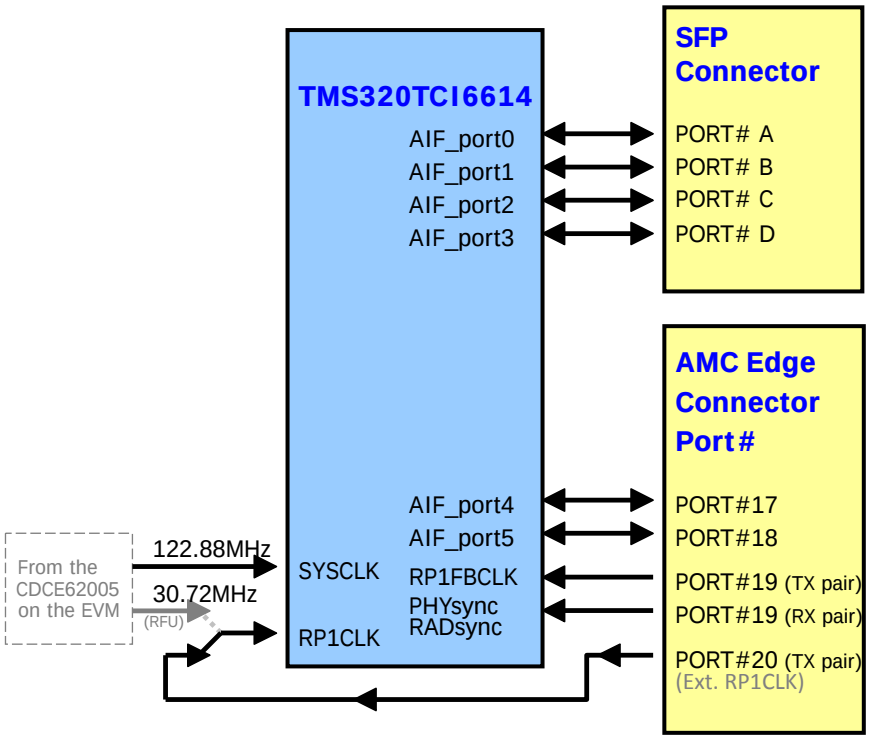


Figure 2.9: TMDXEVM6614LXE EVM AIF Port Connections

2.13 UART Interface

TMS320TCI6614 has two UART ports. One is provided for communication with GPS module, another can be accessed through the three-pin (Tx, Rx, and GND) serial port header (COM1). The selection can be made through the UART Route Select shunt-post COM_SEL1 as follows:

- UART to MMC - Shunts installed over COM_SEL1.3- COM_SEL1.1 and COM_SEL1.4 - COM_SEL1.2

- UART over 3-Pin Header (COM1) - Shunts installed over COM_SEL1.3- COM_SEL1.5 and COM_SEL1.4 –COM_SEL1.6 **(Default)**

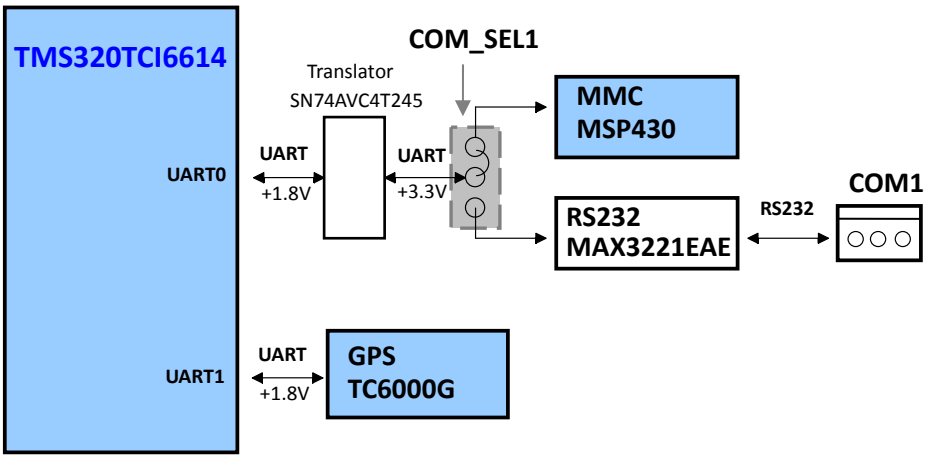


Figure 2.10: TMDXEVM6614LXE EVM UART Connections

2.14 Module Management Controller (MMC) for IPMI

The TMDXEVM6614LXE supports a limited set of Intelligent Platform Management Interface (IPMI) commands using the Module Management Controller (MMC) based on Texas Instruments MSP430F5435 mixed-signal processor.

The MMC communicates with the MicroTCA Carrier Hub (MCH) over the IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 R1.0-compliant chassis. The primary purpose of the MMC is to provide necessary information to the MCH, to enable the payload power to the TMDXEVM6614LXE EVM when it is inserted into the MicroTCA-compliant chassis.

The EVM also supports a Blue LED (D2) and Red LED (D1) on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of the initialization process when the MMC receives management power.

Blue LED (D2):

The blue LED comes ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED goes OFF when payload power is enabled to the EVM by the MCH.

Red LED (D1):

Red colored (D1) will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

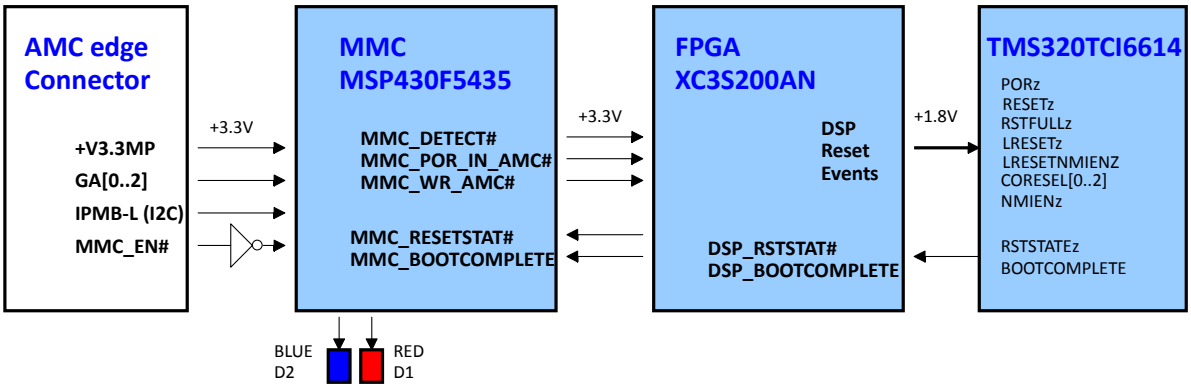


Figure 2.11: TMDXEVM6614LXE EVM MMC Connections for IPMI

2.15 Universal Subscriber identity module (USIM)

The TMS320TCI6614 is equipped with a Universal Subscriber Identity Module (USIM) for user authentication. TMDXEVM6614LXE is designed to support Class-B (2.95V) or Class-C (1.8V) level of USIM with a SIM card translator. The users can plug the USIM card at SIM1 and select the Class-B (2.95V) or Class-C (1.8V) interfaces through CN3.

2.16 Small Cell Application

As a means of supporting Small Cell Base station software development a GPS module, DAC, and VCTCXO are added to the EVM. DAC, DAC7611, is controlled by SPI interface on TMS320TCI6614 to adjust the output voltage for adjusting the frequency of VCTCXO. The block diagram is shown in the below figure:

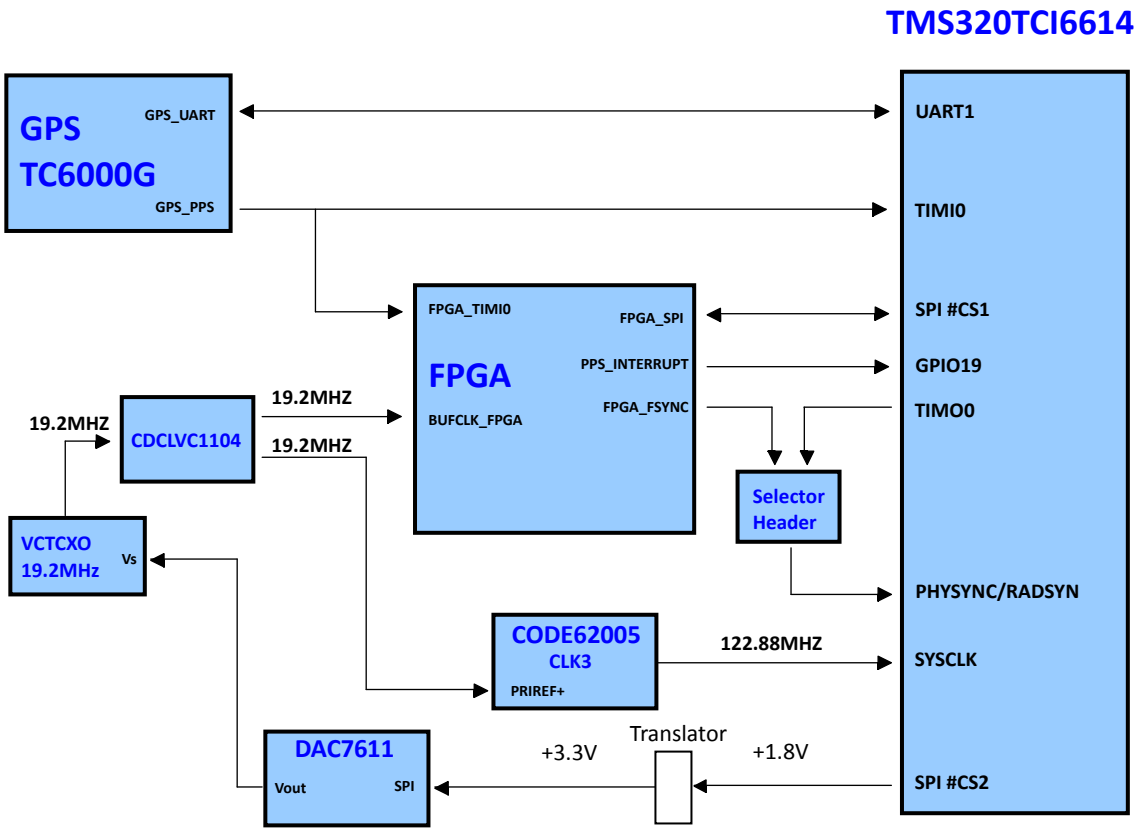


Figure 2.12: Block Diagram of Small Cell Application

2.17 Expansion Headers

The TMDXEVM6614LXE contains an 100-pin header (TEST_PH1) which has I^2C, TIMI[0:1], TIMO[0:1], SPI, GPIO[16:0], EMIF16, CLK2_SYNC, CLK3_SYNC, and UART signal connections. It should be noted that I^2C, TIMI[1:0], TIMO[0:1], SPI GPIO[16:0], and EMIF16 connections to this header (TEST_PH1) are 1.8 V whereas UART signals, CLK2_SYNC and CLK3_SYNC are 3.3 V level.

3. TMDXEVM6614LXE Board Physical Specifications

This chapter describes the physical layout of the TMDXEVM6614LXE board and its connectors, switches, and test points. It contains:

3.1 Board Layout

The TMDXEVM6614LXE board dimension is 225.6mm x 83.5mm. It is a 12-layer board and powered through connector DC_IN1. Figure 3.1 and 3.2 show assembly layout of the TMDXEVM6614LXE EVM Board.

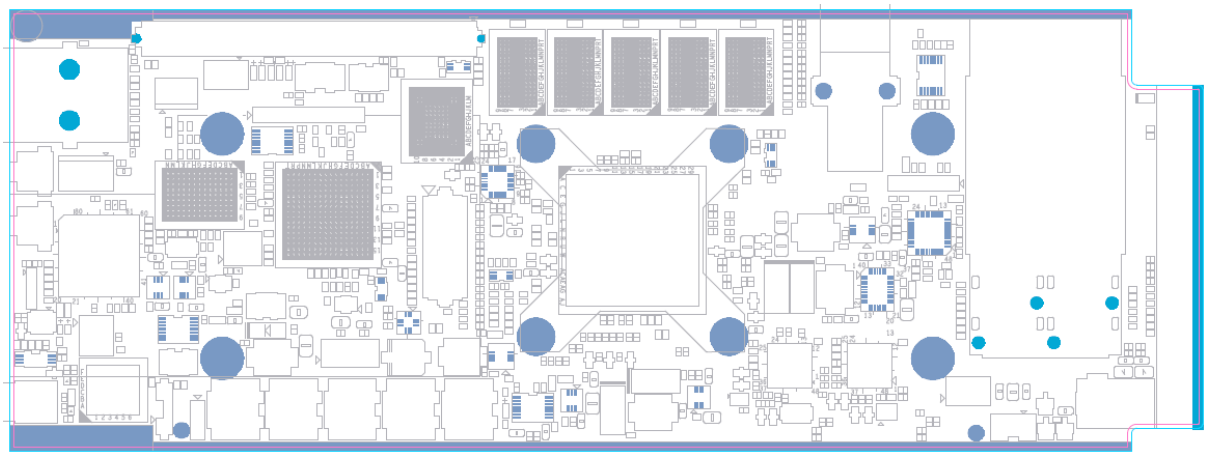


Figure 3.1: TMDXEVM6614LXE EVM Board Assembly Layout – TOP view

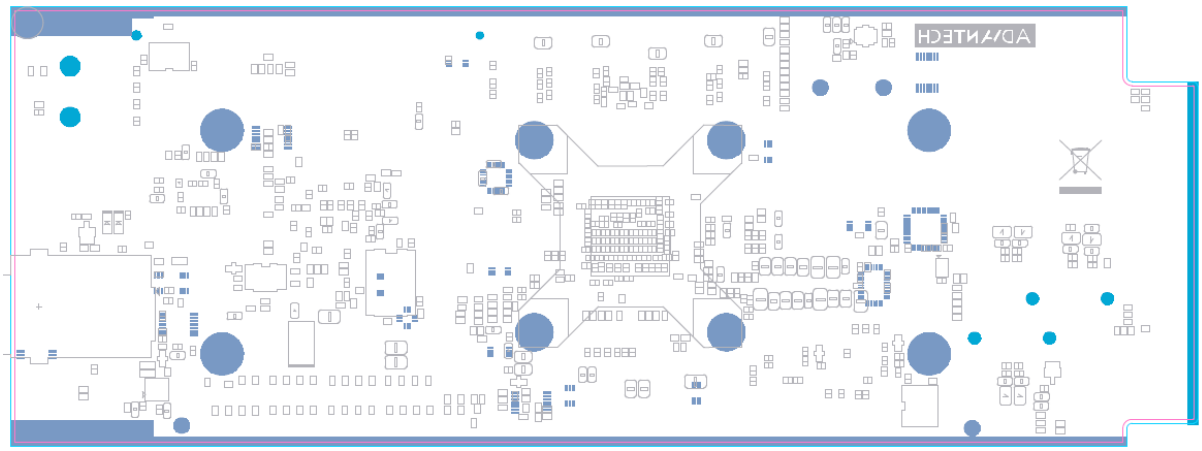


Figure 3.2: TMDXEVM6614LXE EVM Board layout – Bottom view

3.2 Connector Index

The TMDXEVM6614LXE Board has several connectors that provide access to various interfaces on the board.

Table 3.1: TMDXEVM6614LXE EVM Board Connectors

Connector	Pins	Function
560V2_PWR1	8	XDS560v2 Mezzanine Power Connector
AMC1	170	AMC Edge Connector
COM1	3	UART 3-Pin Connector
COM_SEL1	6	UART Route Select Jumper
DC_IN1	3	DC Power Input Jack Connector
EMU1	60	TI 60-Pin Emulation Connector
FAN1	3	FAN connector for +12V DC FAN
HyperLink1	36	HyperLink connector for companion chip/die interface
LAN1	12	Gigabit Ethernet RJ-45 Connector
PMBUS1	5	PMBUS for Smart-Reflex connected to UCD9222
TAP_FPGA1	8	FPGA JTAG Connector
SBW_MMC1	4	MSP430 Spy-Bi-Wire Connector -- For Factory Use Only
TEST_PH1	100	SPI, I^2C, GPIO, TIMI[1:0], TIMO[1:0],EMIF6, and UART0 connections
SIM1	8	USIM Connector
CN1	6	AIF SYNC Select Jumper
CN2	4	GPS SMA Antenna
CN3	3	USIM Voltage Rail Select Jumper
SFP1	80	SFP connector

3.2.1 560V2_PWR1, XDS560v2 Mezzanine Power Connector

560V2_PWR1 is an 8-pin power connector for the XDS560v2 mezzanine emulator board. The pin out of the connector is shown in the table below:

Table 3.2: XDS560v2 Power Connector pin out

Pin #	Signal Name
1	+5VSupply
2	+5VSupply
3	XDS560V2_IL
4	Ground
5	+3.3VSupply
6	+3.3VSupply
7	Ground
8	Ground

3.2.2 AMC1, AMC Edge Connector

The AMC card-edge connector plugs into an AMC compatible carrier board and provides 4 Serial RapidIO lanes, 2 PCIe lanes, 1 SGMII port, 2 AIF2 lanes and the system interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below.

Please note that the TCLKB and TCLKD on the EVM can now be used as optional common clock sources to synchronize the timing between two EVMs for the HyperLink and AIF interfaces. Also, the TCLKC pins can now be used as TMS320TCI6614 timer input and output signals buffered through the FPGA.

Table 3.3: AMC Edge Connector

Pin	Signal	Pin	Signal
1	GND	170	GND
2	VCC12	169	AMC_JTAG_TDI
3	MMC_PS_N1#	168	AMC_JTAG_TDO
4	VCC3V3_MP_AMC	167	AMC_JTAG_RST#
5	MMC_GA0	166	AMC_JTAG_TMS
6	RSVD	165	AMC_JTAG_TCK
7	GND	164	GND
8	RSVD	163	AMC_RP1CLKP
9	VCC12	162	AMC_RP1CLKN
10	GND	161	GND
11	AMC0_SGMII0_TX_DP	160	AMC_EXP_SCL
12	AMC0_SGMII0_TX_DP	159	AMC_EXP_SDA
13	GND	158	GND
14	AMC0_SGMII0_RX_DP	157	RP1FBP

Pin	Signal	Pin	Signal
15	AMC0_SGMII0_RX_DN	156	RP1FBN
16	GND	155	GND
17	MMC_GA1	154	PHYSYNC
18	VCC12	153	RADSYNC
19	GND	152	GND
20	NC	151	AMCC_P18_AIF5_TXP
21	NC	150	AMCC_P18_AIF5_TXN
22	GND	149	GND
23	NC	148	AMCC_P18_AIF5_RXP
24	NC	147	AMCC_P18_AIF5_RXN
25	GND	146	GND
26	MMC_GA2	145	AMCC_P17_AIF4_TXP
27	VCC12	144	AMCC_P17_AIF4_TXN
28	GND	143	GND
29	NC	142	AMCC_P17_AIF4_RXP
30	NC	141	AMCC_P17_AIF4_RXN
31	GND	140	GND
32	NC	139	TCLKD_P / CLK3_PRI_P
33	NC	138	TCLKD_N / CLK3_PRI_N
34	GND	137	GND
35	NC	136	TCLKC_P / DSP_TIMO0_AMC
36	NC	135	TCLKC_N / DSP_TIMI0_AMC
37	GND	134	GND
38	NC	133	NC
39	NC	132	NC
40	GND	131	GND
41	MMC_ENABLE_N	130	NC
42	VCC12	129	NC
43	GND	128	GND
44	AMCC_P4_PCIe_TX1P	127	NC
45	AMCC_P4_PCIe_TX1N	126	NC
46	GND	125	GND
47	AMCC_P4_PCIe_RX1P	124	NC
48	AMCC_P4_PCIe_RX1N	123	NC
49	GND	122	GND
50	AMCC_P5_PCIe_TX2P	121	NC
51	AMCC_P5_PCIe_TX2N	120	NC
52	GND	119	GND
53	AMCC_P5_PCIe_RX2P	118	NC
54	AMCC_P5_PCIe_RX2N	117	NC
55	GND	116	GND
56	SMB_SCL_IPMBL	115	NC
57	VCC12	114	NC
58	GND	113	GND
59	NC	112	NC

Pin	Signal	Pin	Signal
60	NC	111	NC
61	GND	110	GND
62	NC	109	AMCC_P11_SRIO4_TXP
63	NC	108	AMCC_P11_SRIO4_TXN
64	GND	107	GND
65	NC	106	AMCC_P11_SRIO4_RXP
66	NC	105	AMCC_P11_SRIO4_RXN
67	GND	104	GND
68	NC	103	AMCC_P10_SRIO3_TXP
69	NC	102	AMCC_P10_SRIO3_TXN
70	GND	101	GND
71	SMB_SDA_IPMBL	100	AMCC_P10_SRIO3_RXP
72	VCC12	99	AMCC_P10_SRIO3_RXN
73	GND	98	GND
74	TCLKA_P	97	AMCC_P9_SRIO2_TXP
75	TCLKA_N	96	AMCC_P9_SRIO2_TXN
76	GND	95	GND
77	TCLKB_P / CLK2_PRI_P	94	AMCC_P9_SRIO2_RXP
78	TCLKB_N / CLK2_PRI_N	93	AMCC_P9_SRIO2_RXN
79	GND	92	GND
80	PCIE_REF_CLK_P	91	AMCC_P8_SRIO1_TXP
81	PCIE_REF_CLK_N	90	AMCC_P8_SRIO1_TXN
82	GND	89	GND
83	MMC_PS_N0	88	AMCC_P8_SRIO1_RXP
84	VCC12	87	AMCC_P8_SRIO1_RXN
85	GND	86	GND

3.2.3 COM1, UART 3-Pin Connector

COM1 is a 3-pin male connector for RS232 serial interface. A 3-pin female to 9-pin DTE female cable is supplied with the TMDXEVM6614LXE to connect with the PC.

Table 3.4: UART Connector pin out

Pin #	Signal Name
1	Receive
2	Transmit
3	Ground

3.2.4 COM_SEL1, UART Route Select Connector

The UART0 on TMS320TCI6614 can be accessed through the three-pin RS232 Serial port header (COM1) or route the UART0 to MMC. The selection can be made through the UART route select connector COM_SEL1 as follows:

• UART to MMC: Shunts installed over COM_SEL1.3-COM_SEL1.1 and COM_SEL1.4-COM_SEL1.2

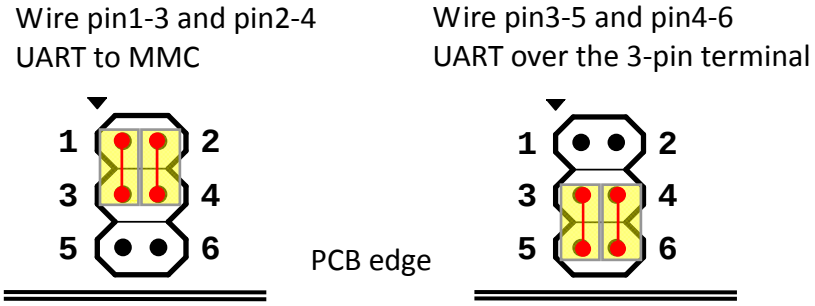
• UART over three-pin Header COM1 (**Default**): Shunts installed over COM_SEL1.3-COM_SEL1.5 and COM_SEL1.4-COM_SEL1.6.

The pin out for the connector is shown in the table below:

Table 3.5: UART Path Select Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	MSP430 Transmit	2	MSP430 Receive
3	UART Transmit	4	UART Receive
5	MAX3221 Transmit	6	MAX3221 Receive

Figure 3.3: COM_SEL1 Jumper setting



3.2.5 DC_IN1, DC Power Input Jack Connector

DC_IN1 is a DC Power-in jack Connector for the stand-alone application of TMDXEVM6614LXE. It is a 2.5 mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into the MicroTCA chassis or the AMC carrier backplane.

3.2.6 EMU1, TI 60-Pin Emulation Connector

EMU1 is a high speed system trace capable TI 60-pin JTAG connector for XDS560v2 type of SoC emulation. The XDS560v2 mezzanine card can be removed and install other compatible external emulator if it is necessary. The I/O voltage level on EMU1 is 1.8 V. So any 1.8V compatible emulator can be used to interface with the TMS320TCI6614 SoC. It should be noted that when an external emulator is plugged into this connector (EMU1), the JTAG port on the AMC edge connector will be disconnected from the SoC. The pin out for the connector is shown in the table below:

Table 3.6: TI 60-pin Emulation Connector pin out

Pin #	Signal Name	Pin #	Signal Name
A1	EMU_DET	C1	ID2 (GND)
A2	Ground	C2	EMU18
A3	Ground	C3	TRST#
A4	Ground	C4	EMU16
A5	Ground	C5	EMU15
A6	Ground	C6	EMU13
A7	Ground	C7	EMU11
A8	Type0 (NC)	C8	TCLKRTN
A9	Ground	C9	EMU10
A10	Ground	C10	EMU8
A11	Ground	C11	EMU6
A12	Ground	C12	EMU4
A13	Ground	C13	EMU3
A14	Ground	C14	EMU1
A15	TRGRST#	C15	ID3 (GND)
B1	ID0 (GND)	D1	NC
B2	TMS	D2	Ground
B3	EMU17	D3	Ground
B4	TDI	D4	Ground
B5	EMU14	D5	Ground
B6	EMU12	D6	Ground
B7	TDO	D7	Ground
B8	TVD (+1.8V)	D8	Type1 (GND)
B9	EMU9	D9	Ground
B10	EMU7	D10	Ground
B11	EMU5	D11	Ground
B12	TCLK	D12	Ground
B13	EMU2	D13	Ground
B14	EMU0	D14	Ground
B15	ID1 (GND)	D15	Ground

3.2.7 FAN1, FAN Connector

The EVM incorporates a dedicated cooling fan. This fan has the capability of easily being removed when the EVM is inserted into an AMC backplane which uses forced air cooling. The fan selected provides maximum cooling (CFM) and operates on 12Vdc. FAN1 will be connected to provide 12Vdc to the fan.

Table 3.7: FAN1 Connector pin out

Pin #	Signal Name
1	GND
2	+12Vdc
3	NC

3.2.8 HyperLink1, HyperLink Connector

The EVM provides a HyperLink connection by a mini-SAS HD+ 4i connector. The connector contains 8 SERDES pairs and 4 sideband sets to carry full HyperLink signals. The connector is shown in Figure 3.4. and its pin out is shown in Table 3.8.

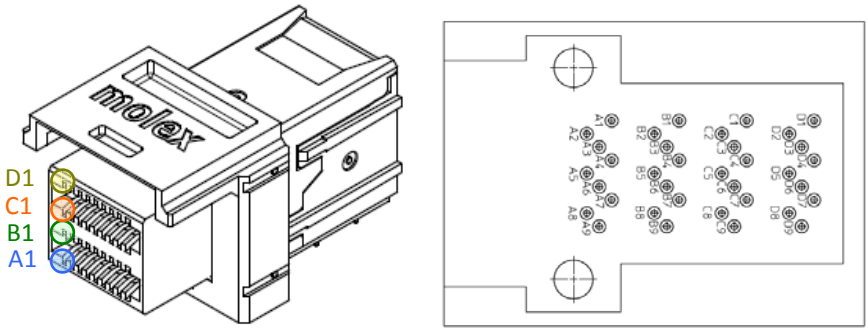


Figure 3.4: The HyperLink Connector

Table 3.8: The HyperLink Connector

Pin#	Net	Pin#	Net
A1	HyperLink_TXFLCLK	B1	HyperLink_RXPMDAT
A2	HyperLink_RXFLCLK	B2	HyperLink_TXFLDAT
A3	GND	B3	GND
A4	HyperLink_RXP1	B4	HyperLink_RXP0
A5	HyperLink_RXN1	B5	HyperLink_RXN0
A6	GND	B6	GND
A7	HyperLink_RXP3	B7	HyperLink_RXP2
A8	HyperLink_RXN3	B8	HyperLink_RXN2
A9	GND	B9	GND
C1	HyperLink_TXPMDAT	D1	HyperLink_RXPMCLK
C2	HyperLink_TXPMCLK	D2	HyperLink_RXFLDAT
C3	GND	D3	GND
C4	HyperLink_TXP1	D4	HyperLink_TXP0
C5	HyperLink_TXN1	D5	HyperLink_TXN0
C6	GND	D6	GND
C7	HyperLink_TXP3	D7	HyperLink_TXP2
C8	HyperLink_TXN3	D8	HyperLink_TXN2
C9	GND	D9	GND

3.2.9 LAN1, Ethernet Connector

LAN1 is a Gigabit RJ45 Ethernet connector with integrated magnetics. It is driven by Marvell Gigabit Ethernet transceiver 88E1111. The connections are shown in the table below:

Table 3.9: Ethernet Connector pin out

Pin #	Signal Name
1	Center Tap2
2	MD2-
3	MD2+
4	MD1-
5	MD1+
6	Center Tap1
7	Center Tap3
8	MD3+
9	MD3-
10	MD0-
11	MD0+
12	Center Tap0
13	ACT_LED1-
14	ACT_LED1+
15	LINK1000_LED2-
16	LINK_LED2+
17	LINK100_LED2-
H3	Shield 1
H4	Shield 2

3.2.10 PMBUS1, PMBUS Connector for Smart-Reflex Control

The TMS320TCI6614 SoC core power is supplied by a Smart-Reflex power controller UCD9222 with the Integrated FET Driver UCD74110 and UCD74106. PMBUS1 provides a connection between UCD9222 and remote connection during development. Through the USB to GPIO pod provided by TI, the user can trace and configure the parameters in UCD9222 with the Smart-Fusion GUI. The pin out of PMBUS1 is shown in table 3.10.

Table 3.10: PMBUS1 Pin out

Pin #	Signal Name
1	PMBUS_CLK
2	PMBUS_DAT
3	PMBUS_ALT
4	PMBUS_CTL
5	GND

3.2.11 TAP_FPGA1, FPGA JTAG Connector (For Factory Use Only)

TAP_FPGA1 is an 8-pin JTAG connector for the FPGA programming and the PHY boundary test of the factory only. The pin out for the connector is shown in the figure below:

Table 3.11: FPGA JTAG Connector pin out

Pin #	Signal Name
1	VCC3V3_FPGA
2	GND
3	BSC_JTAG_TCK
4	BSC_JTAG_TDI
5	BSC_JTAG_TDO
6	BSC_JTAG_TMS
7	BSC_JTAG_RST#
8	BSC_JTAG_P8(PU)

In FPGA debugging and programming mode, pin 8 of BSC_JTAG_P8 keep as PU pin to the EVM board.

The diagram of the boundary scan route is shown in Figure 3.5

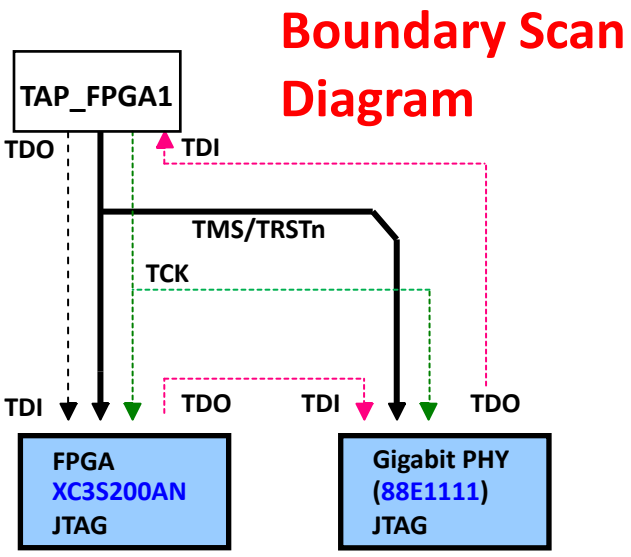


Figure 3.5: TAP_FPGA1 function diagram

3.2.12 SBW_MMC1, MSP430 SpyBiWire Connector (For Factory Use Only)

SBW_MMC1 is a 4-pin SpyBiWire connector for IPMI software loading into MSP430. The TMDXEVM6614LXE is supplied with IPMI software already loaded into MSP430. The pin out of the connector is shown in the table below:

Table 3.12: MSP430 SpyBiWire Connector pin out

Pin #	Signal Name
1	GND
2	VCC3V3_MP
3	MMC_SBWTDIO
4	MMC_SBWTCK

3.2.13 TEST_PH1, Expansion Header (SPI, GPIO, Timer I/O, I^2C, and UART)

TEST_PH1 is an expansion header for several interfaces on the SoC; there are SPI, GPIO, Timer, I^2C, and UART. The signal connections to the expansion header are shown in below table:

Table 3.13: TEST_PH1, The Expansion Header pin out

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	2	GND	Ground
3	DSP_SDA	SoC I2C data	4	DSP_EMIFA00	EMIF address
5	DSP_SCL	SoC I2C clock	6	DSP_EMIFA01	EMIF address
7	GND	Ground	8	DSP_EMIFA02	EMIF address
9	DSP_EMIFD0	EMIF data	10	DSP_EMIFA03	EMIF address
11	DSP_EMIFD1	EMIF data	12	DSP_EMIFA04	EMIF address
13	DSP_EMIFD2	EMIF data	14	GND	Ground
15	DSP_EMIFD3	EMIF data	16	DSP_EMIFA05	EMIF address
17	GND	Ground	18	DSP_EMIFA06	EMIF address
19	DSP_EMIFD4	EMIF data	20	DSP_EMIFA07	EMIF address
21	DSP_EMIFD5	EMIF data	22	DSP_EMIFA08	EMIF address
23	DSP_EMIFD6	EMIF data	24	DSP_EMIFA09	EMIF address
25	DSP_EMIFD7	EMIF data	26	GND	Ground
27	GND	Ground	28	DSP_EMIFA10	EMIF address
29	DSP_EMIFD8	EMIF data	30	DSP_EMIFA11	EMIF address
31	DSP_EMIFD9	EMIF data	32	DSP_EMIFA12	EMIF address
33	DSP_EMIFD10	EMIF data	34	DSP_EMIFA13	EMIF address
35	DSP_EMIFD11	EMIF data	36	DSP_EMIFA14	EMIF address
37	GND	Ground	38	GND	Ground
39	DSP_EMIFD12	EMIF data	40	DSP_EMIFA15	EMIF address
41	DSP_EMIFD13	EMIF data	42	DSP_EMIFA16	EMIF address

43	DSP_EMIFD14	EMIF data	44	DSP_EMIFA17	EMIF address
45	DSP_EMIFD15	EMIF data	46	DSP_EMIFA18	EMIF address
47	GND	Ground	48	DSP_EMIFA19	EMIF address
49	DSP_EMIFCE1Z	EMIF control signals	50	GND	Ground
51	DSP_GPIO_16	SoC GPIO16	52	DSP_EMIFA20	EMIF address
53	GND	Ground	54	DSP_EMIFA21	EMIF address
55	DSP_EMIFBE0Z	EMIF control signals	56	DSP_EMIFA22	EMIF address
57	DSP_EMIFBE1Z	EMIF control signals	58	DSP_EMIFA23	EMIF address
59	DSP_EMIFOEZ	EMIF control signals	60	GND	Ground
61	DSP_EMIFWEZ	EMIF control signals	62	DSP_GPIO_00	SoC GPIO0
63	DSP_EMIFRNW	EMIF control signals	64	DSP_GPIO_01	SoC GPIO1
65	DSP_EMIFWAIT1	EMIF control signals	66	DSP_GPIO_02	SoC GPIO2
67	GND	Ground	68	DSP_GPIO_03	SoC GPIO3
69	DSP_TIMI0	Timer input 0 to FPGA for the SoC Timer0 input	70	DSP_GPIO_04	SoC GPIO4
71	DSP_TIMO0	Timer output 0	72	DSP_GPIO_05	SoC GPIO5
73	DSP_TIMI1	Timer input 1	74	DSP_GPIO_06	SoC GPIO6
75	DSP_TIMO1	Timer output 1	76	DSP_GPIO_07	SoC GPIO7
77	GND	Ground	78	DSP_GPIO_08	SoC GPIO8
79	DSP_SSPMISO	SPI data input	80	DSP_GPIO_09	SoC GPIO9
81	DSP_SSPMOSI	SPI data output	82	DSP_GPIO_10	SoC GPIO10
83	DSP_SSPCS1	SPI chip select	84	DSP_GPIO_11	SoC GPIO11
85	PH_SSPCK	SPI clock	86	DSP_GPIO_12	SoC GPIO12
87	GND	Ground	88	DSP_GPIO_13	SoC GPIO13
89	GND	Ground	90	DSP_GPIO_14	SoC GPIO14
91	DSP_UARTTXD	UART Serial Data Out(+3.3v)	92	DSP_GPIO_15	SoC GPIO15
93	DSP_UARTRXD	UART Serial Data In (+3.3v)	94	GND	Ground
95	DSP_UARTRTS	UART Request To Send (+3.3v)	96	CLK2_SYNC	The HyperLink common control signal
97	DSP_UARTCTS	UART Cear To Send (+3.3v)	98	CLK3_SYNC	The AIF2 common timing control signal
99	GND	Ground	100	GND	Ground

3.2.14 USIM1, USIM Connector

USMI1 is a USMI connector routed to the TMS320TCI6614, and supports Class-B (2.95V) and Class-C (1.8V) interfaces selected by USIM Voltage Rail Select Jumper, CN3. The following table shows the Pin out of the USIM connector.

Table 3.14: USIM Connector pin out

Pin #	Signal Name
C1	SIM_VCC
C2	SIM_RST
C3	SIM_CLK
C5	GND
C6	NC
C7	SIM_IO
SW1	USIM detection
SW2	SIM_EN
H1	Shield 1
H2	Shield 1

3.2.15 CN1, AIF SYNC Select Jumper

The AIF SNC select jumper determines that the PHYSYNC and RADSYNC are routed from DSP_TIMO0 or FPGA_FSYNC. The default configuration is wired the CN1.1-CN1.3 and CN1.4-CN1.6 by shunts.

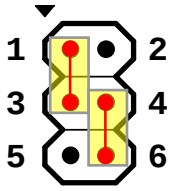
The pin out for the connector is shown in the table below:

Table 3.15: AIF SYNC Select pin out

Pin #	Signal Name	Pin #	Signal Name
1	DSP_TIMO0	2	DSP_TIMO0
3	RADSYNC	4	PHYSYNC
5	FPGA_FSYNC	6	FPGA_FSYNC

Figure 3.6: AIF SYNC Select Jumper setting

Wire pin1-3 and pin2-4



3.2.16 CN2, GPS SMA Antenna

CN2 is a SMA connector to connect the external GPS Antenna for the GPS module.

3.2.17 CN3, USIM Voltage Rail Select Jumper

TMDXEVM6614LXE supports 1.8V or 2.95V USIM interface, and use CN3 to select it

- 2.95V USIM interface: Shunts installed over pin1 and pin2
- 1.8V USIM interface: Shunts installed over pin2 and pin3

The pin out for the connector is shown in the table below:

Table 3.16: USIM Voltage Rail Select Jumper pin out

Pin #	Signal Name
1	VCC1V8
2	SIM_SEL
3	GND

3.2.18 SFP1, SFP connector

SFP1 is a 4 ports SFP connector. The pin out of connector is shown in below table:

Table 3.17: TEST_PH1, The Expansion Header pin out

Pin	Signal	Pin	Signal
A1	GND	C1	GND
A2	TX_FAULT1	C2	TX_FAULT3
A3	TX_DISABLE1	C3	TX_DISABLE3
A4	MOD1_SDA	C4	MOD3_SDA
A5	MOD1_SCK	C5	MOD3_SCK
A6	MOD1_DEF0	C6	MOD3_DEF0
A7	RATESELECT_1	C7	RATESELECT_3
A8	LOS_1	C8	LOS_3
A9	GND	C9	GND
A10	GND	C10	GND
A11	GND	C11	GND
A12	SFP_AIF0_RXN	C12	SFP_AIF2_RXN
A13	SFP_AIF0_RXP	C13	SFP_AIF2_RXP

A14	GND	C14	GND
A15	VCCR1	C15	VCCR3
A16	VCCT1	C16	VCCT3
A17	GND	C17	GND
A18	SFP_AIF0_TXP	C18	SFP_AIF2_TXP
A19	SFP_AIF0_TXN	C19	SFP_AIF2_TXN
A20	GND	A20	GND
B1	GND	D1	GND
B2	TX_FAULT2	D2	TX_FAULT4
B3	TX_DISABLE2	D3	TX_DISABLE4
B4	MOD2_SDA	D4	MOD4_SDA
B5	MOD2_SCK	D5	MOD4_SCK
B6	MOD2_DEF0	D6	MOD4_DEF0
B7	RATESELECT_2	D7	RATESELECT_4
B8	LOS_2	D8	LOS_4
B9	GND	D9	GND
B10	GND	D10	GND
B11	GND	D11	GND
B12	SFP_AIF1_RXN	D12	SFP_AIF3_RXN
B13	SFP_AIF1_RXP	D13	SFP_AIF3_RXP
B14	GND	D14	GND
B15	VCCR2	D15	VCCR4
B16	VCCT2	D16	VCCT4
B17	GND	D17	GND
B18	SFP_AIF1_TXP	D18	SFP_AIF3_TXP
B19	SFP_AIF1_TXN	D19	SFP_AIF3_TXN
B20	GND	D20	GND

3.3 DIP and Pushbutton Switches

The TMDXEVM6614LXE has 2 push button switches and 21 sliding DIP switches s. The RST_FULL1 and RST_WARM1 are push button switches while SW2, SW3, SW4, SW5, SW6 and SW7 are DIP switches. The function of each of the switches is listed in the table below:

Table 3.18: TMDXEVM6614LXE EVM Board Switches

Switch	Function
RST_FULL1	Full Reset Event
RST_WARM1	Warm Reset Event
SW2	Boot master, PCIESS Enable/Disable, CORECLKSEL and PASSCLKSEL
SW3	Boot mode, SoC boot Configuration
SW4	Boot mode ,SoC boot Configuration
SW5	Boot mode ,SoC boot Configuration
SW6	SoC boot Configuration, PLL setting, PCIe mode Selection
SW7	No function

3.3.1 RST_FULL1, Full Reset

Pressing the RST_FULL1 button switch will issue a RESETFULL# to TMS320TCI6614 by the FPGA. It'll reset SoC and other peripherals.

3.3.2 RST_WARM1, Warm Reset

Pressing the RST_WARM1 button switch will issue a RESET# to TMS320TCI6614 by the FPGA. The FPGA will assert the RESET# signal to the SoC and the SoC will execute either a HARD or SOFT resets by the configuration in the RSCFG register in PLLCTL.

Note: Users may refer to the TMS320TCI6614 Data Manual to check the difference between assertion of SoC RESET# and SoC POR# signals.

3.3.3 SW2, SW3, SW4, SW5, and SW6 SoC Boot Configurations

SW2, SW3, SW4, SW5, and SW6 are four-position DIP switches, which are used for ENDIAN, Boot Master, Boot Device, Boot Configuration, and PCI Express subsystem configuration. For the details about the Boot modes and their configuration, please refer to the TMS320TCI6614 Data Manual.

The diagram of the default setting on these switches is shown below:

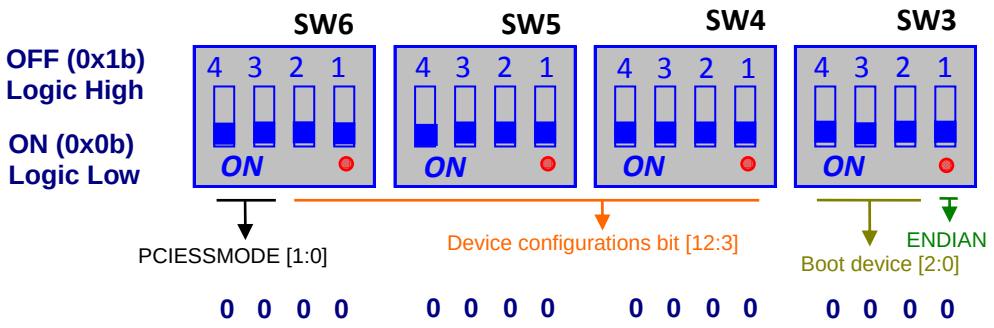


Figure 3.7: SW3, SW4, SW5, and SW6 default settings

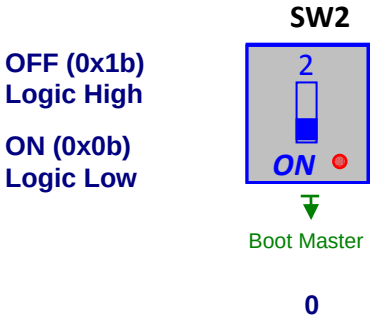


Figure 3.8: SW2, switch 2 default settings

The following table describes the positions and corresponding functions on SW.

Table 3.19: SW2-SW6, Configuration Switch with CorePac as Boot Master

SW#	Description	Default Value	Function
SW2[2]	Boot Master/ BOOTMODE[14]	0x0b (ON)	**Boot Master** 0=CorePac initiates boot 1=ARM initiates boot
SW3[1]	ENDIAN/ BOOTMODE[0]	0x0b (ON)	**Device endian mode (LENDIAN).** 0 = Device operates in big endian mode 1 = Device operates in little endian mode
SW3[4:2]	Boot device/ BOOTMODE[3:1]	0x000b (ON,ON,ON)	**Boot Device** 000b = No boot / EMIF16 001b = Serial Rapid I/O 010b = SGMII (PA driven from core clk) 011b = SGMII (PA driver from PA clk) 100b = PCI Express 101b = I2C 110b = SPI 111b = HyperLink
SW4[2:1]	Reserved/ BOOTMODE[5:4]	0x00b (ON,ON)	reserved in all modes except I2C master boot mode
SW4[4:3] SW5[3:1]	Device Configuration/ BOOTMODE[10:6]	0x00000b (ON,ON,ON ON, ON,)	The device configuration fields BOOTMODE [10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode. For the details about the device configuration, please refer to the TMS320TCI6614 Data Manual.
SW5[4] SW6[1:2]	PLL Mult I2C / SPI Ext Dev Cfg/ BOOTMODE[13:11]	0x000b (ON,ON,ON)	For the details about the device PLL settings, please refer to the TMS320TCI6614 Data Manual.

SW6[4:3]	PCIESSMODE [1:0]	0x00b (ON,ON)	**PCIe Subsystem mode selection.** 00b = PCIe in end point mode 01b = PCIe legacy end point (no support for MSI) 10b = PCIe in root complex mode 11b = Reserved

Table 3.20: SW2-SW6, Configuration Switch with ARM as Boot Master

SW#	Description	Default Value	Function
SW2[2]	Boot Master/ BOOTMODE[14]	0x0b (ON)	**Boot Master** 0=CorePac initiates boot 1=ARM initiates boot
SW3[1]	ENDIAN/ BOOTMODE[0]	0x0b (ON)	**Device endian mode (LENDIAN).** 0 = Device operates in big endian mode 1 = Device operates in little endian mode
SW3[3:2]	Reserved/ BOOTMODE[2:1]	0x00b (ON,ON)	**Reserved**
SW3[4] SW4[3:1]	Boot Mode Config / BOOTMODE[6:3]	0x000b (ON,ON,ON)	Boot mode configuration fields. For the details about the device configuration, please refer to the TMS320TCI6614 Data Manual.
SW4[4] SW5[3:1]	Boot Mode Sequence / BOOTMODE[10:7]	0x0000b (ON,ON,ON ON)	**Boot Device** 0000b = 1st No boot, 2nd NA 0001b = 1st UART, 2nd EMIF16 0010b = 1st UART, 2nd EMIF16/wait 0011b = 1st UART, 2nd NAND 0100b = 1st Ethernet, 2nd EMIF16 0101b = 1st Ethernet, 2nd EMIF16/wait 0110b = 1st Ethernet, 2nd NAND 0111b = 1st PCIe, 2nd EMIF16 1000b = 1st PCIe, 2nd EMIF16/wait 1001b = 1st PCIe, 2nd NAND 1010b = 1st SPI, 2nd EMIF16 1011b = 1st SPI, 2nd EMIF16/wait 1100b = 1st SPI, 2nd NAND 1101b = 1st EMIF16, 2nd NAND 1110b = 1st NAND/I2C, 2nd EMIF16 1111b = 1st NAND, 2nd EMIF16
SW5[4] SW6[1:2]	PLL Cfg/ BOOTMODE[13:11]	0x000b (ON,ON,ON)	For the details about the device PLL settings, please refer to the TMS320TCI6614 Data Manual.

3.3.4 SW2, PCIESSEN / Boot Master and CORECLKSEL / PACLKSEL Switch Configuration

SW2 is a 4-position DIP switch. The first position is used for enabling the PCI Express Subsystem within the SoC. The second position is for boot master. The third and fourth positions are used by selecting the PLL sources for CORECLK and PASSCLK of the SoC. A diagram of the SW2 switch (with factory default settings) is shown below:

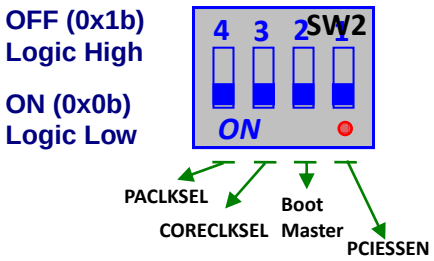


Figure 3.9: SW2 default settings

The following table describes the positions and corresponding functions on SW2.

Table 3.21: SW2, SoC PCIESSEN and Boot Master / CORECLKSEL/ PACLKSEL

SW2	Description	Default Value	Function
SW2[1]	PCIESSEN	0x0b (ON)	PCIe module enable. 0 = PCIe module disabled 1 = PCIe module enabled
SW2[2]	User Switch	0x0b (ON)	Boot Master
SW2[3]	CORECLKSEL	0x0b (ON)	**CORECLKSEL :** RFU, Reserved for Future Use
SW2[4]	PACLKSEL	0x0b (ON)	**PACLKSEL :** RFU, Reserved for Future Use

3.4 Test Points

The TMDXEVM6614LXE EVM Board has 47 test points. The position of each test point is shown in the figures below:

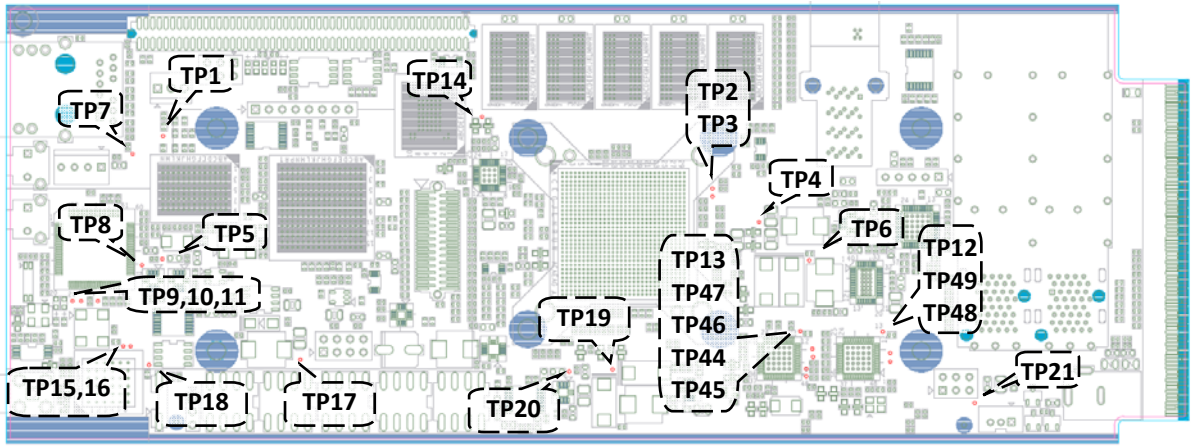


Figure 3.10: TMDXEVM6614LXE test points on top side

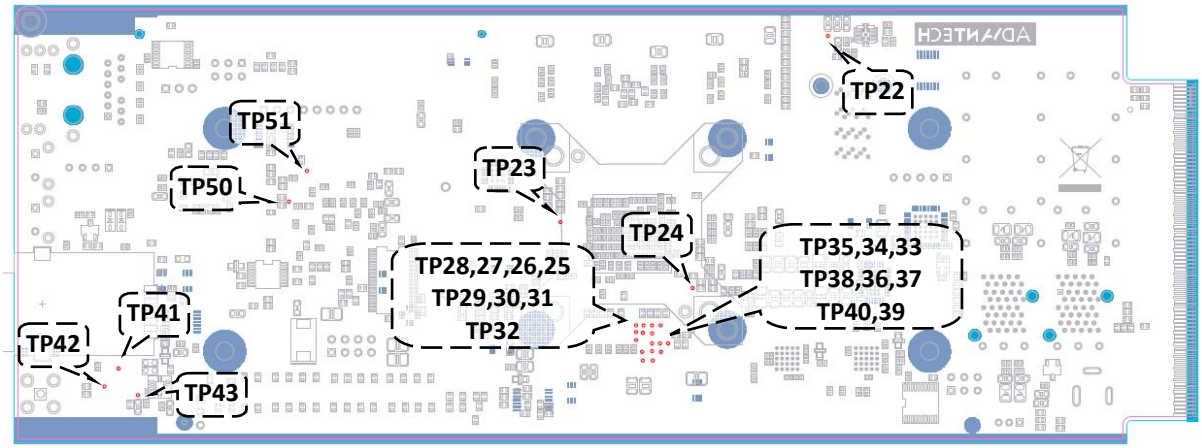


Figure 3.11: TMDXEVM6614LXE test points on the bottom side

Table 3.22: TMDXEVM6614LXE EVM Board Test Points

Test Point	Signal
TP9	Reserved for MMC1 pin23
TP11	Reserved for MMC1 pin33
TP10	Reserved for MMC1 pin25
TP8	Reserved for MMC1 pin43
TP2	HyperLink_REFCLKOUTP
TP3	HyperLink_REFCLKOUTN
TP24	DSP_SYSCLKOUT
TP25	DSP_GPIO29
TP26	DSP_GPIO18
TP27	DSP_GPIO27
TP30	DSP_GPIO25
TP31	DSP_GPIO24
TP32	DSP_GPIO21
TP33	DSP_GPIO30
TP34	DSP_GPIO28
TP35	DSP_GPIO20
TP36	DSP_GPIO31
TP37	DSP_GPIO17
TP38	DSP_GPIO26
TP39	DSP_GPIO23
TP40	DSP_GPIO22
TP23	Reserved for DSP1 pin N 5(EMIFCE2Z)
TP28	Reserved for DSP1 pin AK16 (UART1CTS)
TP29	Reserved for DSP1 pin AJ16 (UART1RTS)
TP1	PHY1 (88E1111) 125MHz clock (default: disable)
TP42	Reserved for GPS1 pin C2 (TCXO_CLK)
TP50	Reserved for FPGA1 (XC3S200AN) pin M4 (+1.8V I/O).
TP51	Reserved for FPGA1 (XC3S200AN) pin N3 (+1.8V I/O).
TP13	Reserved for CLK2 pin13
TP44	Reserved for CLK2 pin3
TP45	Reserved for CLK2 pin2
TP46	Reserved for CLK2 pin6
TP47	Reserved for CLK2 pin7
TP48	Reserved for CLK3 pin6
TP49	Reserved for CLK3pin7
TP12	Reserved for CLK3 pin13
TP6	Test point for CVDD

TP5	Test point for VCC1V2
TP43	Test point for VCC1V8_AUX
TP7	Test point for VCC2V5
TP20	Test point for VCC1V8
TP22	Test point for VCC0V75
TP14	Test point for VCC3V3_AUX
TP17	Test point for VCC5
TP4	Test point for VCC1V5
TP19	Test point for VCC1V0
TP21	Test point for VCC12

3.5 System LEDs

The TMDXEVM6614LXE board has 7 LEDs. Their positions on the board are indicated in figure 3.12. The description of each LED is listed in the table below:

Table 3.23: TMDXEVM6614LXE EVM Board LEDs

LED#	Color	Description
D3	Red	Failure and Out of service status in AMC chassis
D4	Blue	Hot Swap status in AMC chassis
SYSPG_D1	Blue	All Power rails are stable on AMC
FPGA_D1-D4	Blue	Debug LEDs.

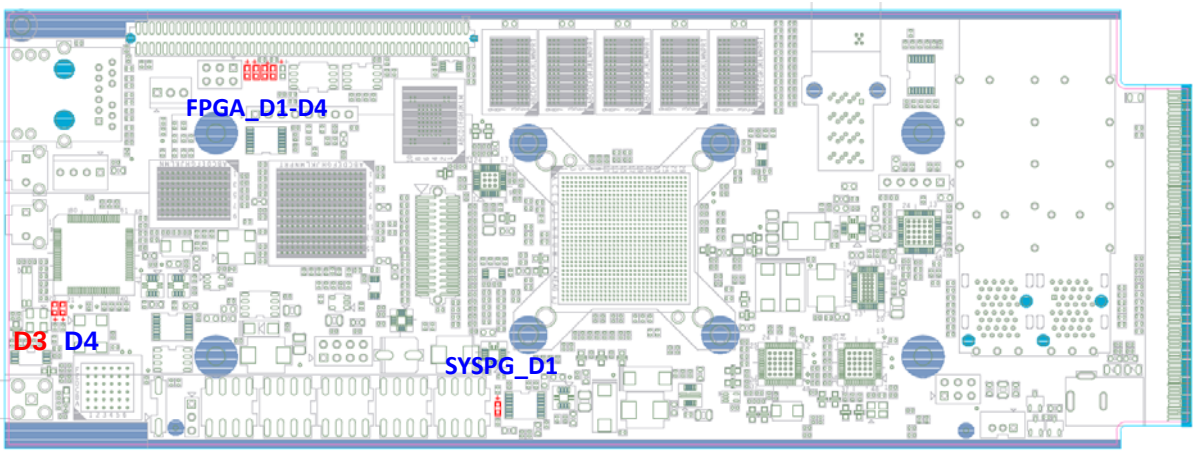


Figure 3.12: TMDXEVM6614LXE EVM Board LEDs

4. System Power Requirements

This chapter describes the power design of the TMDXEVM6614LXE board. It contains:

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units. The selected AC/DC 12-V adapter should be rated for a minimum of 36 Watts.

The power planes in TMDXEVM6614LXE are identified in the following table:

Table 4.1: EVM Voltage Table

Device	Net name	Voltage	Description
Input	3.3V_MP_AMC	+3.3 V	Management Power for MMC
	VCC12	+12 V	Payload Power to AMC
Management	VCC3V3_AUX	+3.3 V	3.3 V Power Rail for all support devices on EVM
	VCC1V2	+1.2 V	1.2 V Power Rail for all support devices on EVM
	VCC1V8_AUX	+1.8V	1.8V Power Rail for all support devices on EVM
TMS320TCI6614	CVDD	+0.6V~1.10V	SoC Core Power
	VCC1V0	+1.0V	SoC Fixed Core Power
	VCC1V8	+1.8V	SoC I/O power
	VCC1V5	+1.5V	SoC DDR3 and SERDES Power
DDR3 Memory	VCC1V5	+1.5V	DDR3 RAM Power
	VCC0V75	+0.75V	DDR3 RAM Termination Power
NAND Flash	VCC1V8	+1.8V	NAND Flash Power
NOR Flash (SPI)	VCC1V8	+1.8V	SPI NOR Flash Power
CDCE62002	VCC3V3_AUX	+3.3V	Clock Gen Power
CDCE62005	VCC3V3_AUX	+3.3V	Clock Gen Power
PHY (88E111)	VCC2V5	+2.5V	PHY Analog and I/O Power
	VCC1V2	+1.2V	PHY Core Power (instead of 1.0V)
MMC (MPS430)	VCC3V3_MP	+3.3V	MMC Power
FPGA	VCC1V2	+1.2V	FPGA Core Power
	VCC3V3_AUX	+3.3V	FPGA I/O Power for +3.3V bank
	VCC1V8_AUX	+1.8V	FPGA I/O Power for +1.8V bank
Misc. Logic	VCC3V3_AUX	+3.3V	Translator and Logic Power
	VCC1V8_AUX	+1.8V	Translator and Logic Power
GPS module	VCC1V8	+1.8V	GPS module power
DAC (DAC7611)	VCC5	+5V	DAC power

4.2 Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1 as well as on the schematic.

In Figure 4.1, the Auxiliary power rails are always on after payload power is supplied. These regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX

- VCC1V8_AUX
- VCC1V2
- VCC5_AUX

The maximum allowable power is 36 W from the external AC brick supply or from the 8 AMC header pins.

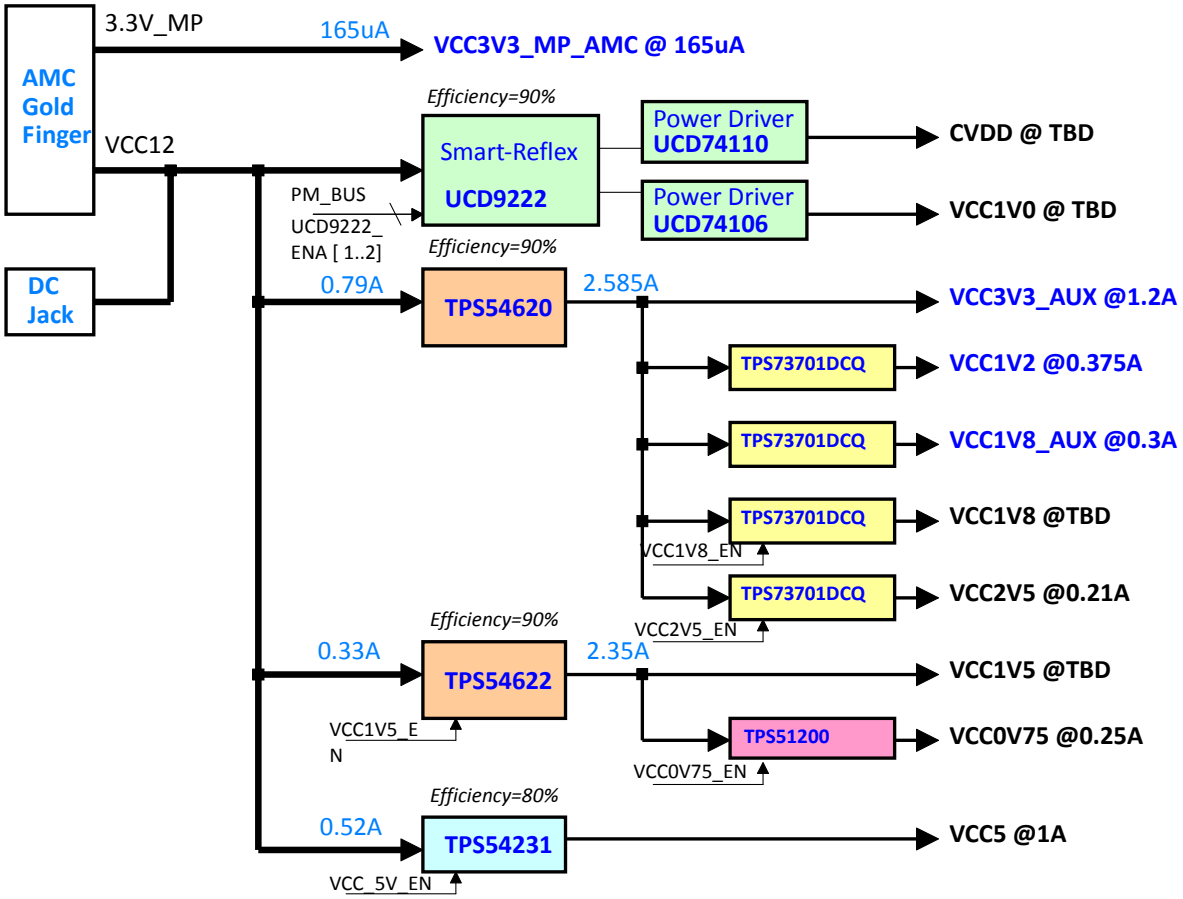


Figure 4.1: All the AMC power supply on TMDXEVM6614LXE EVM

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (See section 4.3 for specific details). The goal of all power supply designs is to support a minimum temperature range of 0°C to 45°C.

The TMS320TCI6614 core power is supplied using a dual digital controller coupled to a high performance FET driver IC. Additional SoC supply voltages are provided by discrete TI Swift power supplies. The TMS320TCI6614 supports a VID interface to enable Smart-Reflex® power supply control for its primary core logic supply. Refer to the TMS320TCI6614 Data Manual and other documentation for an explanation of the Smart-Reflex® control.

Figure 4.1 shows that the EVM power supplies are a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching

supplies are implemented for larger loads. The switching supplies are listed below followed by explanations of critical component selection:

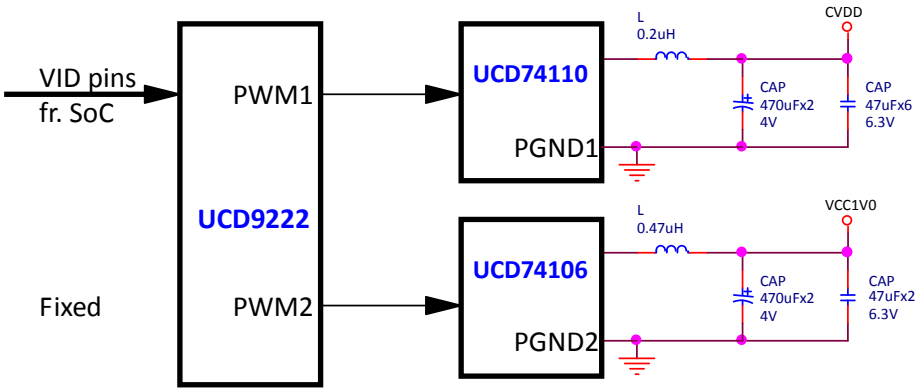
- CVDD (AVS core power for TMS320TCI6614)
- VCC1V0 (1.0V fixed core power for TMS320TCI6614)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC1V5 (1.5V DDR3 power for TMS320TCI6614 and DDR3 memories)
- VCC5 (5.0V power for the XDS520V2 mezzanine card)

The **CVDD** and **VCC1V0** power rails are regulated by TI Smart-Reflex controller UCD9222 and the synchronous-buck power driver UCD74110 and UCD74106 to supply SoC AVS core and CVDD1 core power.

The **VCC3V3_AUX** and **VCC1V5** power rails are regulated by two TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources and the SoC DDR3 EMIF and DDR3 memory chips respectively.

The **VCC5** power rail is regulated by TI 2A Step Down SWIFT™ DC/DC Converter, TPS54231, to supply the power of the XDS560V2 mezzanine card on TMDXEVM6614LXE.

The high level diagrams and output components are shown in figure 4.2, figure 4.3, figure 4.4 and figure 4.5 as well as choosing the proper inductors and buck capacitors.



Inductor for VCC1V0
L : 0.47 uH

Output capacitors for VCC1V0

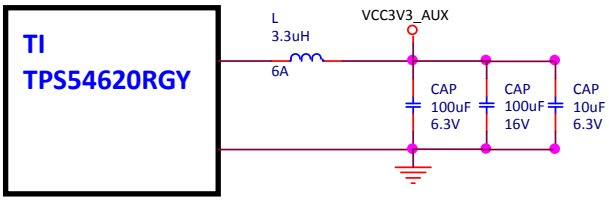
C : 470uF / 4V x 2 +
47uF / 6.3V x 2

Inductor for CVDD
L : 0.2 uH

Output capacitors for VCC1V0

C : 470uF / 4V x 2 +
47uF / 6.3V x 6

Figure 4.2: The CVDD and VCC1V0 (CVDD1) power design on TMDXEVM6614LXE EVM



(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

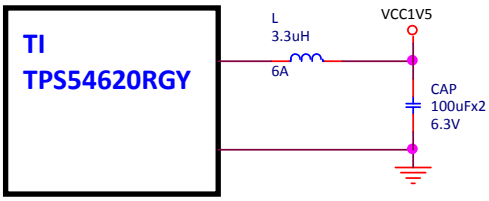
Output capacitor Calculation

Cout> (2 x delta(Iout))/(Fsw x delta(Vout))
Cout> (2 x 3)/(840KHz x 0.0825)
Cout> (6)/(69300)
Cout>87uF
Reference Capacitor : 100uF X2
10uF X1

Inductor Calculation

L = ((Vin(max) - Vout)/Iout x Kind)) x (Vout/(Vin(max) x Fsw))
L = ((12.6 - 3.3)/ 3 x Kind) x (3.3 / (12 x 840KHz))
L = ((8.7/3 x 0.3) x (3.3 / (10.08M))
L = (9.67) x (0.33u)
L ~ 3.2uH
Reference Inductor 3.3uH

Figure 4.3: The VCC3_AUX power esign on TMDXEVM6614LXE EVM



(Over all tolerance is 5% ,DC tolerance is 2.5%)

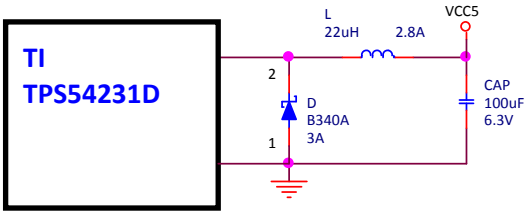
Output capacitor Calculation

Cout> (2 x delta(Iout))/(Fsw x delta(Vout))
Cout> (2 x 2.5)/(840KHz x 0.0375)
Cout> (5)/(31500)
Cout> 159uF
Reference Capacitor : 100uF x 2

Inductor Calculation (KIND=0.3)

L = ((Vin(max) - Vout)/Iout x Kind)) x (Vout/(Vin(max) x Fsw))
L = ((12 - 1.5)/2.5 x Kind) x (1.5 / (12 x 840KHz))
L = ((10.5/2.5 x 0.3) x (1.5 / (10.08M))
L = (10.51/0.75) x (0.1488M)
L = 2.09uH
Reference Inductor 3.3uH

Figure 4.4: The VCC1V5 power design on TMDXEVM6614LXE EVM



Output capacitor Calculation

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max})$$

Cout : 1/(2 x 3.14 x 5 x 25K)
Cout : 1.3 uf

Reference Capacitor : 100uF

Inductor Calculation (KIND=0.3)

L : ((Vin(max) - Vout)/Iout x Kind)) x (Vout/(Vin(max) x Fsw))
L : ((12.6 - 5)/1 x Kind) x (5 / (12.7 x 570K))
L : ((7.6/ 0.3) x (5 / (7239K))
L : (25.3) x (0.69M)
L : 17.5uH

Reference Inductor 22uH

Figure 4.5: The VCC5 power design on TMDXEVM6614LXE EVM

4.3 The Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The TMS320TCI6614 SoC requires specific power up and power down sequencing. Figure 4.6 and Figure 4.7 illustrate the correct boot up and down sequence. Table 4.2 provides the timing details for Figure 4.6 and Figure 4.7.

Refer to the TMS320TCI6614 Data Manual for confirmation of specific sequencing and timing requirements.

Step	Power rails	Timing	Descriptions
	Power-Up		
1	VCC12 (AMC Payload power), VCC3V3_AUX, VCC1V8_AUX VCC1V2 VCC5	Auto	When the 12V power supplied to the TMDXEVM6614LXE, the 3.3V, 1.8V and 1.2V supplies to the FPGA power will turn on. The 1.8V outputs on the FPGA to the SoC will be locked (held at ground).

2	VCC2V5	10mS	Turn on VCC2V5 after VCC3V3 stable for 10mS.
3	CVDD (SoC AVS core power)	5mS	Enable the CVDD and VCC1V0, the UCD9222 power rail#1 is for CVDD and go first after both of VCC5 and VCC2V5 are stable for 5mS.
4	VCC1V0 (SoC CVDD1 fixed core power)	5mS	Turn on VCC1V0, the UCD222 power rail#2. The VCC1V0 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9222 configuration file.
5	VCC1V8 (SoC IO power)	5mS	Turn on VCC1V8 after VCC1V0 stable for 5mS.
6	CDCE62005#2/#3 initiations CDCE62002#1 initiations FPGA 1.8V outputs	5mS	Unlock the 1.8V outputs to the SoC from the FPGA and initiate the CDCE62005s and CDCE62002 after VCC1V8 stable for 5mS. De-asserted CDCE62005s and CDCE62002 power down pins (PD#), initial the clock generators.
7	VCC1V5 (SoC DDR3 power)	5mS	Turn on VCC1V5 after initiation of the clock generators for 5mS.
8	VCC0V75	5mS	Turn on VCC0V75 after VCC1V5 stable for 5mS. When VCC1V5 is valid, FPGA will de-assert the power down pin on the ICS557-08, the PCIE clock multiplexer. When the VCC0V75 is valid, FPGA will enable the ICS557-08 clock outputs by the OE# pin on it.
9	RESETz Other reset and NMI pins	5mS	De-asserted RESETz and unlock other reset and NMI pins for the SoC after VCC0V75 stable and 3 clock generators' PLLs locked for 5mS. In the meanwhile, the FPGA will driving the boot configurations to the SoC GPIO pins.
10	PORz	5mS	De-asserted PORz after RESETz de-asserted for 5mS.
11	RESETFULLz	5mS	De-asserted RESETFULLz after PORz de-asserted for 5mS.
12	SoC GPIO pins for boot configurations	1mS	Release the SoC GPIO pins after RESETFULLz de-asserted for 1mS

	Power-Down		
13	RESETFULLz PORz	0mS	If there is any power failure events or the AMC payload power off, the FPGA will assert the RESETFULLz and PORz signals to the SoC.
14	FPGA 1.8V outputs to SoC CDCE62005 and CDCE62002 PDz pins	5mS	Locked 1.8V output pins on the FPGA and pull the CDCE62005 and CDCE62002 PDz pins to low to disable the SoC clocks.
15	CVDD VCC1V0 VCC1V8 VCC1V5 VCC0V75 VCC2V5 ICS557-08 PD# and OE#	0mS	Turn off all main power rails.

Table 4.2: The power-up and down timing on the TMDXEVM6614LXE

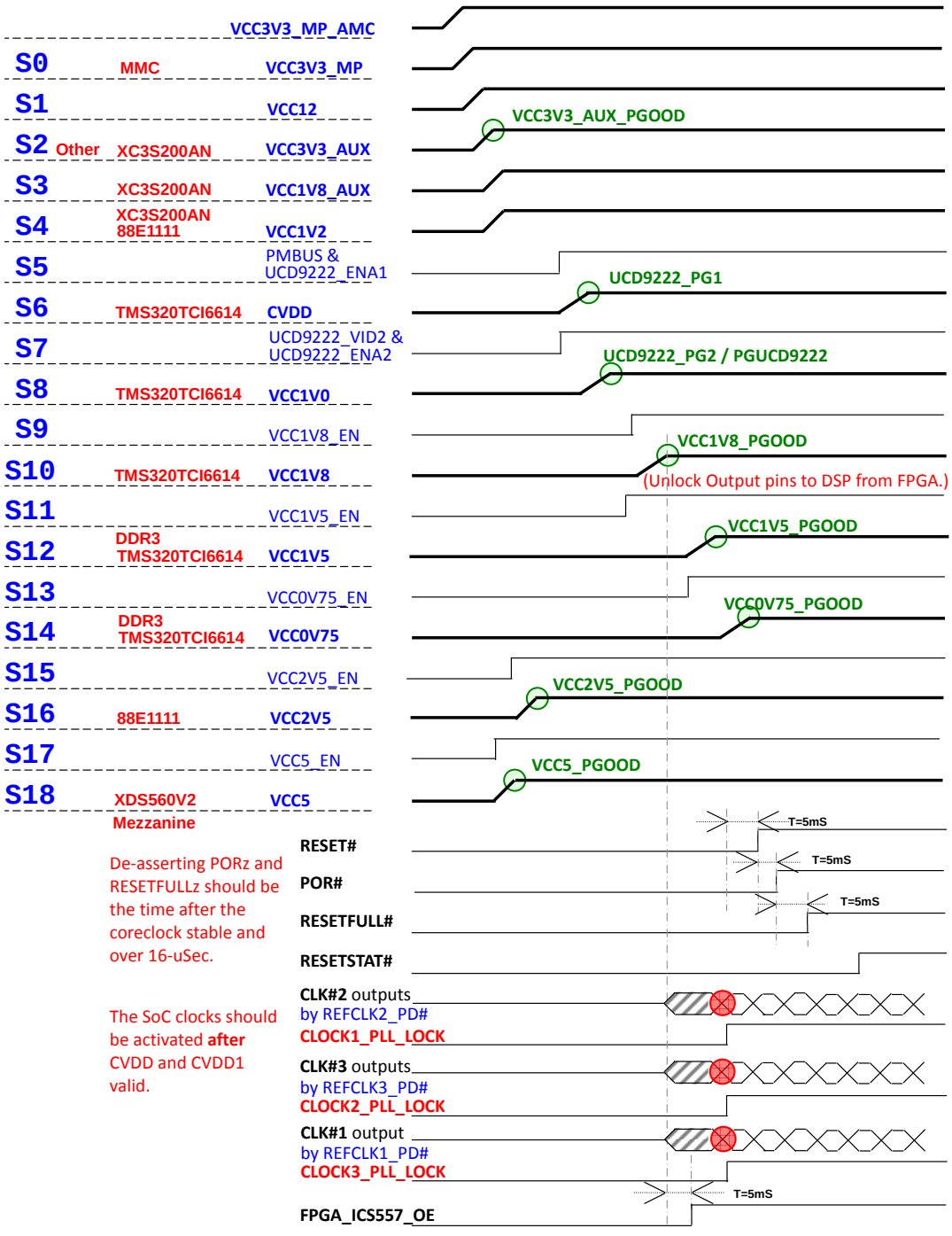


Figure 4.6: Initial Power-on Sequence Timing Diagram

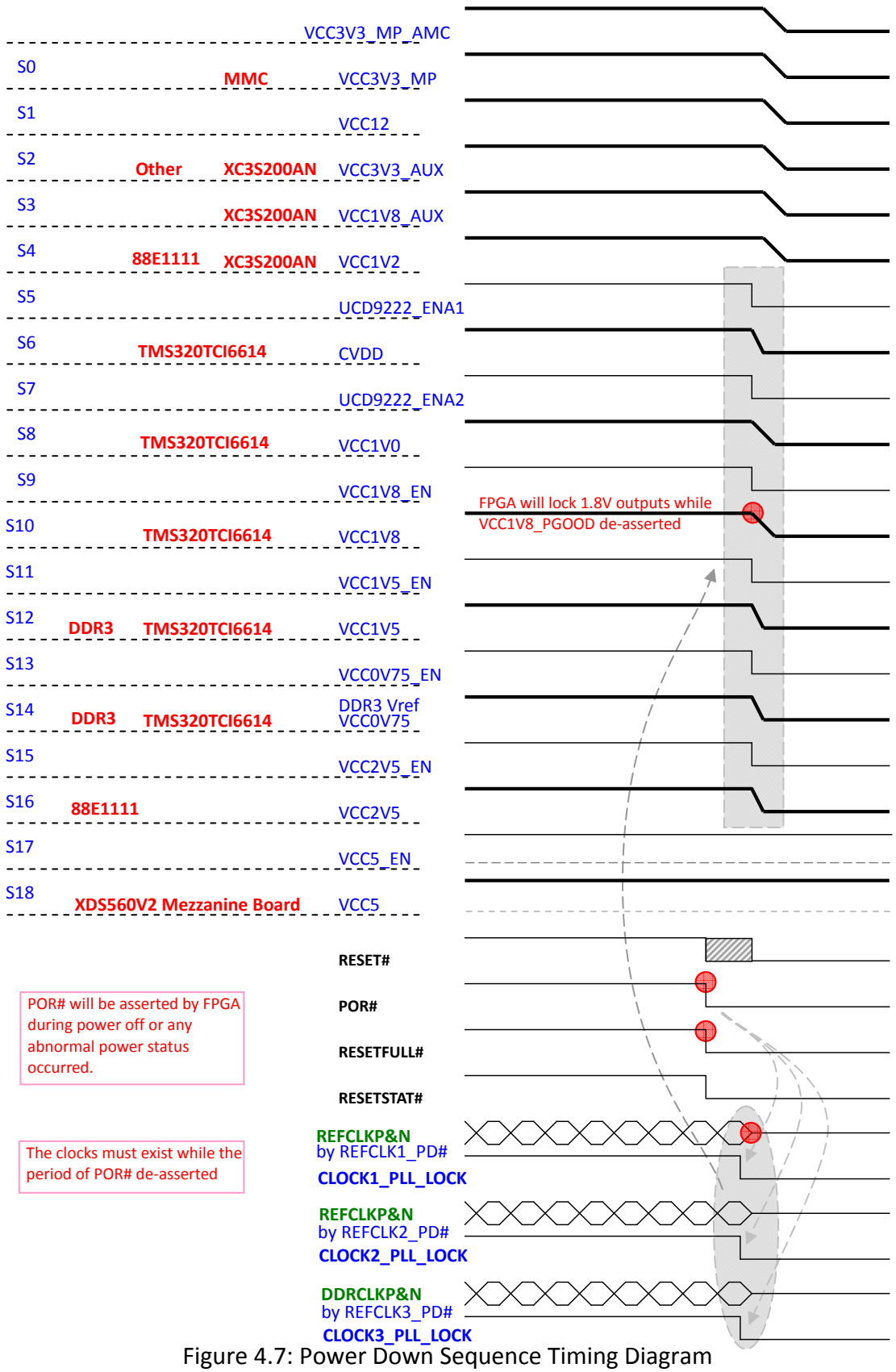


Figure 4.7: Power Down Sequence Timing Diagram

5. TMDXEVM6614LXE FPGA FUNCTIONAL DESCRIPTION

This chapter contains,

5.1 FPGA overview

5.2 FPGA signals description

5.3 FPGA memory map

5.4 Sequence of operation

5.5 Reset definition

5.6 SPI protocol

5.7 CDCE62005 / 62002 Programming Descriptions

5.8 CDCE62005 / 62002 Programming Sequence

5.9 CDCE62005 / 62002 programming register value

5.10 FPGA configuration registers

5.1 FPGA overview

The FPGA (Xilinx XC3S200AN) controls the power sequencing, reset mechanism, SoC boot mode configuration, DAC module control and clock initialization. The FPGA also provides LED control, PACLKSEL switch, GPS module synchronization, and one user switch.

FPGA also supports 4 user LEDs and 1 user switch through control registers. All the FPGA registers are accessible by the TMS320TCI6614 SoC.

5.1.1 FPGA Key Features

The key features of the TMS320TCI6614 EVM FPGA are:

- TMS320TCI6614 EVM Power Sequence Control
- TMS320TCI6614 EVM Reset Mechanism Control
- TMS320TCI6614 EVM Clock Generator Initialization and Control
- TMS320TCI6614 SoC SPI Interface for Accessing the FPGA Configurable Registers
- Provides Shadow Registers for TMS320TCI6614 SoC to Access the Clock Generator Configurations Registers

- Provides TMS320TCI6614 SoC Boot Mode Configuration Strapping
- MMC Reset Events Initiation Interface
- Provide Ethernet PHY Interrupt(RFU) and Reset Control Interface
- Provides Reset Buttons, User Switches, PACLKSEL Switch and Debug LEDs Functions
- Provide SoC synchronization for GPS module
- Provide DAC7611 control
- FPGA Device and Packaging
  - XILINX XC3S200AN FPGA
  - 256 Ball ftBGA (17x17 mm), 1.0 mm pitch

5.2 FPGA signals description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. Throughout this manual, a '#' or 'Z' will be used at the end of a signal name to indicate that the active, or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type.

I	Input pin
O	Output pin
I/O	Bi-directional pin
Differential	Differential Pair pins

.

Table 5.1 : TMDXEVM6614LXE EVM FPGA Pin Description

Pin Name	IO Type	Description
MMC Control :		
MMC_DETECT#	I Internal Pull-Up	**MMC Detection on the insertion to an AMC Chassis :** This signal is an insertion indication from the MMC. The MMC will drive logic low state when the EVM module is inserted into an AMC chassis.
MMC_RESETSTAT#	O	**RESETSTAT# state to MMC :** The FPGA will drive the same status of the SoC RESETSTAT# to the MMC via this signal.

Pin Name	IO Type	Description
MMC_POR_IN_AMC#	I Internal Pull-Up	**MMC POR Request** : This signal is used by the MMC to request a power on reset sequence to SoC. A logic Low to High transition on this signal will complete the FPGA POR sequence with a specified delay time.
MMC_WR_AMC#	I Internal Pull-Up	**MMC WARM Request** : This signal is used by the MMC to initiate a warm reset request. A logic Low to High transition on this signal will complete the FPGA warm reset sequence with a specified delay time.
MMC_BOOTCOMPLETE	O	**BOOTCOMPLETE state to MMC :** The FPGA will drive the same status of the SoC BOOTCOMPLETE to the MMC via this signal.
MMC_SPI_SCK	O	**SPI Serial Clock :** This signal is connected to the TI MSP430 UCA1CLK pin. The FPGA SPI bus clocks data in and out on the rising edge of MMC_SPI_SCK. Data transitions therefore occur on the falling edge of the clock.
MMC_SPI_STE	O	**SPI Chip Select Enable :** This signal is connected to the TI MSP430 UCA1STE pin. The falling edge of the pin initiates a transfer. If MMC_SPI_STE is high, no data transfer can take place.
MMC_SPI_MISO	I Internal Pull-Up	**SPI Serial Data MISO :** This signal is connected to the TI MSP430 UCA1SOMI pin. This signal is used for the serial data transfers from the slave (MMC) output to the master (FPGA) input.
MMC_SPI_MOSI	O	**SPI Serial Data MOSI :** This signal is connected to the TI MSP430 UCA1MISO pin. This signal is used for serial data transfers from the master (FPGA) output to the slave (MMC) input.
Power Sequences Control :		

Pin Name	IO Type	Description
VCC5_PGOOD	I	**5V Voltage Power Good Indication :** This signal indicates the 5V power is valid.
VCC2P5_PGOOD	I	**2.5V Voltage Power Good Indication :** This signal indicates the 2.5V power is valid.
VCC3_AUX_PGOOD	I	**3.3V Auxiliary Voltage Power Good Indication :** This signal indicates the 3.3V auxiliary power is valid.
VCC0P75_PGOOD	I	**0.75V Voltage Power Good Indication :** This signal indicates the 0.75V auxiliary power is valid.
VCC1P5_PGOOD	I	**1.5V Voltage Power Good Indication :** This signal indicates the 1.5V power is valid.
VCC1P8_PGOOD	I	**1.8V Voltage Power Good Indication :** This signal indicates the 1.8V power is valid.
SYS_PGOOD	O	**System Power Good Indication :** This signal is indicated by the FPGA to the system other logics when all the powers are valid.
VCC1P8_EN1	O	**1.8V Voltage Power Supply Enable :** VCC1P8_EN1 is for 1.8V power plane control.
VCC0P75_EN	O	**0.75V Voltage Power Supply Enable :** VCC0P75_EN is for 0.75V power plane control.
VCC2P5_EN	O	**2.5V Voltage Power Supply Enable :** VCC2P5_EN is for 2.5V power plane control.
VCC_5V_EN	O	**5V Voltage Power Supply Enable :** VCC_5V_EN is for 5V power plane control.
VCC1P5_EN	O	**1.5V Voltage Power Supply Enable :** VCC1P5_EN is for 1.5V power plane control.
CLOCK Configurations :		

Pin Name	IO Type	Description
CLOCK[1:3]_SSPCS1	O	**SPI Chip Select Enable :** This signal is connected to the TI 62005 & 62002 CLOCK Generators SPI_LE pin. The falling edge of the SSPCS1 initiates a transfer. If SSPCS1 is high, no data transfer can take place.
CLOCK[1:3]_SSPCK	O	**SPI Serial Clock :** This signal is connected to the TI 62005 & 62002 CLOCK Generators SPI_CLK pin. The FPGA SPI bus clocks data in and out on the rising edge of SSPCK. Data transitions therefore occur on the falling edge of the clock.
CLOCK[1:3]_SSPSI	O	**SPI Serial Data MOSI :** This signal is connected to the TI 62005 & 62002 CLOCK Generators MOSI pin. This signal is used for serial data transfers from the master (FPGA) output to the slave (62005) input.
CLOCK[1:3]_SSPSO	I Internal Pull-Up	**SPI Serial Data MISO :** This signal is connected to the TI 62005 & 62002 CLOCK Generators MISO pin. This signal is used for the serial data transfers from the slave (62005) output to the master (FPGA) input.
REFCLK[1:3]_PD#	O	**TI 62005/62002 CLOCK Generators Power Down** : The power down pin places the CDCE62005 / 62002 into the power down state.
UCD9222 Interface :		
UCD9222_PG1	I Internal Pull-Up	**UCD9222 Power Good Indication for CVDD SoC Core Power :** This signal indicates the CVDD SoC core power is valid.
UCD9222_ENA1	O	**UCD9222 Enable for CVDD SoC Core Power :** UCD9222_ENA1 is for CVDD SoC core power plane control.

Pin Name	IO Type	Description
UCD9222_PG2	I Internal Pull-Up	**UCD9222 Power Good Indication for VCC1V0 SoC Core Power :** This signal indicates the VCC1V0 SoC core power is valid.
UCD9222_ENA2	O	**UCD9222 Enable for VCC1V0 SoC Core Power :** UCD9222_ENA2 is for VCC1V0 SoC core power plane control.
PGUCD9222	I	**UCD9222 Power Good Indication for SoC Core Power :** This signal indicates both the CVDD SoC and VCC1V0 SoC core powers are valid.
UCD9222_RST#	O	**UCD9222 Reset :** An active low signal will reset the UCD9222 device.
PHY Interface :		
PHY_INT#	I	**Interrupt Request from 88E111 PHY**
PHY_RST#	O	**Reset to 88E111 PHY :** This signal is used to reset the 82E111 PHY device. The PHY_RST# will be asserted during the active SoC_PORZ or SoC_RESETFULLZ period. The PHY_RST# logic also can be configured by the SoC accessed register.
SoC SPI :		
SoC_SSPCS1	I	**SoC SPI Chip Select 1 :** This signal is connected to the TMDXEVM6614LXE SoC SPISCS1 pin. The falling edge of the SSPCS1 from the SoC will initiate a transfer. If SSPCS1 is high, no data transfer can take place.
FPGA_SSPCK	I	**SoC SPI Serial Clock :** This signal is connected to the TMDXEVM6614LXE SoC SPICLK pin. The FPGA SPI bus clocks data in on the falling edge of SSPCK. Data transitions therefore occur on the rising edge of the clock.

Pin Name	IO Type	Description
NOR_SSPMISO	O	**SoC SPI Serial Data MISO :** This signal is connected to the TMDXEVM6614LXE SoC SPIDIN pin. This signal is used for serial data transfers from the slave (FPGA) output to the master (SoC) input in the SoC_SSPCS1 asserted period.
NOR_SSPMOSI	I	**SoC SPI Serial Data MOSI :** This signal is connected to the SoC SPIDOUT pin. This signal is used for serial data transfers from the master (SoC) output to the slave (FPGA) input.
RESET Buttons and Requests :		
FULL_RESET	I	**Full Reset Button Input :** This button input is used to initiate a Full Reset event.
WARM_RESET	I	**Warm Reset Button Input :** This button input is used to initiate a Warm Reset event.
TRGRSTZ	I	**Reset Request from the SoC Emulator Header :** A RESET sequence will be initiated if an active TRGRSTZ event is recognized by the FPGA.
SoC Boot & Device configurations :		
BM_GPIO[0 : 16]	I	**SoC Boot Mode Strap Configurations:** These switches inputs are used to drive the SoC boot mode strap configurations during the EVM power up period.
SoC_GPIO[0 : 16]	I/O	**SoC GPIO:** In normal operation mode, these signals will input polarity for the recognition of the SoC GPO pins. During the EVM power on or PORZ/RESETFULLZ asserted period, the FPGA will output the BM_GPIO switches value to the SoC for SoC boot mode configuration strapping.
SoC RESET & Interrupts Control :		
SoC_CORESEL[0:2]	O	**SoC Core Selection Bit**
SoC_PACLKSEL	O	**SoC PACLKSEL :** This pin is used for the SoC PA clock selection setting.

Pin Name	IO Type	Description
FPGA_SoCCLKSEL	O	**CORECLKSEL :** Core Clock Select to select between SYSCLK and ALTCORECCLK to the Main PLL
FPGA_EXTFRAMEEVENT	I	**EXTFRAMEEVENT :** SoC Frame Sync Clock Output
SoC_LRESETNMIENZ	O	**SoC Local Reset and NMI Enable.**
SoC_NMIZ	O	**SoC NMI.**
SoC_LRESETZ	O	**SoC Local Reset.**
SoC_HOUT	I	**SoC HOUT**
SoC_BOOTCOMPLETE	I	**SoC Boot Complete Indication**
SoC_SYSCLKOUT	I	**SoC System Clock Output**
SoC_PORZ	O	**SoC Power On Reset**
SoC_RESETFULLZ	O	**SoC Full Reset.**
SoC_RESETZ	O	**SoC Reset**
SoC TDM CLK :		
TCLKA/B[p/n]	I, Differential	**TCLKA/B Different Clock Input Pairs**
TCLKC/D[p/n]	I, Differential	**TCLKC/D Different Clock Input Pairs**
DEBUG LED:		
DEBUG_LED[0:3]	O	**Debug LED :** The LEDs are used for debugging purposes only.
Miscellaneous : (RFU, Reserved for Future Use)		
MAIN_48MHZ_CLK_R	I	**FPGA Main Clock Source :** A 48 MHz clock is used as the FPGA main clock source.
SoC_TIMI0	O	**SoC Time 0 Clock :** The FPGA drives high impedances on SoC_TIMI0 pin during the runtime. During the EVM power on or PORZ/RESETFULLZ asserted period, the FPGA will drive the PCIESSEN switch state to SoC for the boot configuration strapping.
SoC_TIMI1	O	**SoC Time1 Clock :** The FPGA drives high impedances on SoC_TIMI1.
SoC_TIMO0(RFU)	I	**SoC Time 0 Clock :**
SoC_TIMO1(RFU)	I	**SoC Time1 Clock :**
SoC_VCL_FPGA (RFU)	I	**SoC Smart Reflex I2C Clock**
SoC_VD_FPGA (RFU)	I/O	**SoC Smart Reflex I2C DATA**

Pin Name	IO Type	Description
PCA9306_EN	O	**PCA9306 Enable:** This signal is used to enable the SoC Smart Reflex I2C buffer function.
NAND_WP#	O	**NAND Flash Write Protect:** This signal is used to control the NAND flash write-protected function.
NOR_WP#	O	**NOR Flash Write Protect:** This signal is used to control the NOR flash write-protected function.
EEPROM_WP	O	**EEPROM Write Protect:** This signal is used to control the EEPROM write-protected function.
PCIESSEN	I	**PCIE Subsystem Enable:** This is used for the PCIESSEN switch input.
USER_DEFINE	I	**User Define Switch:** This is reserved for the user defined switch input.
FPGA_PACLKSEL	I	**FPGA PACLKSEL Switch:** This is used for the FPGA_PACLKSEL switch input.
FPGA JTAG :		
JTAG_FPGA_TCK	I	**FPGA JTAG Clock Input**
JTAG_FPGA_TDI	I	**FPGA JTAG Data Input**
JTAG_FPGA_TDO	O	**FPGA JTAG Data Output**
JTAG_FPGA_TMS	I	**FPGA JTAG Mode Select Input**
ICS 557 MUX Control:		
FPGA_ICS557_SEL	O	**ICS557 Clock Selection:** The selection pin is used to choose clock source. CLK MUX control pin is controlled by switch GPIO7 before power-up sequence is finished. CLK SEL pin is controlled by register setting after power-up sequence is finished.
FPGA_ICS557_PD#	O	**ICS557 Power Down**: The power down pin places the ICS557 into the power down state.
FPGA_ICS557_OE	O	**ICS557 Output Enable:** The pin is used to enable output.
Level Shift Control:		

Pin Name	IO Type	Description
VID_OE#	O	**VID Output Enable:** The pin is used to enable level shift component output.
SFP Connector : (RFU, Reserved for Future Use)		
MOD_SDA[0:3](RFU)	I/O	**MOD Data:** A I2C Bus slave device can receive data provided by the master (FPGA), or it can also provide data to the master (FPGA) via this signal line.
MOD_CLK[0:3](RFU)	O	**MOD Clock:** The FPGA provides the clock source on the I2C bus.
RATESELECT(RFU)	O	**Rate Select:** This signal is used to select between full or reduced receiver bandwidth. Now, the signal always keeps to logic low.
TX_DISABLE(RFU)	O	**Transmitter Disable:** The signal is used to shut down the transmitter optical output.
LOS(RFU)	I	**Loss of Signal:** This signal indicates if the received optical power is below the worst-case receiver sensitivity..
TX_FAULT(RFU)	I	**Transmitter Fault:** This signal indicates if the transmitter is fault.
GPS Module Synchronization		
PPS_INTERRUPT	O	**PPS Interrupt:** This signal is used to bypass PPS signal to SoC when FPGA receive the PPS signal and is stable and valid.
FPGA_SYNC	O	**FPGA SYNC:** This signal is used to transmit one 362 nsec width pulse to SoC at a specified free-running 32 bit counter value. (Note1: Sysclk_period=1/122.8Mhz=8.143 nsec Note2: 362nsec > 24*sysclk_period = 195.43nsec)
BUFCLK_FPGA	I	**BUFFER Clock Source:** A 19.2 MHz clock is used as the GPS synchronization module main clock source.

Pin Name	IO Type	Description
FPGA_TIMI0	I	**FPGA TIME 0:** The pin is connected with GPS pulse per second (PPS) pin.
DAC 7611 Control		
DAC_CLR_np	O	**Clear DAC Register:** This signal is used to clear the DAC7611 register.
DAC_LD_np	O	**Load DAC Register:** This signal is used to control the internal DAC7611 register load function.
Board Version		
BID[0:1]	I	**Board ID**: The board ID pins provided PCB version.
The others unused IO pin		
The others unused IO pin	I	The pins are floating.

5.3 FPGA Memory Map

Table 5.2 : TMS320TCI6614 EVM FPGA Memory Map

Memory Map Base Address	Memory Map Offset Address	Memory
SoC SPI Chip Select 1 0x20BF0000-0x20BF03FF (TMS320TCI6614 SoC SPI Memory Map Address)	0x00-0x6F	Configuration Registers

5.4 Sequence of operation

This section describes the FPGA sequence of operation on the EVM. It contains:

5.4.1 Power On Sequence

5.4.2 Power Off Sequence

5.4.3 Boot Configuration Timing

5.4.1 Power On Sequence

The following section provides details of the FPGA Power-on sequence of operation.

1. After applying the +12V from either AMC edge connector or the DC-IN connector, the Point of Load supplies (POLs) of VCC3V3_AUX, VCC1V8_AUX and VCC1V2 rail on the EVM start automatically. The FPGA begins for the Power-on sequence of operation when VCC3_AUX_PGOOD asserted.
2. The 5V power is enabled first by the FPGA, then it waits for 10 ms and then it enables the 2.5V power rail.
3. Once the 5V and 2.5V voltages (VCC5_PGOOD and VCC2P5_PGOOD) are valid, wait for 5 ms, the FPGA asserts UCD9222_ENA1 and UCD9222_ENA2 signals simultaneously to enable the CVDD and VCC1V0 DSP core power. The UCD9222 configuration begins ramping CVDD immediately and it waits 5ms before it begins ramping VCC1V0.
4. After both the UCD9222_PG1 and UCD9222_PG2 are valid, wait for 5 ms, the FPGA enables the 1.8V power.
5. After the 1.8V voltage (VCC1P8_PGOOD) is valid, wait for 5 ms, the FPGA initializes the CDCE62005 clock generator#2 and CDCE62005 clock generator#3. Wait for 1 ms after the PLL_LOCK pins asserted on CDCE62005 clock generator#2 and generator#3, then the FPGA initializes CDCE62002 clock generator#1. Wait for 1 ms after initializations of CDCE62002, the FPGA enables the 1.5V power controller.
6. Wait for 5 ms after the 1.5V power rail valid (VCC1V5_PGOOD asserted), the FPGA enables the 0.75V power, level translators (I/O pins for TMS320TCI6614) and ICS557-08, the PCIe clock multiplexor.
7. Wait for 5 ms after the 0.75V voltage valid (VCC0V75_PGOOD asserted), the FPGA removes the states of DSP_RESETz, DSP_LRESETz and other I/O pins of TMS320TCI6614 except **DSP_PORz and DSP_RESETFULLz**.
8. Wait for 5ms after de-asserting the DSP_RESETz, DSP_LRESETz and other I/O pins of TMS320TCI6614, the FPGA checks the PLL locked bits in three clock generators to make sure all clock outputs are stable, If all PLL locked bits are set, there are some tasks the FPGA will do.
   8.1 The FPGA de-asserts the DSP_PORz and keeps the DSP_RESETFULLz asserted.
   8.2 Wait for another 5 ms, the FPGA de-asserts the DSP_RESETFULLz.
   8.3 The FPGA drives the GPIO pins for the DSP boot configuration from the settings of the BM_GPIO switches during the period starting when VCC0P75_PGOOD becomes valid until 1mS after RESETSTAT# becomes inactive.
   8.4 The FPGA also drives DSP_TIMI0 based on the PCIESSEN switch setting to enable / disable PCIe subsystem of the DSP during the time of the boot configurations.
9. The EVM Power-on sequence is completed if DSP_RESETSTAT# de-asserted after the DSP_RESETFULLz removed.

10. The LEDs on the board can be checked to validate successful power-up. These also indicate the power-up state if the board fails to start-up and also indicates failure if a supply fault is detected after a completed start-up.

    10.1 After the Power-up sequence, the FPGA lights the Power Good LED to indicate that all power rails are valid and all LVDS clock outputs from the clock generators are available.

    10.2 During the Power-on period, the FPGA reports the sequencing "state" and then holds the current value if the sequence stalls before completion. This will be because one of the power rails did not power-up properly or one of the clocks cannot lock after being enabled.

    10.3 If a power failure is detected after a proper and completed power-up sequence; the FPGA turns off the DSP power rails, the clock outputs, the Power Good LED and flashes the FPGA_D[1:4] LEDs. This will prevent damage to the DSP. The FPGA does not control the power rails of VCC1V2, VCC1V8_AUX, VCC3V3 and VCC5 because they are for the FPGA and support circuitry and the XDS560V2 mezzanine card.

Below table shows the power states of the indicators during EVM power-on.

Table 5.3: The LED states for Power-on Sequence

LED4	LED3	LED2	LED1	SysPG	State	Note	
@	@	@	@	@	Idle	System Ready for Power On	Power Up
@	@	@	@	@	V2P5	Enable 5V and 2.5V; Check 5V & 2.5V power-good	Power Up
@	@	@	@	@	PMBS	Enable UCD9222-enable1	Power Up
@	@	@	@	@	PMB2	Enable UCD9222-enable2; Check UCD9222_pg1, UCD9222_pg2 and pgUCD9222	Power Up
@	@	@	@	@	V1P8	Enable 1.8V; Check 1.8V power-good; 62002 CLK1 , 62005 CLK2 & CLK3 initialization	Power Up
@	@	@	@	@	V1P5	Enable 1.5V; Check 1.5V power-good	Power Up
@	@	@	@	@	V075	Enable 0.75V; Check 0.75V power-good	Power Up
@	@	@	@	@	CLKG	De-assert RESET#; Check62002 CLK1 PLL Lock, 62005 CLK2 & CLK3 PLL Lock	Power Up
@	@	@	@	@	PORWR	De-assert POR#	Power Up
@	@	@	@	@	WAIT	De-assert RESETFULL#; Check RESETSTAT# de-assertion	Power Up
@	@	@	@	@	ON	Power Up Sequence completed; LEDs will changed to FPGA register set value	ON
@	@	@	@	@	ON	Default FPGA register(08h) value = "0000"; @ = '0', @ = '1'	ON
%	%	%	%	@	ON	The % reflects the FPGA register (08h) value; R/W accessible by the SoC through the SoC-FPGA SPI interface	ON

Below table shows the power states of the indicators after a proper and completed power-up sequence.

Table 5.4: The LED states for Power Failure

LED4	LED3	LED2	LED1	SysPG	State	Note	
@	@	**PGS1**	**PGS0**	@	Power Fail	PGS0 : Last recorded “ucd9222_pg1” status before the power failure occurred PGS1 : Last recorded “ucd9222_pg2” status before the power failure occurred PGSx @ means power good status is ‘1’; PGSx @ means power good status is ‘0’.	Power Fail
@	@	**PGS3**	**PGS2**	@	Power Fail	PGS2 : Last recorded “pgucd9222” status before the power failure occurred PGS3 : Last recorded 0.75v_PG status before the power failure occurred PGSx @ means power good status is ‘1’; PGSx @ means power good status is ‘0’.	Power Fail
@	@	**PGS5**	**PGS4**	@	Power Fail	PGS4 : Last recorded 1.5v_PG” status before the power failure occurred PGS5 : Last recorded 1.8v_PG status before the power failure occurred PGSx @ means power good status is ‘1’; PGSx @ means power good status is ‘0’.	Power Fail
@	@	**PGS7**	**PGS6**	@	Power Fail	PGS6 : Last recorded 2.5v_PG” status before the power failure occurred PGS7 : Last recorded 5v_PG status before the power failure occurred PGSx @ means power good status is ‘1’; PGSx @ means power good status is ‘0’.	Power Fail
*	*	*	*	@		LED2 & LED1 will be function as a free-run counter LED3 = FPGA FW Update SPI CLK LED4 = FPGA FW Update SPI CS#	FPGA Update

5.4.2 Power Off Sequence

Following section provides details of FPGA power off sequence of operation.

1. Once the system powers on, any power failure events (any one of power good signals de-asserted) will trigger the FPGA to proceed to the power off sequence.
2. Once any de-asserted Power Good signals have been detected by the FPGA, the FPGA will assert the DSP_PORz to DSP immediately.
3. Wait for 5 ms, the FPGA will disable all the system power rails , assert all the other DSP resets to DSP, lock the +1.8V output pins from the FPGA to the DSP and also assert power down signals to the CDCE62005 and the CDCE62002 clock generators.
4. FPGA remains in the power failure state until main 12V power is removed and restored.

5.4.3 Boot Configuration Timing

The boot configuration timing of the power-up and the RESETFULLz event are shown below.

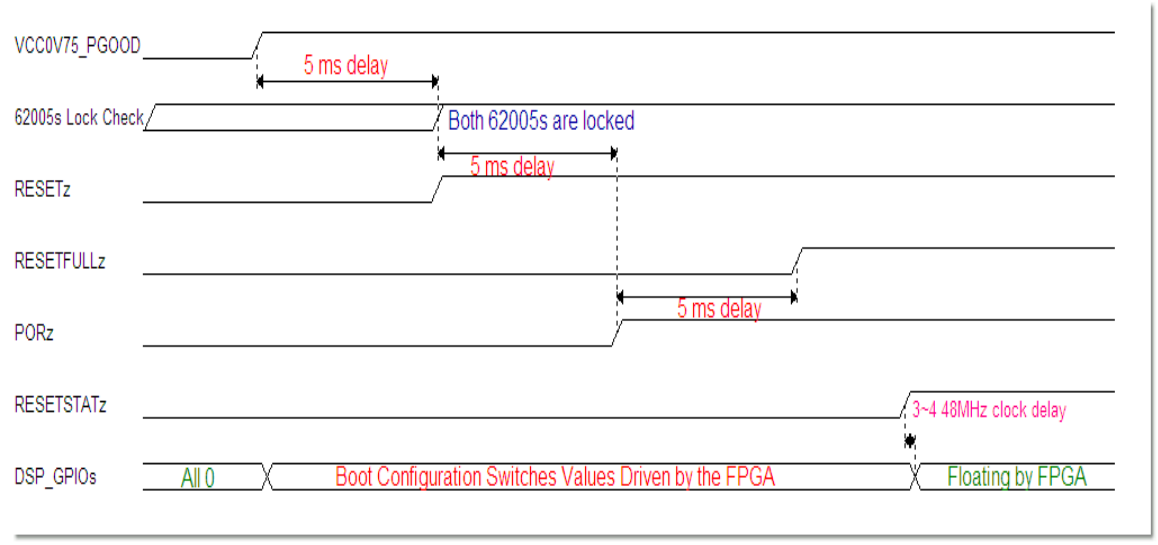


Figure: 5-1 Power-on Reset Boot Configuration Timing

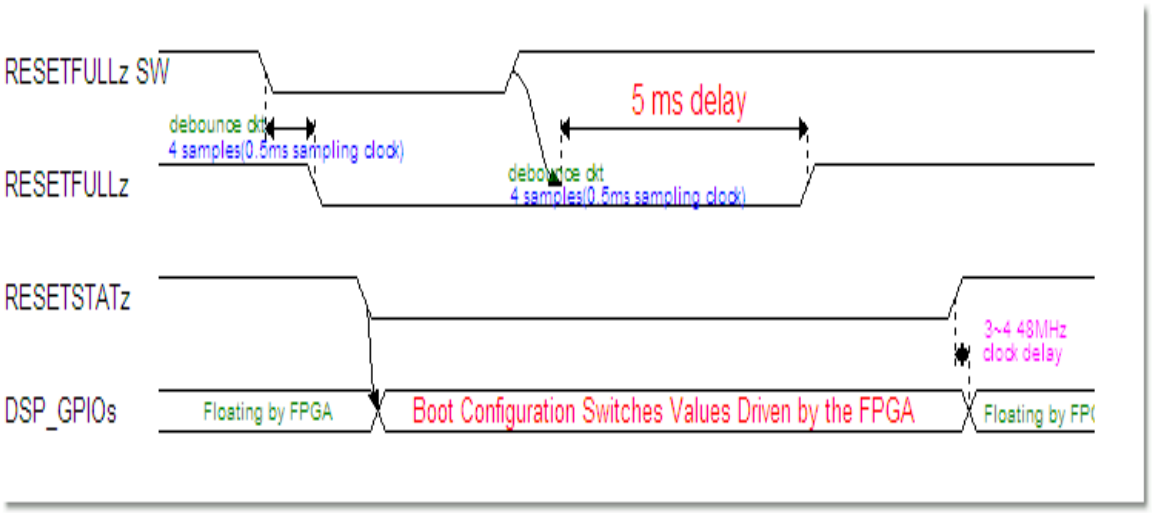


Figure: 5-2 Reset-Full Switch/Trigger Boot Configuration Timing

5.5 Reset definition

5.5.1 Reset Behavior

Power-On : The Power-On behavior includes initiating and sequencing the power sources, clock sources and then SoC startup. Please refer to the section 5.5.1 for detailed sequence and operations.

Full Reset : The RESETFULLz is asserted low to the SoC. This causes RESETSTAT# to go low which triggers the boot configuration to be driven from the FPGA. Reset to the Marvell PHY is also asserted. POR# and RESET# to the SoC remain high. The power supplies and clocks operate without interruption. Please refer to the section 5.5.3 for detailed timing diagrams.

Warm Reset : The RESETz is asserted low to the SoC. The PORz and RESETFULLz to the SoC remain high. The power supplies and clocks operate without interruption.

5.5.2 Reset Switches and Triggers

FULL_RESET – a logic low state with a low to high transition will trigger a Full Reset behavior event.

WARM_RESET – a logic low state with a low to high transition will trigger a warm reset behavior event.

MMC_POR_IN_AMC# - a logic low state with a low to high transition will trigger a Full Reset behavior event.

MMC_WR_AMC# - a logic low state with a low to high transition will trigger a warm reset behavior event.

TRGRSTz - a logic low state with a low to high transition on the Target Reset signal from emulation header that will trigger a warm reset behavior event.

FPGA_JTAG_RST# - not used in current implementation.

5.6 SPI protocol

This section describes the FPGA SPI bus protocol design specification for interfacing with TMDXEVM6614LXE SoC and CDCE62005 / 62002 clock generators. It contains:

5.6.1 FPGA-SoC SPI Protocol

5.6.2 FPGA-CEDC62005/62002(Clock Generator) SPI Protocol

5.6.1 FPGA-SoC SPI Protocol

The FPGA supports the simple write and read commands for the TMS320TCI6614 to access the FPGA configuration registers through the SPI interface. The FPGA SPI bus clocks data in on the falling edge of SoC SPI Clock. Data transitions therefore occur on the rising edge of the clock.

The figures below illustrate a SoC to FPGA SPI write operation.

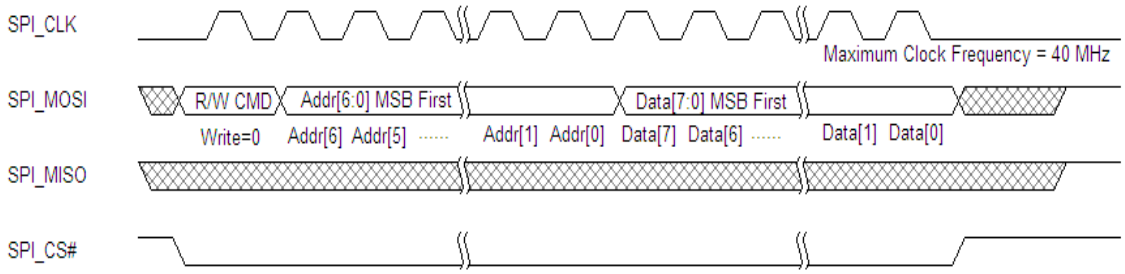


Figure 5-3: The SPI access form the TMS320TCI6614 to the FPGA (WRITE / high level)

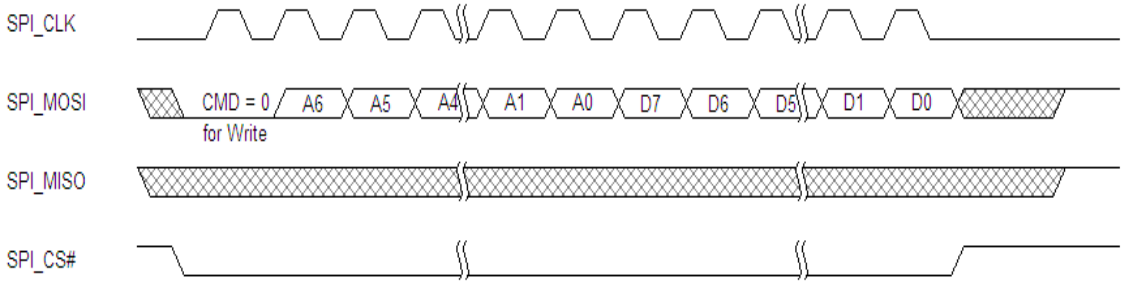


Figure 5-4: The SPI access form the TMS320TCI6614 to the FPGA (WRITE)

The figures below illustrate a SoC to FPGA SPI read operation.

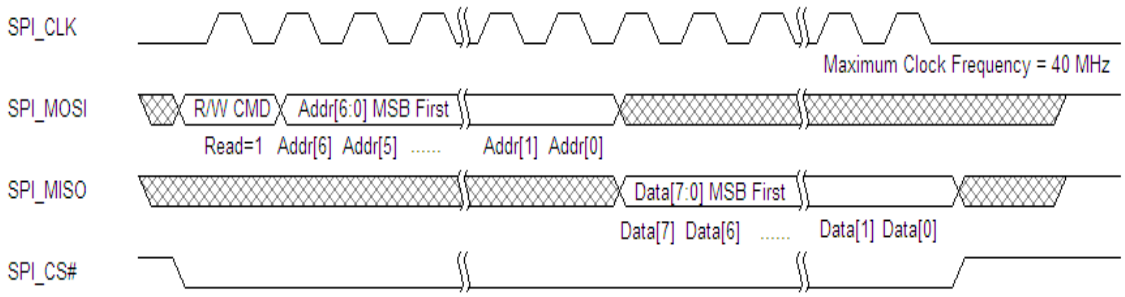


Figure 5-5: The SPI access form the TMS320TCI6614 to the FPGA (READ / high level)

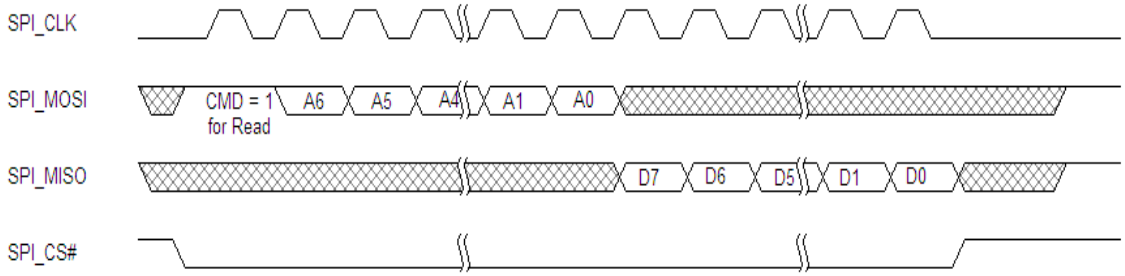


Figure 5-6: The SPI access form the TMS320TCI6614 to the FPGA (READ)

5.6.2 FPGA- CDCE62005 / 62002(Clock Generator) SPI Protocol

The FPGA-Clock Generator SPI interface protocol is compatible to CDCE62005 / 62002 SPI. The FPGA SPI bus clocks data in on the rising edge of SoC SPI Clock. Data transitions therefore occur on the falling edge of the clock.

The figure below illustrates a FPGA to CDCE62005 / 62002 SPI write operation.

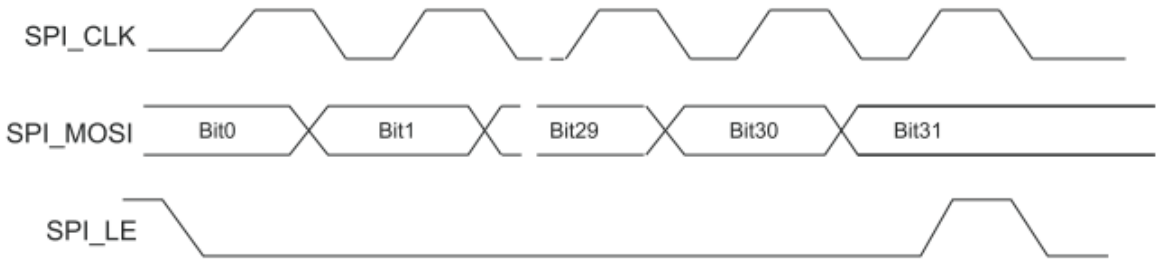


Figure 5-7: The SPI access form the FPGA to the CDCE62005 (WRITE)

The figure below illustrates a FPGA to CDCE62005 / 62002 SPI read operation.

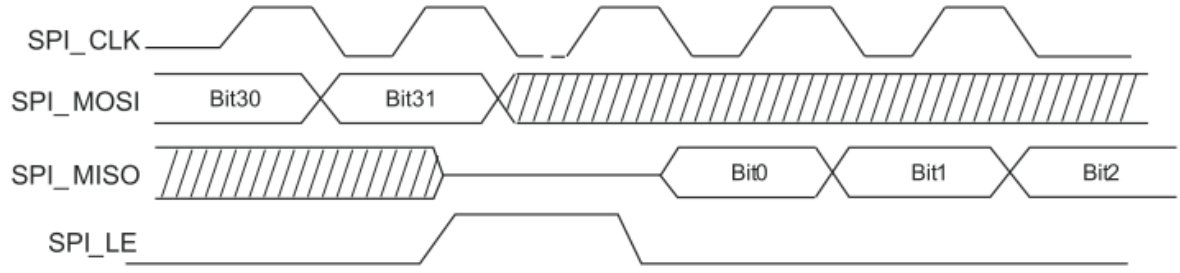


Figure 5-8: The SPI access form the FPGA to the CDCE62005 (READ)

5.7 CDCE62005 / 62002 Programming Descriptions

This section describes how to configure the CDCE62005 clock generators by the SPI interface from the DSP to the FPGA.

- How to configure CDCE62005 for the clock outputs:

Programming sequence of CDCE62005 via the FPGA by the SoC is setting the desire values to the relevant offsets on the FPGA for the settings on the Register[0:7] of CDCE62005 and issues a “start command (send)” by offset 10h on the FPGA to conduct programming sequences to CDCE62005.

There are eight banks (Register[0:7]) inside the FPGA mapping to eight registers of CDCE62005 by the same offsets for the CLK#2 and CLK3. Configuring the Clock Generator#2 (CDCE62005) by the SoC is described as below for example.

The CLK#2 offset on the FPGA are 0x17h (MSB) to 0x14h (LSB), they are including 28-bit data field and 4-bit addr. Field as the same of CDCE62005, user can refer to CDCE62005 specification on TI website for the configuration details.

Offset	Register definitions	Type	Default
0x10h	CLK-GEN 2 Control Register	R/W	0x00h
0x11h	CLK-GEN 2 Interface Clock Setting	R/W	0x03h
0x14h	CLK-GEN 2 Command Byte 0	R/W	0x00h
0x15h	CLK-GEN 2 Command Byte 1	R/W	0x00h
0x16h	CLK-GEN 2 Command Byte 2	R/W	0x00h
0x17h	CLK-GEN 2 Command Byte 3	R/W	0x00h
0x18h	CLK-GEN 2 Read Data Byte 0	RO	0x00h
0x19h	CLK-GEN 2 Read Data Byte 1	RO	0x00h
0x1Ah	CLK-GEN 2 Read Data Byte 2	RO	0x00h
0x1Bh	CLK-GEN 2 Read Data Byte 3	RO	0x00h

1. The SoC must set the address number to the offset 0x14h of the FPGA first to indicate the bank for the corresponding register of CDCE62005. After that, the SoC can set the data to the offset 0x17h, 0x16h, 0x15h and 0x14h on the FPGA in sequence for the corresponding register on CDCE62005.

e.g.: User wants to write the 0xEB860300h value to CDCE62005 Registor[0] and 0x69860314h value to CDCE62005 Register[4] on CLK-GEN#2 (refer to CLK2 in the EVM schematics).

a. Check the bits 0 of 'Busy Status' on offset 0x10h to make sure the last progress have been finished.

b. Set address 0x00h to the offset 0x14h, the last 4-bit were set for the Register 0;

c. Set data 0xEBh, 0x86h, 0x03h and 0x00h to the offset 0x17h, 0x16h, 0x15h and 0x14h respectively for the new configurations of the clock output0;

d. Set address 0x04h to the offset 0x14h, the last 4-bit were set for the Register 4;

e. Set data 0x69h, 0x86h, 0x03h and 0x14h to the offset 0x17h, 0x16h, 0x15h and 0x14h respectively for the new configurations of the clock output4;

f. The Register 0 and Register 4 on the FPGA for CLK-GEN#2 are updated by the SoC.

g. Please note that the default values in the Register[0:7] are the same of values initialized during power-on phase.

2. The SoC sets offset 0x10h bit 0 on the FPGA to upload the configurations to CDCE62005 (CLK-GEN#2).
    a. The offset 0x10h bit 0 on the FPGA is “initiate/start the data transfer” bit. The FPGA will program the CDCE62005 by the values of the Register[0:7] inside the FPGA via the SPI interface if this bit is set (‘1’).
    b. If any of reset events needed after re-programming the CLK GEN, please set the FPGA offset 0x10h register bits 2, 3, or(and) 4 for DSP_PORz, DSP_RESETFULLz or RESETz. The FPGA will issue the reset events based on the offset 0x10h bit[2:4] after finished CDCE62005 programming.
    c. The SoC could check if the programming process finished by the offset 0x10h bit1 of ‘Busy State’. The ‘1’ on the offset 0x10h bit1 indicates that the FPGA is programming of CDCE62005.
    d. Please note that the SoC is not allowed to start another programming event on the clock generator while its ‘Busy State’ at ‘1’.

- <u>How to read the Register settings on CDCE62005:</u>

The FPGA uses Eh to be a ‘read command’ on offset 0x14h low 4-bit and the value of 0h to 8h to indicate the ‘Register number of CDCE62005’ on offset 0x14h high 4-bit, the allowed value are between 0 to 8.

Reading the value of Register8 on CLK-GEN#2 by the SoC is shown as below for example. The Register[8] on CDCE62005 indicates the status of clock synthesizer. Please note that the offset 0x15h, 0x16h and 0x17h need to be clean to zero before send a reading command.

Set 8Eh to FPGA offset 14h first and clear the offset 15h, 16h and 17h and then issue a start(send) command to the SPI bus. The CDCD62005 data could be read through the FPGA offset 1Bh~18h registers once the SPI protocol is completed.

The detail steps are :

a. The SoC sets value of 8Eh to the FPGA offset 0x14h register

   (8h -> Register 8; Eh -> reading);

b. The SoC clears the FPGA offset 15h, 16h, and 17h registers by 00h;

c. The SoC sets 0x01h to the FPGA offset 10h register (issue the SPI protocol),

   The bit 0 of the offset 0x10h register means “initiate/start the data transfer”.
   The data field on the offset 0x17h-0x14h registers will be sent to the 2nd Clock Generator CDCE62005 via the SPI interface to indicate the reading register number if this bit is set to ‘1’.);

d. SoC checks the FPGA offset 0x10h register bit 1;

The FPGA offset 0x10h register bit1 means “Busy status” and it is used to indicate the CDCE62005 SPI bus status. The SPI bus is busy and a SPI command is processing while this bit is read as ‘1’.

If the FPGA offset 0x10h register bit1 is ‘0’, the related register value of CDCE62005 has ready been read out and stored on the offset 0x1Bh to 0x18h registers of the FPGA.

e. The SoC could read the CDCE62005 register 8 (32 SPI bits = 28 data field bits + 4 address field bits) value through the FPGA offset 0x1Bh~0x18h registers.

f. SoC would be allowed to issue the next CDCE62005 SPI command.

5.8 CDCE62005 / 62002 Programming Sequence

This section describes that FPGA program CDCE62002 / 62005 sequence.

CDCE62002 Programming Sequence

(1) The FPGA initializes and programs all data into necessary CDCE62002 registers.
(2) Wait 2ms after initialization and programming have been completed.
(3) Set CDCE62002 Register #2 bit 13 (PLL_RESET, SPI bit 17) **“0➔1”.**
    - This register bit is currently named “PLLRESET” but will be renamed to “CALSELECT”
(4) Toggle CDCE62002 Register #2 bit 20 (RESERVED, SPI bit 24) **“1➔0➔1”.**
    - This register bit is currently named “RESERVED” but will be renamed to “PLLRESET”
(5) Wait 100uS minimum.
(6) Toggle CDCE62002 Register #2 bit8 (SYNC, SPI bit 12) **“1➔0➔1”.**

CDCE62005 Programming Sequence

(1) The FPGA initializes and programs all data into necessary CDCE62005 registers
(2) Wait 2ms after initialization and programming have been completed.
(3) Set the CDCE62005 Register #6 bit 27 (ENCAL_MODE, SPI bit31) by 1 for manual mode of PLL calibration.
(4) Toggle CDCE62005 Register #6 bit 22 (ENCAL, SPI bit26) **“1➔0➔1”**.

5.9 DCE62005/62002 Programming Register Value

The tables provide CDCE62005 / 62002 programming registers value. FPGA program CDCE62005 / 62002 with the programming register value during power on sequence.

Table 5.5 : CDCE62002 Generator – 1 Programming Register value

Register NO.	Programming Register value
Register 0	1030_0050(H)
Register 1	838F_00E1(H)
Register 2	2100_3DE2(H)

Table 5.6: CDCE62005 Generator – 2 Programming Register value

Register NO.	Programming Register value
Register 0	EB84_0320(H)
Register 1	EB80_0301(H)
Register 2	EB80_0302(H)
Register 3	EB40_0103(H)
Register 4	6884_0014(H)
Register 5	001C_03C5(H)
Register 6	840E_19A6(H)
Register 7	BD00_37F7(H)

Table 5.7: CDCE62005 Generator – 3 Programming Register value

Register NO.	Programming Register value
Register 0	EB86_0320(H)
Register 1	EB86_0301(H)
Register 2	EB0E_0302(H)
Register 3	EB86_0303(H)
Register 4	6884_0314(H)
Register 5	3810_0BE5(H)
Register 6	84be_09A6(H)
Register 7	FD00_37F7(H)

5.10 FPGA Configuration Registers

The TMS320TCI6614 SoC communicates with the FPGA configuration registers through the SPI interface. These registers are addressed by the memory mapped location and defined by the SoC SPI chip enable setting. The following tables list the FPGA configuration registers and the respective descriptions.

5.10.1 FPGA Configuration Registers Summary

Table 5.8: FPGA Configuration Registers Summary

Address Offset	Definition	Attribute (R/W) (RO : Read-Only)	Default Value
00h	FPGA Device ID (Low Byte)	RO	05h
01h	FPGA Device ID (High Byte)	RO	80h
02h	FPGA Revision ID (Low Byte)	RO	**
03h	FPGA Revision ID (High Byte)	RO	00h*
04h	BM GPI Status (Low Byte)	RO	----
05h	BM GPI Status (High Byte)	RO	----
06h	SoC GPI Status (Low Byte)	RO	----
07h	SoC GPI status (High Byte)	RO	----
08h	Debug LED and GPI 16 status	R/W, RO	-0h
09h	MMC Control	RO	----
0Ah	PHY Control	R/W	03h
0Bh	Reset Buttons Status	RO	00h
0Ch	Miscellaneous - 1	R/W	1Ch
0Dh	Miscellaneous - 2	RO	--
0Eh	FPGA FW Update SPI Interface Control Register	R/W	00h
0Fh	Scratch Register	R/W	00h
10h	CLK-GEN 2 Control Register	R/W	00h
11h	CLK-GEN 2 Interface Clock Setting	R/W	03h
13h~12h	Reserved		0s
14h	CLK-GEN 2 Command Byte 0	R/W	00h
15h	CLK-GEN 2 Command Byte 1	R/W	00h
16h	CLK-GEN 2 Command Byte 2	R/W	00h
17h	CLK-GEN 2 Command Byte 3	R/W	00h
18h	CLK-GEN 2 Read Data Byte 0	RO	00h
19h	CLK-GEN 2 Read Data Byte 1	RO	00h
1Ah	CLK-GEN 2 Read Data Byte 2	RO	00h
1Bh	CLK-GEN 2 Read Data Byte 3	RO	00h
1Fh~1Ch	Reserved		0s
20h	CLK-GEN 3 Control Register	R/W	00h
21h	CLK-GEN 3 Interface Clock Setting	R/W	03h
23h~22h	Reserved		0s
24h	CLK-GEN 3 Command Byte 0	R/W	00h
25h	CLK-GEN 3 Command Byte 1	R/W	00h

Address Offset	Definition	Attribute (R/W) (RO : Read-Only)	Default Value
26h	CLK-GEN 3 Command Byte 2	R/W	00h
27h	CLK-GEN 3 Command Byte 3	R/W	00h
28h	CLK-GEN 3 Read Data Byte 0	RO	00h
29h	CLK-GEN 3 Read Data Byte 1	RO	00h
2Ah	CLK-GEN 3 Read Data Byte 2	RO	00h
2Bh	CLK-GEN 3 Read Data Byte 3	RO	00h
3Fh~2Ch	Reserved		0s
40h	CLK-GEN 1 Control Register	R/W	00h
41h	CLK-GEN 1 Interface Clock Setting	R/W	03h
43h~42h	Reserved		0s
44h	CLK-GEN 1 Command Byte 0	R/W	00h
45h	CLK-GEN 1 Command Byte 1	R/W	00h
46h	CLK-GEN 1 Command Byte 2	R/W	00h
47h	CLK-GEN 1 Command Byte 3	R/W	00h
48h	CLK-GEN 1 Read Data Byte 0	RO	00h
49h	CLK-GEN 1 Read Data Byte 1	RO	00h
4Ah	CLK-GEN 1 Read Data Byte 2	RO	00h
4Bh	CLK-GEN 1 Read Data Byte 3	RO	00h
4Fh~4Ch	Reserved		0s
50h	ICS 557 Clock Select Control Register	R/W	0-h
51h	DAC7611 Control Register	R/W	03h
5Fh~52h	Reserved		0s
60h	32-Bit Counter Captured Value Byte0	RO	----
61h	32-Bit Counter Captured Value Byte1	RO	----
62h	32-Bit Counter Captured Value Byte2	RO	----
63h	32-Bit Counter Captured Value Byte3	RO	----
64h	32-Bit Counter Compared Value Byte0	R/W	00h
65h	32-Bit Counter Compared Value Byte1	R/W	00h
66h	32-Bit Counter Compared Value Byte2	R/W	00h
67h	32-Bit Counter Compared Value Byte3	R/W	00h
6Fh~68h	Reserved		0s
Note : “*” means the value may be changed in the future FPGA FW update release.			

5.10.2 FPGA Configuration Registers Descriptions

Register Address : **SPI Base + 00h**
Register Name : **FPGA Device ID (Low Byte) Register**
Default Value: 0Ch
Attribute : Read Only

Bit	Description	Read/Write
7-0	FPGA Device ID (Low Byte) This offset 01h field combined with this field identifies the particular device. This identifier is allocated by the FPGA design team.	RO

Register Address : **SPI Base + 01h**
Register Name : **FPGA Device ID (High Byte) Register**
Default Value: 80h
Attribute : Read Only

Bit	Description	Read/Write
7-0	FPGA Device ID (High Byte) This field combined with the offset 00h field identifies the particular device. This identifier is allocated by the FPGA design team.	RO

Register Address : **SPI Base + 02h**
Register Name : **FPGA Revision ID (Low Byte) Register**
Default Value: **
Attribute : Read Only

Bit	Description	Read/Write
7-0	FPGA Revision ID (Low Byte) This offset 03h register combined with this register specifies the FPGA device specific revision identifier. The value may be changed in the future FPGA FW update release.	RO

Register Address : **SPI Base + 03h**
Register Name : **FPGA Revision ID (High Byte) Register**
Default Value: 00h*
Attribute : Read Only

Bit	Description	Read/Write
7-0	FPGA Revision ID (High Byte) This register combined with the offset 02h register specifies the FPGA device specific revision identifier. The value may be changed in the future FPGA FW update release.	RO

Register Address : **SPI Base + 04h**
Register Name : **BM GPI Status (07-00 Low Byte) Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	BM GPIO 00 : This bit reflects the state of the BM general purpose input signal GPIO 00 and writes will have no effect.	RO

	0 : BM GPIO 00 state is low 1 : BM GPIO 00 state is high	
1	BM GPIO 01 : This bit reflects the state of the BM general purpose input signal GPIO 01 and writes will have no effect. 0 : BM GPIO 01 state is low 1 : BM GPIO 01 state is high	RO
2	BM GPIO 02 : This bit reflects the state of the BM general purpose input signal GPIO 02 and writes will have no effect. 0 : BM GPIO 02 state is low 1 : BM GPIO 02 state is high	RO
3	BM GPIO 03 : This bit reflects the state of the BM general purpose input signal GPIO 03 and writes will have no effect. 0 : BM GPIO 03 state is low 1 : BM GPIO 03 state is high	RO
4	BM GPIO 04 : This bit reflects the state of the BM general purpose input signal GPIO 04 and writes will have no effect. 0 : BM GPIO 04 state is low 1 : BM GPIO 04 state is high	RO
5	BM GPIO 05 : This bit reflects the state of the BM general purpose input signal GPIO 05 and writes will have no effect. 0 : BM GPIO 05 state is low 1 : BM GPIO 05 state is high	RO
6	BM GPIO 06 : This bit reflects the state of the BM general purpose input signal GPIO 06 and writes will have no effect. 0 : BM GPIO 06 state is low 1 : BM GPIO 06 state is high	RO
7	BM GPIO 07 : This bit reflects the state of the BM general purpose input signal GPIO 07 and writes will have no effect. 0 : BM GPIO 07 state is low 1 : BM GPIO 07 state is high	RO

Register Address : **SPI Base + 05h**
Register Name : **BM GPI (15-08 High Byte) Status Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	BM GPIO 08 : This bit reflects the state of the BM general purpose input signal GPIO 08 and writes will have no effect. 0 : BM GPIO 08 state is low 1 : BM GPIO 08 state is high	RO
1	BM GPIO 09 : This bit reflects the state of the BM general purpose input signal GPIO 09 and writes will have no effect. 0 : BM GPIO 09 state is low 1 : BM GPIO 09 state is high	RO
2	BM GPIO 10 : This bit reflects the state of the BM general purpose input signal GPIO 10 and writes will have no effect. 0 : BM GPIO 10 state is low	RO

	1 : BM GPIO 10 state is high	
3	BM GPIO 11 : This bit reflects the state of the BM general purpose input signal GPIO 11 and writes will have no effect. 0 : BM GPIO 11 state is low 1 : BM GPIO 11 state is high	RO
4	BM GPIO 12 : This bit reflects the state of the BM general purpose input signal GPIO 12 and writes will have no effect. 0 : BM GPIO 12 state is low 1 : BM GPIO 12 state is high	RO
5	BM GPIO 13 : This bit reflects the state of the BM general purpose input signal GPIO 13 and writes will have no effect. 0 : BM GPIO 13 state is low 1 : BM GPIO 13 state is high	RO
6	BM GPIO 14 : This bit reflects the state of the BM general purpose input signal GPIO 14 and writes will have no effect. 0 : BM GPIO 14 state is low 1 : BM GPIO 14 state is high	RO
7	BM GPIO 15 : This bit reflects the state of the BM general purpose input signal GPIO 15 and writes will have no effect. 0 : BM GPIO 15 state is low 1 : BM GPIO 15 state is high	RO

Register Address : **SPI Base + 06h**
Register Name : **SoC GPI (07-00 Low Byte) Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	SoC GPIO 00 : This bit reflects the state of the SoC general purpose input signal GPIO 00 and writes will have no effect. 0 : SoC GPIO 00 state is low 1 : SoC GPIO 00 state is high	RO
1	SoC GPIO 01 : This bit reflects the state of the SoC general purpose input signal GPIO 01 and writes will have no effect. 0 : SoC GPIO 01 state is low 1 : SoC GPIO 01 state is high	RO
2	SoC GPIO 02 : This bit reflects the state of the SoC general purpose input signal GPIO 02 and writes will have no effect. 0 : SoC GPIO 02 state is low 1 : SoC GPIO 02 state is high	RO
3	SoC GPIO 03 : This bit reflects the state of the SoC general purpose input signal GPIO 03 and writes will have no effect. 0 : SoC GPIO 03 state is low 1 : SoC GPIO 03 state is high	RO
4	SoC GPIO 04 : This bit reflects the state of the SoC general purpose input signal GPIO 04 and writes will have no effect. 0 : SoC GPIO 04 state is low 1 : SoC GPIO 04 state is high	RO

5	SoC GPIO 05 : This bit reflects the state of the SoC general purpose input signal GPIO 05 and writes will have no effect. 0 : SoC GPIO 05 state is low 1 : SoC GPIO 05 state is high	RO
6	SoC GPIO 06 : This bit reflects the state of the SoC general purpose input signal GPIO 06 and writes will have no effect. 0 : SoC GPIO 06 state is low 1 : SoC GPIO 06 state is high	RO
7	SoC GPIO 07 : This bit reflects the state of the SoC general purpose input signal GPIO 07 and writes will have no effect. 0 : SoC GPIO 07 state is low 1 : SoC GPIO 07 state is high	RO

Register Address : **SPI Base + 07h**
Register Name : **SoC GPI (15-08 High Byte) Status Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
0	SoC GPIO 08 : This bit reflects the state of the SoC general purpose input signal GPIO 08 and writes will have no effect. 0 : SoC GPIO 08 state is low 1 : SoC GPIO 08 state is high	RO
1	SoC GPIO 09 : This bit reflects the state of the SoC general purpose input signal GPIO 09 and writes will have no effect. 0 : SoC GPIO 09 state is low 1 : SoC GPIO 09 state is high	RO
2	SoC GPIO 10 : This bit reflects the state of the SoC general purpose input signal GPIO 10 and writes will have no effect. 0 : SoC GPIO 10 state is low 1 : SoC GPIO 10 state is high	RO
3	SoC GPIO 11 : This bit reflects the state of the SoC general purpose input signal GPIO 11 and writes will have no effect. 0 : SoC GPIO 11 state is low 1 : SoC GPIO 11 state is high	RO
4	SoC GPIO 12 : This bit reflects the state of the SoC general purpose input signal GPIO 12 and writes will have no effect. 0 : SoC GPIO 12 state is low 1 : SoC GPIO 12 state is high	RO
5	SoC GPIO 13 : This bit reflects the state of the SoC general purpose input signal GPIO 13 and writes will have no effect. 0 : SoC GPIO 13 state is low 1 : SoC GPIO 13 state is high	RO
6	SoC GPIO 14 : This bit reflects the state of the SoC general purpose input signal GPIO 14 and writes will have no effect. 0 : SoC GPIO 14 state is low 1 : SoC GPIO 14 state is high	RO
7	SoC GPIO 15 : This bit reflects the state of the SoC general	RO

	purpose input signal GPIO 15 and writes will have no effect. 0 : SoC GPIO 15 state is low 1 : SoC GPIO 15 state is high	

Register Address : **SPI Base + 08h**
Register Name : **Debug LED and GPI16 Status Register**
Default Value: -0h
Attribute : Read/Write

Bit	Description	Read/Write
0	DEBUG_LED 0 : This bit can be updated by the SoC software to drive a high or low value on the debug LED 0 pin. 0 : DEBUG_LED 0 drives low 1 : DEBUG_LED 0 drives high	R/W
1	DEBUG_LED 1 : This bit can be updated by the SoC software to drive a high or low value on the debug LED 1 pin. 0 : DEBUG_LED 1 drives low 1 : DEBUG_LED 1 drives high	R/W
2	DEBUG_LED 3 : This bit can be updated by the SoC software to drive a high or low value on the debug LED 2 pin 0 : DEBUG_LED 3 drives low 1 : DEBUG_LED 3 drives high	R/W
3	DEBUG_LED 3 : This bit can be updated by the SoC software to drive a high or low value on the debug LED 3 pin 0 : DEBUG_LED 3 drives low 1 : DEBUG_LED 3 drives high	R/W
5-4	Reserved	RO
6	BM GPIO 16 : This bit reflects the state of the BM general purpose input signal GPIO 16 and writes will have no effect. 0 : BM GPIO 16 state is low 1 : BM GPIO 16 state is high	RO
7	SoC GPIO 16 : This bit reflects the state of the SoC general purpose input signal GPIO 16 and writes will have no effect. 0 : SoC GPIO 16 state is low 1 : SoC GPIO 16 state is high	RO

Register Address : **SPI Base + 09h**
Register Name : **MMC Control Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	MMC_DETECT# : This bit reflects the MMC_DETECT# state and it is used by the MMC to indicate the AMC chassis insertion status. 0 : MMC_DETECT# state is low to indicate that the EVM is inserted into the AMC chassis. 1 : MMC_DETECT# state is high to indicate that the EVM is not inserted into the AMC chassis.	RO
1	MMC_RESETSTAT# : This bit reflects the SoC RESETSTAT# state	RO

	and the FPGA will drive the same logic value on the MMC_RESETSTAT# pin (to MMC). 0 : SoC RESETSTAT# state is low and the FPGA drives MMC_RESETSTAT# low to MMC 1 : SoC RESETSTAT# state is high and the FPGA drives MMC_RESETSTAT# high to MMC	
2	MMC_POR_IN_AMC# : This bit reflects the MMC_POR_IN_AMC# state and it is used by the MMC to trigger a power on sequence & reset event. 0 : MMC_POR_IN_AMC# state is low to trigger a power on sequence & reset event. 1 : MMC_POR_IN_AMC# state is high and the FPGA stays in current state.	RO
3	MMC_WR_AMC# : This bit reflects the MMC_WR_AMC# state and it is used by the MMC to trigger a warm reset event. 0 : MMC_WR_AMC# state is low to trigger a warm reset event. 1 : MMC_WR_AMC# state is high and the FPGA stays in current state	RO
4	MMC_BOOTCOMPLETE: This bit reflects the SoC_BOOTCOMPLETE state and the FPGA will drive the same logic value on the MMC_ BOOTCOMPLETE pin (to MMC). 0 : SoC_BOOTCOMPLETE state is low and the FPGA drives MMC_ BOOTCOMPLETE low to MMC 1 : SoC_BOOTCOMPLETE state is high and the FPGA drives MMC_ BOOTCOMPLETE high to MMC	RO
7-5	Reserved	RO

Register Address : **SPI Base + 0Ah**
Register Name : **PHY Control Register**
Default Value: 03h
Attribute : Read/Write

Bit	Description	Read/Write
0	PHY_INT# : This bit reflects the PHY_INT# state. 0 : PHY_INT# state is low. 1 : PHY_INT# state is high.	RO
1	PHY_RST# : This bit can be updated by the SoC software to drive a high or low value on the PHY_RST# pin 0 : PHY_RST# drives low 1 : PHY_RST# drives high	R/W
7-3	Reserved	RO

Register Address : **SPI Base + 0Bh**
Register Name : **Reset Button Status Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	FULL_RESET button status : This bit reflects the FULL_RESET	RO

	button state. This button is used to request a power full reset sequence to SoC. A logic Low to High transition on this button signal will complete the FPGA FULL_RESET sequence with a specified delay time. 0 : FULL_RESET button state is low 1 : FULL_RESET button state is high	
1	WARM_RESET button status : This bit reflects the WARM _RESET button state. This button is used to request a warm reset sequence to SoC. A logic Low to High transition on this button signal will complete the FPGA WARM_RESET sequence with a specified delay time. 0 : WARM_RESET button state is low 1 : WARM_RESET button state is high	RO
3-2	Reserved	RO
4	SoC_RESETSTAT# : This bit reflects the SoC_RESETSTAT# state. 0 : SoC_RESETSTAT# state is low 1 : SoC_RESETSTAT# state is high	RO
5	TRGRSTZ : This bit reflects the TRGRSTZ state. 0 : TRGRSTZ state is low 1 : TRGRSTZ state is high	RO
6	PCIESSEN : This bit reflects the PCIESSEN switch state. 0 : PCIESSEN state is low 1 : PCIESSEN state is high	RO
7	User_Define Switch : This bit reflects the User_Define Switch state. 0 : User_Define Switch state is low 1 : User_Define Switch state is high	RO

Register Address : **SPI Base + 0Ch**
Register Name : **Miscellaneous - 1 Register**
Default Value: 1Ch
Attribute : Read/Write

Bit	Description	Read/Write
1-0	Reserved	R/W
2	NAND_WP# : This bit can be updated by the SoC software to drive a high or low value on the NAND_WP# pin 0 : NAND_WP# drives low 1 : NAND_WP# drives high	R/W
3	XDS560_IL control 0 : Disable XDS560 mezzanine card 1 : Enable XDS560 mezzanine card (Default)	R/W
4	NOR_WP# : This bit can be updated by the SoC software to drive a high or low value on the NOR_WP# pin 0 : NOR_WP# drives low 1 : NOR_WP# drives high	R/W
5	EEPROM_WP : This bit can be updated by the SoC software to drive a high or low value on the EEPROM_WP pin	R/W

	0 : EEPROM_WP drives low 1 : EEPROM_WP drives high	
6	PCA9306_EN : This bit can be updated by the SoC software to drive a high or low value on the PCA9306_EN pin (RFU) 0 : PCA9306_EN drives low (Default) 1 : PCA9306_EN drives high	R/W
7	Reserved	RO

Register Address : **SPI Base + 0Dh**
Register Name : Miscellaneous - 2 Register
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
0	FPGA FW Update SPI Interface Enable Status : This bit reflects the FPGA FW Update SPI Interface Enable status. The FPGA FW Update SPI interface could be enabled/disabled through the offset 0Eh register. 0 : FPGA FW update SPI interface is disabled. 1 : FPGA FW update SPI interface is enabled. The SoC_GPIO[12] is mapped to FPGA_FW_SPI_CLK. The SoC_GPIO[13] is mapped to FPGA_FW_SPI_CS#. The SoC_GPIO[14] is mapped to FPGA_FW_SPI_MOSI. The SoC_GPIO[15] is mapped to FPGA_FW_SPI_MISO.	RO
1	SoC_HOUT status : This bit reflects the SoC_HOUT signal state. 0 : SoC_HOUT state is low 1 : SoC_HOUT state is high	RO
2	SoC_SYSCLKOUT status : This bit reflects the SoC_SYSCLKOUT signal state. 0 : SoC_SYSCLKOUT state is low 1 : SoC_SYSCLKOUT state is high	RO
7-3	Reserved	RO

Register Address : **SPI Base + 0Eh**
Register Name : **FPGA FW Update SPI Interface Control Register**
Default Value: Default Value: ----
Attribute : Read/Write

Bit	Description	Read/Write
7-0	FPGA FW Update SPI Interface Enable Control : These bits are used to enable/disable the FPGA FW Update SPI Interface. If the value of this register be set to 68h, the FPGA FW Update SPI interface would be enabled. All the other values set to this register would disable the FPGA FW Update SPI interface. 68h : FPGA FW update SPI interface is enabled. Others : FPGA FW update SPI interface is disabled. The SoC_GPIO[12] is mapped to FPGA_FW_SPI_CLK. The SoC_GPIO[13] is mapped to FPGA_FW_SPI_CS#. The SoC_GPIO[14] is mapped to FPGA_FW_SPI_MOSI.	R/W

	The SoC_GPIO[15] is mapped to FPGA_FW_SPI_MISO.	

Register Address : **SPI Base + 0Fh**
Register Name : **Scratch Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	Scratch Data	R/W

Register Address : **SPI Base + 10h**
Register Name : **CLK-GEN 2 Control Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
0	Initiate the data transfer sequence via the SPI bus to update the SPI command to CDCE62005 Clock Generator 2 The CDCE62005 will be reprogrammed by data transfer sequence. 0 : Idle state 1 : Write 1 to perform the SPI command update process.	R/W
1	The BUSY status indication for the CDCE62005 Clock Generator 2 SPI bus 0 : The SPI bus for the CDCE62005 Clock Generator 2 is idle. 1 : The SPI bus for the CDCE62005 Clock Generator 2 is busy and a SPI command is processing..	RO
2	SoC_PORZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
3	SoC_RESETFULLZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
4	SoC_RESETZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
7-5	Reserved	RO

Register Address : **SPI Base + 11h**
Register Name : **CLK-GEN 2 Interface Clock Setting Register**
Default Value: 03h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register is a clock divider setting to adjust the interface clock for the CDCE62005 Clock Generator 2 SPI bus. 00 : CDCE62005 2 SPI Clock = 12MHz (= 48 / 4)	R/W

	01 : CDCE62005 2 SPI Clock = 12MHz (= 48 / 4) 02 : CDCE62005 2 SPI Clock = 8 MHz (= 48 / 6) 03 : CDCE62005 2 SPI Clock = 6 MHz (= 48 / 8) 04 : CDCE62005 2 SPI Clock = 4.8 MHz (= 48 /10) 05 : CDCE62005 2 SPI Clock = 4 MHz (= 48 /12) 06 : CDCE62005 2 SPI Clock = 3.42 MHz (= 48 / 14) …… X : CDCE62005 2 SPI Clock = 48 MHz /((X+1)*2) if X != 0	

Register Address : **SPI Base + 12h ~ 13h**
Register Name : **Reserved**

Register Address : **SPI Base + 14h**
Register Name : **CLK-GEN 2 Command Byte 0 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 0 to the CDCE62005 Clock Generator 2 3-0 : SPI command address field bit 3 to bit 0 7-4 : SPI command data field bit 3 to bit 0	R/W

Register Address : **SPI Base + 15h**
Register Name : **CLK-GEN 2 Command Byte 1 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 1 to the CDCE62005 Clock Generator 2 7-0 : SPI command data field bit 11 to bit 4	R/W

Register Address : **SPI Base + 16h**
Register Name : **CLK-GEN 2 Command Byte 2 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 2 to the CDCE62005 Clock Generator 2 7-0 : SPI command data field bit 19 to bit12	R/W

Register Address : **SPI Base + 17h**
Register Name : **CLK-GEN 2 Command Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 3 to the CDCE62005 Clock Generator 2	R/W

	7-0 : SPI command data field bit 27 to bit 20	

Register Address : **SPI Base + 18h**
Register Name : **CLK-GEN 2 Read Data Byte 0 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62005 Clock Generator 2 for responding a host SPI Read Command. 3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4 : The SPI read back data bit 3 to bit 0 for a SPI Read Command.	RO

Register Address : **SPI Base + 19h**
Register Name : **CLK-GEN 2 Read Data Byte 1 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 2 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 11 to bit 4 for a SPI Read Command.	RO

Register Address : **SPI Base + 1Ah**
Register Name : **CLK-GEN 2 Read Data Byte 2 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 2 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 19 to bit 12 for a SPI Read Command.	RO

Register Address : **SPI Base + 1Bh**
Register Name : **CLK-GEN 2 Read Data Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 2 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 27 to bit 20 for a SPI Read Command.	RO

Register Address : **SPI Base + 1Ch ~ 1Fh**
Register Name : **Reserved**

Register Address : **SPI Base + 20h**
Register Name : **CLK-GEN 3 Control Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
0	Initiate the data transfer sequence via the SPI bus to update the SPI command to CDCE62005 Clock Generator 3 The CDCE62005 will be reprogrammed by data transfer sequence. 0 : Idle state 1 : Write 1 to perform the SPI command update process.	R/W
1	The BUSY status indication for the CDCE62005 Clock Generator 2 SPI bus 0 : The SPI bus for the CDCE62005 Clock Generator 2 is idle. 1 : The SPI bus for the CDCE62005 Clock Generator 2 is busy and a SPI command is processing..	RO
2	SoC_PORZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
3	SoC_RESETFULLZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
4	SoC_RESETZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
7-5	Reserved	RO

Register Address : **SPI Base + 21h**
Register Name : **CLK-GEN 3 Interface Clock Setting Register**
Default Value: 03h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register is a clock divider setting to adjust the interface clock for the CDCE62005 Clock Generator 3 SPI bus. 00 : CDCE62005 3 SPI Clock = 12MHz (= 48 / 4) 01 : CDCE62005 3 SPI Clock = 12MHz (= 48 / 4) 02 : CDCE62005 3 SPI Clock = 8 MHz (= 48 / 6) 03 : CDCE62005 3 SPI Clock = 6 MHz (= 48 / 8) 04 : CDCE62005 3 SPI Clock = 4.8 MHz (= 48 /10) 05 : CDCE62005 3 SPI Clock = 4 MHz (= 48 /12)	R/W

	06 : CDCE62005 3 SPI Clock = 3.42 MHz (= 48 / 14) …… X : CDCE62005 3 SPI Clock = 48 MHz /((X+1)*2) if X != 0	

Register Address : **SPI Base + 22h ~ 23h**
Register Name : **Reserved**

Register Address : **SPI Base + 24h**
Register Name : **CLK-GEN 3 Command Byte 0 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 0 to the CDCE62005 Clock Generator 3 3-0 : SPI command address field bit 3 to bit 0 7-4 : SPI command data field bit 3 to bit 0	R/W

Register Address : **SPI Base + 25h**
Register Name : **CLK-GEN 3 Command Byte 1 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 1 to the CDCE62005 Clock Generator 3 7-0 : SPI command data field bit 11 to bit 4	R/W

Register Address : **SPI Base + 26h**
Register Name : **CLK-GEN 3 Command Byte 2 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 2 to the CDCE62005 Clock Generator 3 7-0 : SPI command data field bit 19 to bit 12	R/W

Register Address : **SPI Base + 27h**
Register Name : **CLK-GEN 3 Command Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 3 to the CDCE62005 Clock Generator 3 7-0 : SPI command data field bit 27 to bit 20	R/W

Register Address : **SPI Base + 28h**
Register Name : **CLK-GEN 3 Read Data Byte 0 Register**
Default Value: 00h

Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62005 Clock Generator 3 for responding to a host SPI Read Command. 3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4 : The SPI read back data bit 3 to bit 0 for a SPI Read Command.	RO

Register Address : **SPI Base + 29h**
Register Name : **CLK-GEN 3 Read Data Byte 1 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 3 for responding to a host SPI Read Command. 7-0 : The SPI read back data bit 11 to bit 4 for a SPI Read Command.	RO

Register Address : **SPI Base + 2Ah**
Register Name : **CLK-GEN 3 Read Data Byte 2 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 3 for responding to a host SPI Read Command. 7-0 : The SPI read back data bit 19 to bit 12 for a SPI Read Command.	RO

Register Address : **SPI Base + 2Bh**
Register Name : **CLK-GEN 3 Read Data Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator 3 for responding to a host SPI Read Command. 7-0 : The SPI read back data bit 27 to bit 20 for a SPI Read Command.	RO

Register Address : **SPI Base + 2Ch ~ 3Fh**
Register Name : **Reserved**

Register Address : **SPI Base + 40h**

Register Name : **CLK-GEN 1 Control Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
0	Initiate the data transfer sequence via the SPI bus to update the SPI command to CDCE62002 Clock Generator 1 The CDCE62002 will be reprogrammed by data transfer sequence. 0 : Idle state 1 : Write 1 to perform the SPI command update process.	R/W
1	The BUSY status indication for the CDCE62005 Clock Generator 2 SPI bus 0 : The SPI bus for the CDCE62002 Clock Generator 1 is idle. 1 : The SPI bus for the CDCE62002 Clock Generator 1 is busy and a SPI command is processing..	RO
2	SoC_PORZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
3	SoC_RESETFULLZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
4	SoC_RESETZ signal will generate one active pulse after data transfer sequence is finished 1: Enable 0: Disable	R/W
7-5	Reserved	RO

Register Address : **SPI Base + 41h**
Register Name : **CLK-GEN 1 Interface Clock Setting Register**
Default Value: 03h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register is a clock divider setting to adjust the interface clock for the CDCE62002 Clock Generator 1 SPI bus. 00 : CDCE62002 SPI Clock = 12MHz (= 48 / 4) 01 : CDCE62002 SPI Clock = 12MHz (= 48 / 4) 02 : CDCE62002 SPI Clock = 8 MHz (= 48 / 6) 03 : CDCE62002 SPI Clock = 6 MHz (= 48 / 8) 04 : CDCE62002 SPI Clock = 4.8 MHz (= 48 /10) 05 : CDCE62002 SPI Clock = 4 MHz (= 48 /12) 06 : CDCE62002 SPI Clock = 3.42 MHz (= 48 / 14) …… X : CDCE62002 SPI Clock = 48 MHz /((X+1)*2) if X != 0	R/W

Register Address : **SPI Base + 42h ~ 43h**

Register Name : **Reserved**

Register Address : **SPI Base + 44h**
Register Name : **CLK-GEN 1 Command Byte 0 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 0 to the CDCE62002 Clock Generator 1 3-0 : SPI command address field bit 3 to bit 0 7-4 : SPI command data field bit 3 to bit 0	R/W

Register Address : **SPI Base + 45h**
Register Name : **CLK-GEN 1 Command Byte 1 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 1 to the CDCE62002 Clock Generator 1 7-0 : SPI command data field bit 11 to bit 4	R/W

Register Address : **SPI Base + 46h**
Register Name : **CLK-GEN 1 Command Byte 2 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 2 to the CDCE62002 Clock Generator 1 7-0 : SPI command data field bit 19 to bit12	R/W

Register Address : **SPI Base + 47h**
Register Name : **CLK-GEN 1 Command Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 3 to the CDCE62002 Clock Generator 1 7-0 : SPI command data field bit 27 to bit 20	R/W

Register Address : **SPI Base + 48h**
Register Name : **CLK-GEN 1 Read Data Byte 0 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62002 Clock Generator 1 for responding a host SPI Read Command.	RO

	3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4 : The SPI read back data bit 3 to bit 0 for a SPI Read Command.	

Register Address : **SPI Base + 49h**
Register Name : **CLK-GEN 1 Read Data Byte 1 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62002 Clock Generator 1 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 11 to bit 4 for a SPI Read Command.	RO

Register Address : **SPI Base + 4Ah**
Register Name : **CLK-GEN 1 Read Data Byte 2 Register**
Default Value: 00h
Attribute : Read Only

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62002 Clock Generator 1 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 19 to bit 12 for a SPI Read Command.	RO

Register Address : **SPI Base + 4Bh**
Register Name : **CLK-GEN 1 Read Data Byte 3 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62002 Clock Generator 1 for responding a host SPI Read Command. 7-0 : The SPI read back data bit 27 to bit 20 for a SPI Read Command.	RO

Register Address : **SPI Base + 4Ch ~ 4Fh**
Register Name : **Reserved**

Register Address : **SPI Base + 50h**
Register Name : **ICS 557 Clock Selection Control Register**
Default Value: 0-h
Attribute : Read/Write

Bit	Description	Read/Write
0	FPGA_ICS557_SEL : This bit can be updated by the SoC software	R/W

	to drive a high or low value on the FPGA_ICS557_SEL pin. FPGA will latch the BM_GPIO7 as the default value when power-sequence is finished. 0 : FPGA_ICS557_SEL drives low 1 : FPGA_ICS557_SEL drives high	
7-1	Reserved	RO

Register Address : **SPI Base + 51h**
Register Name : **DAC7611 Control Register**
Default Value: 03h
Attribute : Read/Write

Bit	Description	Read/Write
0	DAC_CLR# : This bit can be updated by the SoC software to drive a high or low value on the DAC_CLR# pin. 0 : DAC_CLR# drives low 1 : DAC_CLR# drives high	R/W
1	DAC_LD# : This bit can be updated by the SoC software to drive a high or low value on the DAC_LD# pin. 0 : DAC_LD# drives low 1 : DAC_LD# drives high	R/W
7-2	Reserved	RO

Register Address : **SPI Base + 52h ~ 5Fh**
Register Name : **Reserved**

Register Address : **SPI Base +60h**
Register Name : **32-Bit Counter Captured Value Byte0 Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
7-0	The register reflect the 32-bit counter captured value byte0 data 7-0 : The SPI read back data bit 7 to bit 0 for the 32-bit counter captured value.	RO

Register Address : **SPI Base +61h**
Register Name : **32-Bit Counter Captured Value Byte1 Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
7-0	The register reflect the 32-bit counter captured value byte1 data 7-0 : The SPI read back data bit 15 to bit 8 for the 32-bit counter captured value.	RO

Register Address : **SPI Base +62h**
Register Name : **32-Bit Counter Captured Value Byte2 Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
7-0	The register reflect the 32-bit counter captured value byte2 data 7-0 : The SPI read back data bit 23 to bit 16 for the 32-bit counter captured value.	RO

Register Address : **SPI Base +63h**
Register Name : **32-Bit Counter Captured Value Byte3 Register**
Default Value: ----
Attribute : Read Only

Bit	Description	Read/Write
7-0	The register reflect the 32-bit counter captured value byte3 data 7-0 : The SPI read back data bit 31 to bit 24 for the 32-bit counter captured value.	RO

Register Address : **SPI Base +64h**
Register Name : **32-Bit Counter Compared Value Byte0 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the 32-bit counter compared value byte0 7-0 : 32-bit counter compared value bit 7 to bit 0	R/W

Register Address : **SPI Base +65h**
Register Name : **32-Bit Counter Compared Value Byte1 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the 32-bit counter compared value byte1 7-0 : 32-bit counter compared value bit 15 to bit 8	R/W

Register Address : **SPI Base +66h**
Register Name : **32-Bit Counter Compared Value Byte2 Register**
Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the 32-bit counter compared value byte2 7-0 : 32-bit counter compared value bit 23 to bit 16	R/W

Register Address : **SPI Base +67h**
Register Name : **32-Bit Counter Compared Value Byte3 Register**

Default Value: 00h
Attribute : Read/Write

Bit	Description	Read/Write
7-0	This register specifies the 32-bit counter compared value byte3 7-0 : 32-bit counter compared value bit 31 to bit 24	R/W

Register Address : **SPI Base + 68h ~ 6Fh**
Register Name : **Reserved**

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