Keystone 2 EVM Technical Reference Manual Version 1.0

Literature Number: SPRUHO2

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EVALUATION BOARD / KIT / MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all, or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

Your Obligations and Responsibilities

Please consult the EVM documentation, including but not limited to any user guides, setup guides or getting started guides, and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of, or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Warning

The EVM board may get very hot during use. Specifically, the DSP, its heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

Preface

About this Document

This document is a Technical Reference Manual for the Keystone 2 Evaluation Modules designed and developed by Advantech Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

Release	Chapter	Description of Change
1.00	All	The First Release for draft

Acronyms

Acronym	Description
AMC or *Advanced*MC	Advanced Mezzanine Card
AIF2	Second generation Antenna Interface
CCS	Code Composer Studio
DDR3	Double Data Rate 3 Interface
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MCH	MicroTCA Carrier Hub
MCU	Microcontroller Unit
MTCA or *Micro*TCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PICMG®	PCI Industrial Computer Manufacturers Group
PCIE	PCI express
RFU	Reserved for Future Use
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
TSIP	Telecom Serial Interface Port
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XGMII	10-Gbps media independent interface
XDS200	Texas Instruments' System Trace Emulator

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1. Overview

This chapter provides an overview of the EVM along with the key features and block diagram.

1.1 Key Features

The EVM is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Keystone 2 Texas Instruments' System-on-Chip (SoC).The EVM's form-factor is equivalent to a double-wide PICMG® MTCA.4 R1.0 *Advanced*MC module.

Schematics, code examples and application notes are available to ease the hardware development process and to reduce the time to market.

The key features of the EVM are:

- Texas Instruments' eight-core DSP+ four ARM core SoC
- 1024/2048 Mbytes of DDR3-1600 Memory on board
- 2048 Mbytes of DDR3-1333 ECC SO-DIMM
- 512 Mbytes of NAND Flash
- 16MB SPI NOR FLASH
- Four Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – two on AMC connector and two RJ-45 connector
- 170 pin B+ style AMC Interface containing SRIO, PCIe, Gigabit Ethernet, AIF2 and TDM
- TWO 160 pin ZD+ style uRTM Interface containing HyperLink, AIF2 ,XGMII (not supported all EVMs)
- 128K-byte I2C EEPROM for booting
- 4 User LEDs, 1 Banks of DIP Switches and 3 Software-controlled LEDs
- Two RS232 Serial interface on 4-Pin header or UART over mini-USB connector
- EMIF, Timer, I2C, SPI, UART on 120-pin expansion header
- One USB3.0 ports supporting 5 Gbps data-rate
- MIPI 60-Pin JTAG header to support all external emulator types
- LCD Display for Debugging state
- Micro Controller Unit (MCU) for Intelligent Platform Management Interface (IPMI)
- Optional XDS200 System Trace Emulation Mezzanine Card

- Powered by DC power-brick adaptor (12V/7.0A) or AMC Carrier backplane
- PICMG® AMC.0 R2.0 and uTCA.4 R1.0 Double width, full height *Advanced*MC module

1.2 Functional Overview

The SoC is a member of the C66x family based on TI's new KeyStone II Multicore SoC Architecture designed specifically for high performance applications.

The TMS320C66x™ DSPs are the highest-performance fixed / floating-point DSP generation in the TMS320C6000™ DSP platform. The SoC on this EVM is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), designed specifically for high density wireline / wireless media gateway infrastructure. It is an ideal solution for IP border gateways, video transcoding and translation, video-server and intelligent voice and video recognition applications. The C66x devices are backward code-compatible from previous devices that are part of the C6000™ DSP platform.

The functional block diagram and placement of EVM is shown in the figure below:

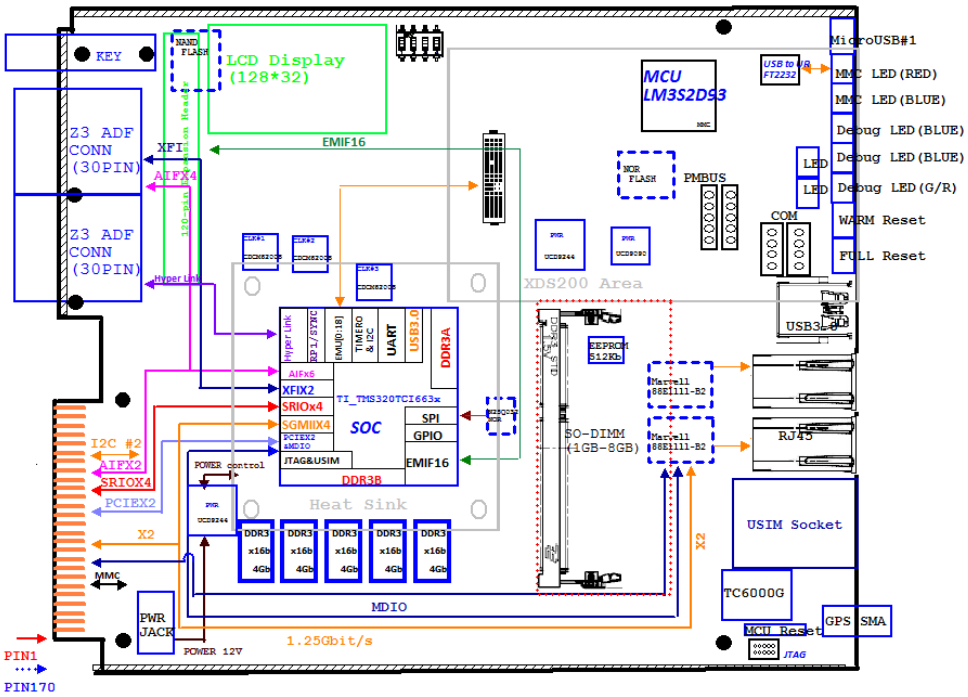


Figure 1.1: Placement of EVM

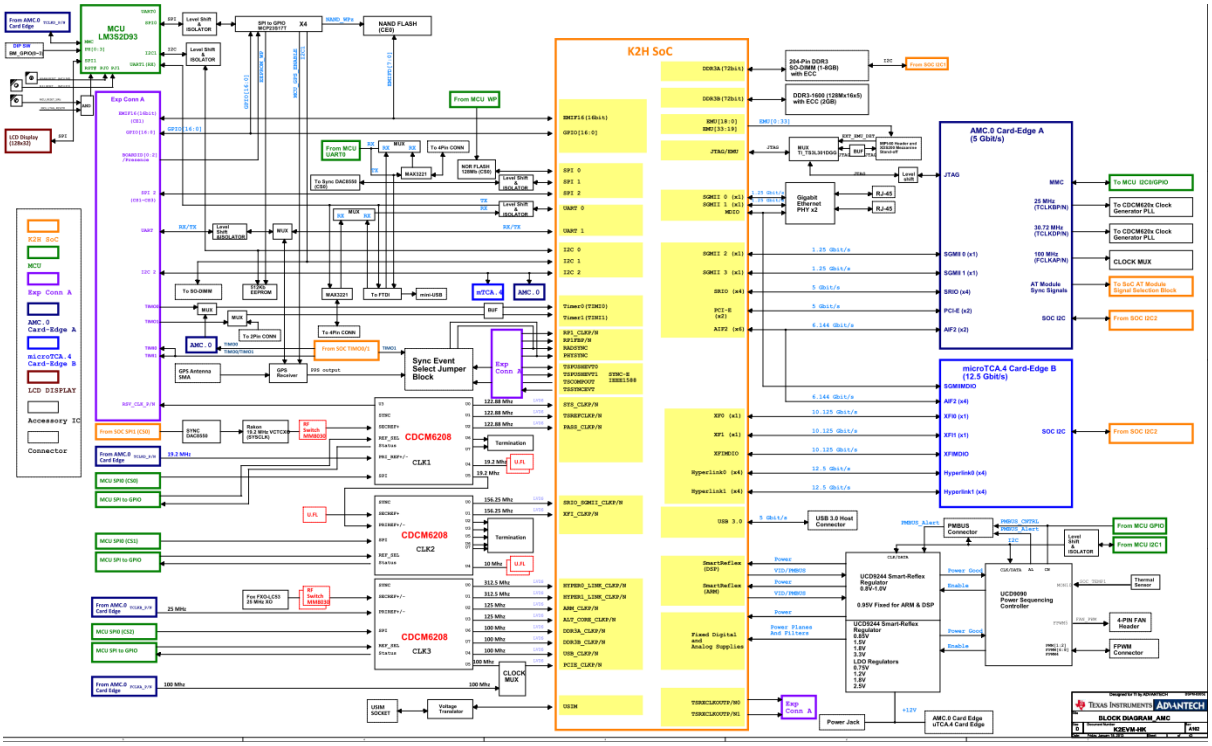


Figure 1.2: Block Diagram of EVM

1.3 Basic Operation

The EVM platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interface with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through an external emulator. We recommend using CCS rev 5.3 later versions.

The EVM comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. The MCSDK also includes an out-of-box demonstration; see the "MCSDK Getting Started Guide".

To start operating the board, follow instructions in the Quick Start Guide. This guide provides instruction for proper connections and configuration for running the POST and OOB Demos. After completing the POST and OOB Demos, proceed with installing CCS and the EVM support files by following the instructions on the DVD. This process will install all the necessary development tools, drivers and documentation.

After the installation has completed, follow the steps below to run Code Composer Studio.

1. Power-on the board using the power brick adaptor (12V/7.0A) supplied along with this EVM or inserting this EVM board into a MicroTCA chassis or AMC carrier backplane.

2. Connect the supplied USB cable from host PC to EVM board.

3. Launch Code Composer Studio from host PC by double clicking on its icon on the PC desktop.

Detailed information about the EVM including examples and reference materials are available in the DVD included with this EVM kit.

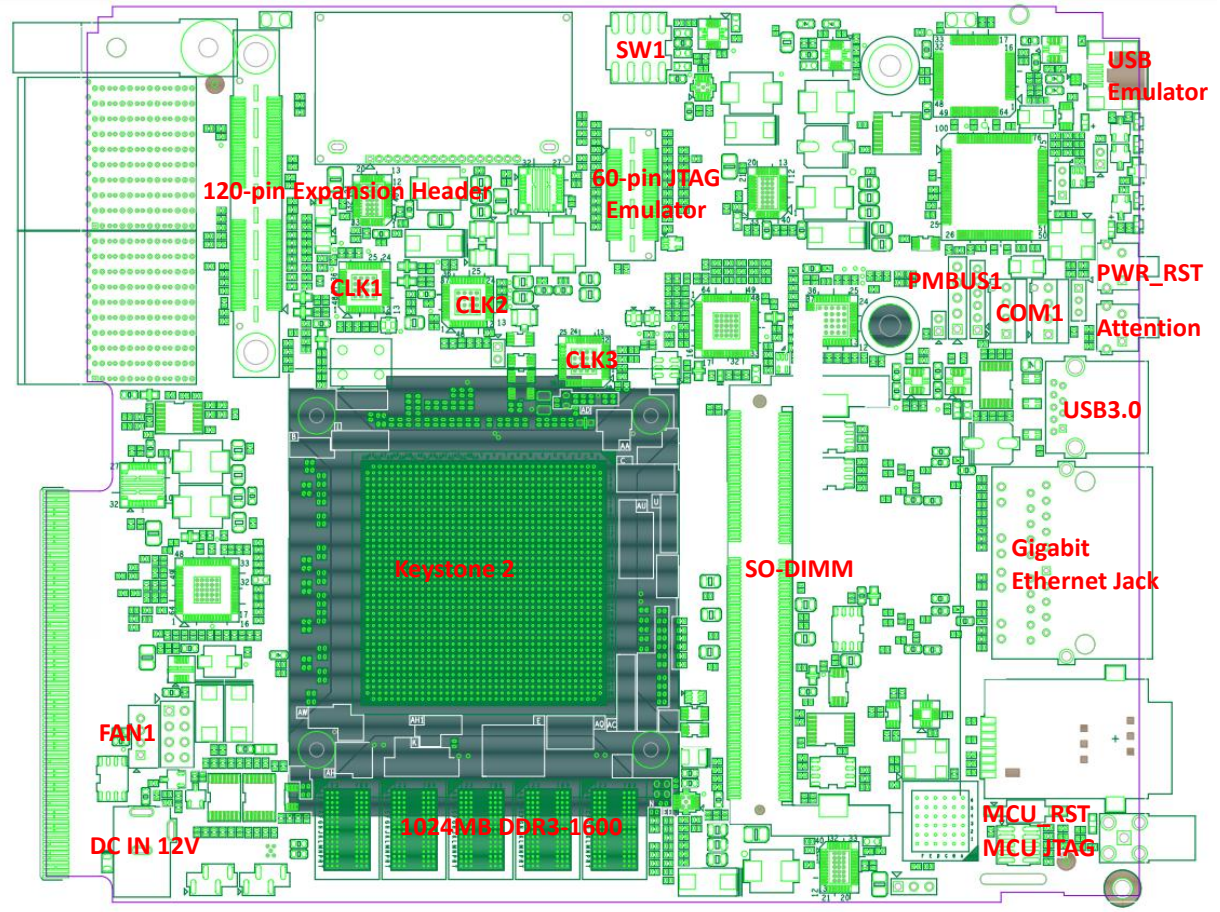


Figure 1.3: EVM Layout

1.4 Boot Mode and Boot Configuration Switch Setting

The EVM has 4 sliding DIP switches (Board Ref. SW1) to determine boot mode and boot configuration.

1.5 Power Supply

The EVM can be powered from a single +12V / 7.0A DC (84W) external power supply connected to the DC power jack (DC_IN1). Internally, +12V input is converted into required voltage levels using local DC-DC converters.

- CVDD (+0.75V~+1.00V) used for the Smart-Reflex enabled DSP and ARM Core logic
- CVDD1 (+0.95V) is used for DSP Array SRAM
- CVDD1 (+0.95V) is used for ARM Array SRAM
- +1.5V is used for DDR3 buffers of SoC, HyperLink/SRIO/SGMII/PCIe SERDES regulators in SoC and DDR3 DRAM chips
- +1.8V is used for DSP PLLs, ARM PLLs, DSP LVCMOS I/Os and MCU I/Os driving the DSP
- +2.5V is used for Gigabit Ethernet PHY core
- +1.2V is used for Gigabit Ethernet PHY core
- +3.3V is used for USB Digital and Analog of SoC
- +0.85V is used for SERDES Low Analog and USB Analog of SoC
- +5V is used for external USB3.0 port
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity

The EVM can also draw power from the AMC edge connector (AMC1). If the board is inserted into a PICMG® MicroTCA.0 R1.0 compliant system chassis or AMC Carrier backplane, an external +12V supply from DC jack (DC_IN1) is not required.

2. Introduction to the EVM board

This chapter provides an introduction and details of interfaces for the EVM board.It contains:

2.1 Memory Map

The memory map of the SoC device is as shown in Table 2.1. The external memory configuration register address ranges in the SoC device begin at the hex address location 0x3000 0000 for EMIFA , hex address location 0x6000 0000 - 0xFFFF FFFF for DDR3B

Memory Controller and hex address location 0x08 F000 0000 - 0x09 FFFF FFFF for DDR3A Memory Controller . For the details about the memory map, please refer to the TCI6638K2K Data Manual.

Table 2.1: SoC Memory Map

Address Range	Bytes	Memory Block Description
0x00000000 – 0x003FFFFF	**256K**	**ARM ROM**
0x00800000 – 0x008FFFFF	1M	Local L2 SRAM
0x00E00000 – 0x00E07FFF	32K	Local L1P SRAM
0x00F00000 – 0x00F07FFF	32K	L1D SRAM
0x01000000 – 0x0100FFFF	64K	C66x CorePac Registers
0x01010000 – 0x010FFFFF	1M-64K	C66x CorePac Registers
0x01000000 – 0x0100FFFF	64K	C66x CorePac Registers
0x01010000 – 0x01BFFFFF	11M-64K	C66x CorePac Registers
0x01E80000 – 0x01E83FFF	16K	ARM CorePac_CFG
0x01F00000 – 0x01F7FFFF	512K	AIF2 control
0x01F80000 – 0x01F8FFFF	64K	RAC_1 – FEI control
0x01F90000 – 0x01F9FFFF	64K	RAC_1 – BEI control
0x01FA0000 – 0x01FBFFFF	128K	RAC_1 – GCCP0 control
0x01FC0000 – 0x01FDFFFF	128K	RAC_1 – GCCP1 control
0x02100000 – 0x0210FFFF	64K	RAC_0 – FEI control
0x02110000 – 0x0211FFFF	64K	RAC_0 – BEI control
0x02120000 – 0x0213FFFF	128K	RAC_0 – GCCP0 control
0x02140000 – 0x0215FFFF	128K	RAC_0 – GCCP1 control
0x021C0000 – 0x021C03FF	1K	TCP3d_0
0x021C4000 – 0x021C43FF	1K	TCP3d_2
0x021C6000 – 0x021C63FF	1K	TCP3d_3
0x021C8000 – 0x021C83FF	1K	TCP3d_1
0x021D0000 – 0x021D00FF	256	VCP2_0 configuration
0x021D4000 – 0x021D40FF	256	VCP2_1 configuration
0x021D8000 – 0x021D80FF	256	VCP2_2 configuration
0x021DC000 – 0x021DC0FF	256	VCP2_3 configuration
0x021F0000 – 0x021F07FF	2K	FFTC_0 configuration
0x021F0800 – 0x021F0FFF	2K	FFTC_4 configuration
0x021F1000 – 0x021F17FF	2K	FFTC_5 configuration
0x021F4000 – 0x021F47FF	2K	FFTC_1 configuration
0x021F8000 – 0x021F87FF	2K	FFTC_2 configuration
0x021FC000 – 0x021FC7FF	2K	FFTC_3 configuration
0x02310000 – 0x023101FF	512	PLL Controller
0x0231A000 – 0x0231BFFF	8K	HyperLink0 SerDes Config
0x0231C000 – 0x0231DFFF	8K	HyperLink1 SerDes Config
0x0231E000 – 0x0231FFFF	8K	10GbE SerDes Config

Address Range	Bytes	Memory Block Description
0x02320000 – 0x02323FFF	16K	PCIE SerDes Congig
0x02324000 – 0x02325FFF	8K	AIF2 SerDes B4 Config
0x02325000 – 0x02327FFF	8K	AIF2 SerDes B8 Config
0x02328000 – 0x02328FFF	4K	DDRB PHY Config
0x02329000 – 0x02329FFF	4K	DDRA PHY Config
0x0232A000 – 0x0232BFFF	8K	SGMII SerDes Config
0x0232C000 – 0x0232CFFF	4K	SRIO SerDes Config
0x02330000 – 0x023303FF	1K	SmartReflex0
0x02330400 – 0x023307FF	1K	SmartReflex1
0x02340000 – 0x023400FF	256	VCP2_4 configuration
0x02344000 – 0x023440FF	256	VCP2_5 configuration
0x02348000 – 0x023480FF	256	VCP2_6 configuration
0x0234C000 – 0x0234C0FF	256	VCP2_7 configuration
0x02350000 – 0x02350FFF	4K	Power Sleep Controller (PSC)
0x02360000 – 0x023603FF	1K	Memory Protection Unit (MPU) 0
0x02368000 – 0x023683FF	1K	Memory Protection Unit (MPU) 1
0x02370000 – 0x023703FF	1K	Memory Protection Unit (MPU) 2
0x02378000 – 0x023783FF	1K	Memory Protection Unit (MPU) 3
0x02380000 – 0x023803FF	1K	Memory Protection Unit (MPU) 4
0x02388000 – 0x023883FF	1K	Memory Protection Unit (MPU) 5
0x02388400 – 0x023887FF	1K	Memory Protection Unit (MPU) 6
0x02388800 – 0x02388BFF	1K	Memory Protection Unit (MPU) 7
0x0238C000 – 0x02388FFF	1K	Memory Protection Unit (MPU) 8
0x02389000 – 0x023893FF	1K	Memory Protection Unit (MPU) 9
0x02389400 – 0x023897FF	1K	Memory Protection Unit (MPU) 10
0x02389800 – 0x02389BFF	1K	Memory Protection Unit (MPU) 11
0x02389C00 – 0x02389FFF	1K	Memory Protection Unit (MPU) 12
0x0238A000 – 0x0238A3FF	1K	Memory Protection Unit (MPU) 13
0x0238A400 – 0x0238A7FF	1K	Memory Protection Unit (MPU) 14
0x02440000 – 0x02443FFF	16K	DSP trace formatter 0
0x02450000 – 0x02453FFF	16K	DSP trace formatter 1
0x02460000 – 0x02463FFF	16K	DSP trace formatter 2
0x02470000 – 0x02473FFF	16K	DSP trace formatter 3
0x02480000 – 0x02483FFF	16K	DSP trace formatter 4
0x02490000 – 0x02493FFF	16K	DSP trace formatter 5
0x024A0000 – 0x024A3FFF	16K	DSP trace formatter 6
0x024B0000 – 0x024B3FFF	16K	DSP trace formatter 7
0x02530000 – 0x0253007F	128	I2C Data & Control 0
0x02530400 – 0x0253047F	128	I2C Data & Control 1
0x02530800 – 0x0253087F	128	I2C Data & Control 2
0x02530C00 – 0x02530C3F	64	UART0
0x02531000 – 0x0253103F	64	UART1
0x02540000 – 0x0255FFFF	128K	BCP

Address Range	Bytes	Memory Block Description
0x02560080 – 0x0257FFFF	128K	ARM CorePac INTC
0x02580000 – 0x025FFFFF	512K	TAC
0x02600000 – 0x02601FFF	8K	Secondary Interrupt Controller (INTC) 0
0x02604000 – 0x02605FFF	8K	Secondary Interrupt Controller (INTC) 1
0x02608000 – 0x02609FFF	8K	Secondary Interrupt Controller (INTC) 2
0x0260BF00 – 0x0260BFFF	256	GPIO Config
0x02620000 – 0x02620FFF	4K	Chip-Level Registers (boot cfg)
0x02630000 – 0x0263FFFF	64K	USB PHY Config
0x02640000 – 0x026407FF	2K	Semaphore Config
0x02680000 – 0x0268FFFF	512K	USB MMR Config
0x02700000 – 0x02707FFF	32K	EDMA Channel Controller (TPCC) 0
0x02708000 – 0x0270FFFF	32K	EDMA Channel Controller (TPCC) 4
0x02720000 – 0x02727FFF	32K	EDMA Channel Controller (TPCC) 1
0x02780000 – 0x0272FFFF	32K	EDMA Channel Controller (TPCC) 3
0x02740000 – 0x02747FFF	32K	EDMA Channel Controller (TPCC) 2
0x02760000 – 0x027603FF	1K	EDMA TPCC0 Transfer Controller (TPTC) 0
0x02768000 – 0x027683FF	1K	EDMA TPCC0 Transfer Controller (TPTC) 1
0x02770000 – 0x027703FF	1K	EDMA TPCC1 Transfer Controller (TPTC) 0
0x02778000 – 0x027783FF	1K	EDMA TPCC1 Transfer Controller (TPTC) 1
0x02780000 – 0x027803FF	1K	EDMA TPCC1 Transfer Controller (TPTC) 2
0x02788000 – 0x027883FF	1K	EDMA TPCC1Transfer Controller (TPTC) 3
0x02790000 – 0x027903FF	1K	EDMA TPCC2 Transfer Controller (TPTC) 0
0x02798000 – 0x027983FF	1K	EDMA TPCC2 Transfer Controller (TPTC) 1
0x027A0000 – 0x027A03FF	1K	EDMA TPCC2 Transfer Controller (TPTC) 2
0x027A8000 – 0x027A83FF	1K	EDMA TPCC2 Transfer Controller (TPTC) 3
0x027B0000 – 0x027B03FF	1K	EDMA TPCC3 Transfer Controller (TPTC) 0
0x027B8000 – 0x027B83FF	1K	EDMA TPCC3 Transfer Controller (TPTC) 1
0x027B8400 – 0x027B87FF	1K	EDMA TPCC4 Transfer Controller (TPTC) 0
0x027B8800 – 0x027B8BFF	1K	EEDMA TPCC4 transfer controller (TPTC) 1
0x027C4000 – 0x027C03FF	1K	BCR config
0x027D0000 – 0x027D3FFF	16K	TI Embedded Trace Buffer (TETB) core 0
0x027D4000 – 0x027D7FFF	16K	TBR ARM CorePac – Trace buffer –ARM CorePac
0x027E0000 – 0x027E3FFF	16K	TI Embedded Trace Buffer (TETB) core 1
0x027F0000 – 0x027F3FFF	16K	TI Embedded Trace Buffer (TETB) core 2
0x02800000 – 0x02803FFF	16K	TI Embedded Trace Buffer (TETB) core 3
0x02810000 – 0x02813FFF	16K	TI Embedded Trace Buffer (TETB) core 4
0x02820000 – 0x02823FFF	16K	TI Embedded Trace Buffer (TETB) core 5
0x02830000 – 0x02833FFF	16K	TI Embedded Trace Buffer (TETB) core 6
0x02840000 – 0x02843FFF	16K	TI Embedded Trace Buffer (TETB) core 7
0x02850000 – 0x02857FFF	32K	TRB_SYS-Trace Buffer-System
0x02900000 – 0x0293FFFF	256K	Serial RapidIO (SRIO) Configuration
0x02A00000 – 0x02AFFFFF	1M	Navigator Configuration

Address Range	Bytes	Memory Block Description
0x02B00000 – 0x02BFFFFF	1M	Navigator linking RAM
0x02C00000 – 0x02C0FFFF	64K	RAC_2 – FEI control
0x02C10000 – 0x02C1FFFF	64K	RAC_2 – BEI control
0x02C20000 – 0x02C3FFFF	128K	RAC_2 – GCCP 0 control
0x02C40000 – 0x02C5FFFF	128K	RAC_2 – GCCP 1 control
0x02C80000 – 0x02C8FFFF	64K	RAC_3 – FEI control
0x02C90000 – 0x02C9FFFF	64K	RAC_3 – BEI control
0x02CA0000 – 0x02CBFFFF	128K	RAC_3 – GCCP 0 control
0x02CC0000 – 0x02CDFFFF	128K	RAC_3 – GCCP 1 control
0x02F00000 – 0x02FFFFFF	1M	10Gbe Config
0x03000000 – 0x030FFFFF	1M	DBG Config
0x08000000 – 0x0801FFFF	128K	Extended Memory Controller (XMC) Configuration
0x0BC00000 – 0x0BCFFFFF	1M	Multicore Shared Memory Controller (MSMC) Config
0x0C000000 – 0x0C5FFFFF	6M	Multicore Shared Memory (MSM)
0x 10800000 – 0x 108FFFFF	1M	CorePac0 L2 SRAM
0x 10E00000 – 0x 10E07FFF	32K	CorePac0 L1P SRAM
0x 10F00000 – 0x 10F07FFF	32K	CorePac0 L1D SRAM
0x 11800000 – 0x 118FFFFF	1M	CorePac1 L2 SRAM
0x 11E00000 – 0x 11E07FFF	32K	CorePac1 L1P SRAM
0x 11F00000 – 0x 11F07FFF	32K	CorePac1 L1D SRAM
0x 12800000 – 0x 128FFFFF	1M	CorePac2 L2 SRAM
0x 12E00000 – 0x 12E07FFF	32K	CorePac2 L1P SRAM
0x 12F00000 – 0x 12F07FFF	32K	CorePac2 L1D SRAM
0x 13800000 – 0x 1388FFFF	1M	CorePac3 L2 SRAM
0x 13E00000 – 0x 13E07FFF	32K	CorePac3 L1P SRAM
0x 13F00000 – 0x 13F07FFF	32K	CorePac3 L1D SRAM
0x 14800000 – 0x 148FFFFF	1M	CorePac4 L2 SRAM
0x 14E00000 – 0x 14E07FFF	32K	CorePac4 L1P SRAM
0x 14F00000 – 0x 14F07FFF	32K	CorePac4 L1D SRAM
0x 15800000 – 0x 158FFFFF	1M	CorePac5 L2 SRAM
0x 15E00000 – 0x 15E07FFF	32K	CorePac5 L1P SRAM
0x 15F00000 – 0x 15F07FFF	32K	CorePac5 L1D SRAM
0x 16800000 – 0x 168FFFFF	1M	CorePac6 L2 SRAM
0x 16E00000 – 0x 16E07FFF	32K	CorePac6 L1P SRAM
0x 16000000 – 0x 16F07FFF	32K	CorePac6 L1D SRAM
0x 17800000 – 0x 178FFFFF	1M	CorePac7 L2 SRAM
0x 17E00000 – 0x 17E07FFF	32K	CorePac7 L1P SRAM
0x 17F00000 – 0x 17F07FFF	32K	CorePac7 L1D SRAM
0x20000000 – 0x200FFFFF	1M	System Trace Manager (STM) Configuration
0x 20600000 – 0x 206FFFFF	1M	Turbo Decoder Coprocessor_1(TCP3d_1) data
0x 20700000 – 0x 207FFFFF	1M	TCP3d_2 data

Address Range	Bytes	Memory Block Description
0x 20800000 – 0x 208FFFFF	1M	TCP3d_0 data
0x 20900000 – 0x 209FFFFF	1M	TCP3d_3 data
0x 20B00000 – 0x 20B3FFFF	256	Boot ROM
0x 21004000 – 0x 210005FF	512	SPI0
0x 21006000 – 0x 210007FF	512	SPI1
0x 21008000 – 0x 210009FF	512	SPI2
0x 21000000 – 0x 21000AFF	256	AEMIF Configuration
0x 21010000 – 0x 210101FF	512	DDR3A EMIF Configuration
0x 21020000 – 0x 2103FFFF	128K	DDR3B EMIF Configuration
0x21400000 – 0x214000FF	256	HyperLink0 Configuration
0x21400100 – 0x214001FF	256	HyperLink1 Configuration
0x21800000 – 0x21807FFF	32K	PCIe Configuration
0x22B00000 – 0x22B0FFFF	64K	VCP2_1 Data
0x22C00000 – 0x22C0FFFF	64K	VCP2_2 Data
0x22D00000 – 0x22D0FFFF	64K	VCP2_3 Data
0x22E00000 – 0x22E0FFFF	64K	VCP2_4 Data
0x22F00000 – 0x22F0FFFF	64K	VCP2_5 Data
0x23000000 – 0x2300FFFF	64K	VCP2_6 Data
0x23100000 – 0x2310FFFF	64K	VCP2_7 Data
0x23200000 – 0x2324FFFF	384K	TAC_BEI
0x23A00000 – 0x23BFFFFF	2M	Navigator
0x23C00000 – 0x23FFFFFF	4M	BCR-RAC data
0x28000000– 0x2FFFFFFF	128M	HyperLink1 data
0x30000000 – 0x33FFFFFF	64M	EMIF16 CS2 Data NAND Memory
0x34000000 – 0x37FFFFFF	64M	EMIF16 CS3 Data NAND Memory
0x38000000 – 0x3BFFFFFF	64M	EMIF16 CS4 Data NOR Memory
0x3C000000 – 0x3FFFFFFF	64M	EMIF16 CS5 Data SRAM Memory
0x40000000 – 0x4FFFFFFF	256M	HyperLink0 data
0x50000000 – 0x5FFFFFFF	256M	PCIe Data
0x60000000 – 0x7FFFFFFF	512M	DDR3B_ Data
0x80000000 – 0xFFFFFFFF	2G	DDR3B_ Data
0x01 21000000 – 0x01 210001FF	512	DDR3A_ EMIF configuration
0x08 F0000000 – 0x09 FFFFFFFF	8G	DDR3A_ Data

2.2 EVM Boot Mode

The EVM has one configuration DIP switch: (SW1) that can set up to 16 different pre-defined configurations to the BMC. Each DIP configuration results in the BMC latching in a different boot mode when the SoC RESETFULL reset signal is de-asserted. This occurs when power is applied the board, after the user presses the MCU_RESET push button or after a POR reset is requested from the MMC.

SW1 determines general DSP configuration, Little or Big Endian mode as well as boot mode selection.

More information about using these DIP switches is contained in Section 3.3 of this document. For more information on DSP supported Boot Modes, refer to SoC Data Manual and C66x Boot Loader User Guide.

2.3 JTAG - Emulation Overview

The EVM includes the **XDS200** mezzanine card which provides JTAG emulation circuitry; hence users do not require any external emulator to connect EVM with Code Composer Studio. Users can connect CCS with the target SoC on the EVM through the USB cable supplied along with this board.

In case users wish to connect an external emulator to the EVM, the MIPI 60-pin JTAG header (EMU1) is provided for high speed, real-time emulation. The MIPI 60-pin JTAG supports all standard TI SoC emulators. An adapter will be required for use with some emulators.

The on-board embedded JTAG emulator is the default connection to the SoC However when an external emulator is connected to EVM, the board circuitry switches automatically to give emulation control to the external emulator.

When the on-board emulator and external emulator both are connected at the same time, the external emulator has priority and the on-board emulator is disconnected from the SoC.

The third way of accessing the SoC is through the JTAG port on the AMC edge connector, users can connect the SoC through the AMC backplane if they don’t use the 60-pin header with the external emulator.

The JTAG interface among the SoC, external emulator and the AMC edge connector is shown in the below figure.

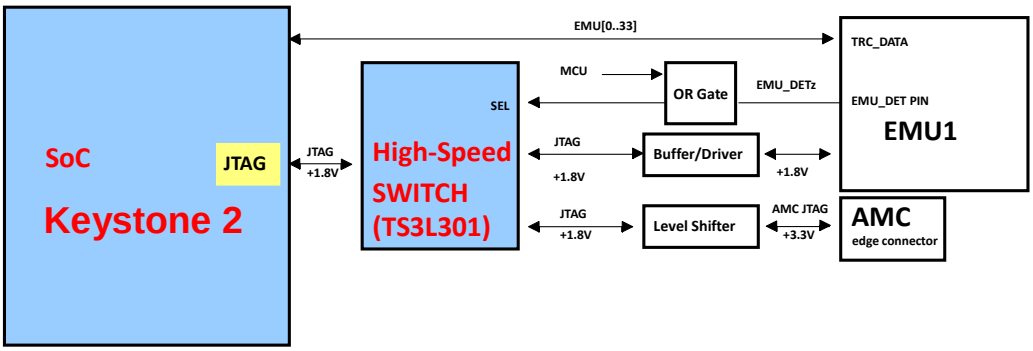


Figure 2.1: EVM JTAG emulation

2.4 Clock Domains

The EVM incorporates a variety of clocks to the SoC as well as other devices which are configured automatically during the power up configuration sequence. The figure below illustrates clocking for the system in the EVM module.

A new feature on the Rev 1.0 EVM board supports external clock reference. This is needed for some applications using the HyperLink SERDES interface. The external reference clock is driven into the clock generation device rather than using the local crystal.

For the timing synchronization on the HyperLink SERDES, a common 25MHz timing source is fed from the AMC edge finger to the clock generator, CLK3, that drives a 100MHz source clock for the DDR3A&B_CLK input on the SoC. It is supplied on the AMC connector at the TCLKB input.

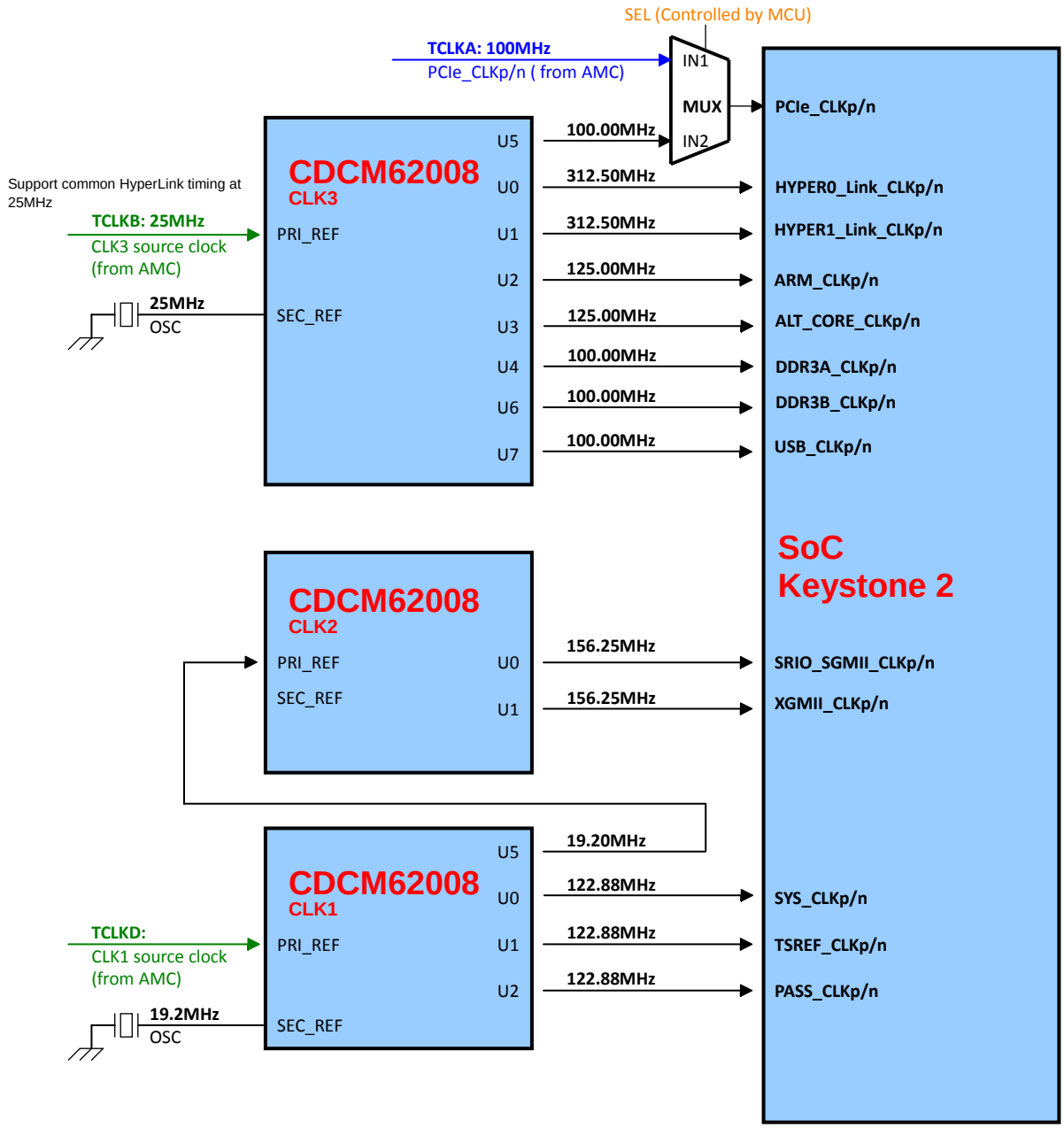


Figure 2.2: EVM Clock Domains

2.5 I2C Boot EEPROM / SPI NOR Flash

The I2C modules on the SoC may be used by the SoC to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one EEPROM and to the 120-pin expansion header (CN3). There are two banks in the I2C EEPROM which respond separately at addresses 0x50 and 0x51. These banks can be loaded with demonstration programs. Currently, the bank at 0x50 contains the I2C boot code and PLL initialization procedure and the bank at 0x51 contains

the second level boot-loader program. The second level boot-loader can be used to run the POST program or launch the OOB demonstration from NOR flash memory.

The serial peripheral interconnect (SPI) module provides an interface between the SoC and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on SoC is supported only in Master mode.

The NOR FLASH attached to CS0z on the SoC is a NUMONYX N25Q128A11. This NOR FLASH size is 16MB. It can contain demonstration programs such as POST or the OOB demonstration. The CS0z of the SPI is used by the DSP to access registers within the MCU.

2.6 MCU

The MCU (TI LMS2D93) controls the reset mechanism of the SoC and provides boot mode and boot configuration data to the SoC through SW1. MCU also provides the transformation of TDM Frame Sync and Clock between AMC connector and the SoC. The MCU also supports 3 user LEDs and 1 user switch through control registers. All MCU registers are accessible over the SPI interface.

The EVM also supports a limited set of Intelligent Platform Management Interface (IPMI) commands using Microcontroller based on Texas Instruments LMS2D93.

The MCU will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 R1.0 compliant chassis. The primary purpose of the MCU is to provide necessary information to MCH, to enable the payload power to EVM EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED (D5) and Red LED(D3) on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the MCU will receive management power.

Blue LED (D5):

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED will turn OFF when payload power is enabled to the EVM by the MCH.

Red LED (D3):

Red colored D3 will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

The figure below shows the interface between SoC and MCU.

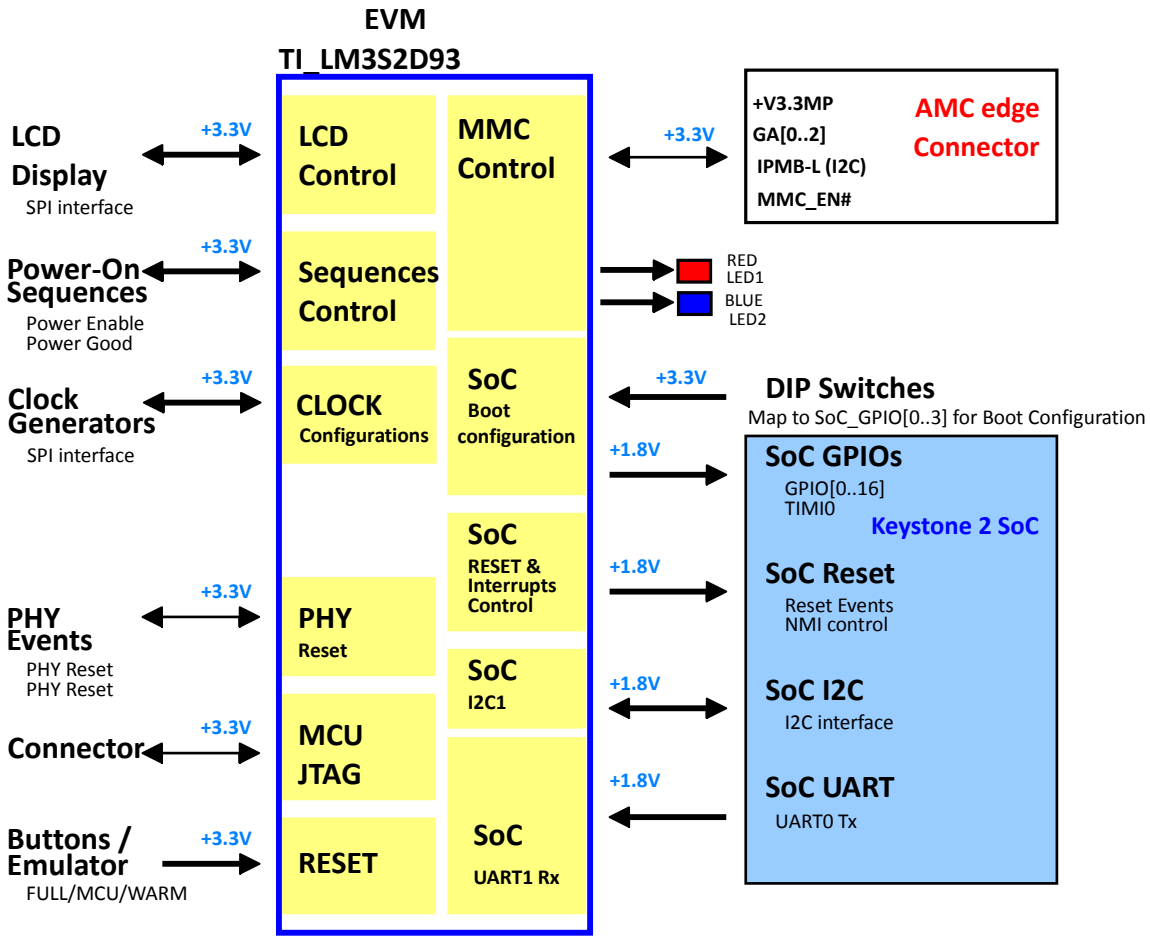


Figure 2.3: EVM MCU Connections

2.7 Gigabit Ethernet Connections

The EVM provides connectivity for both SGMII Gigabit Ethernet ports on the EVM. These are shown in figure below:

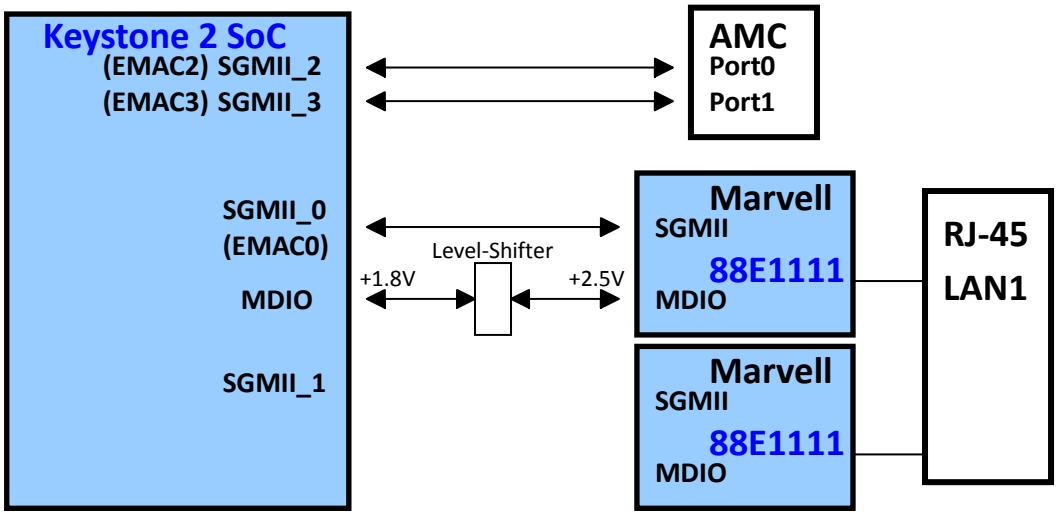


Figure 2.4: EVM Ethernet Routing

The Ethernet PHY (PHY1 and PHY2) is connected to SoC EMAC0 & 1 to provide a copper interface and routed to a Gigabit RJ-45 connector (LAN1). The EMAC2 & 3 of SoC is routed to Port0 & 1 of the AMC edge connector backplane interface.

2.8 Serial RapidIO (SRIO) Interface

The EVM supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total 4 RapidIO ports available on SoC . All SRIO ports are routed to AMC edge connector on board. Below figure shows RapidIO connections between the DSP and AMC edge connector.

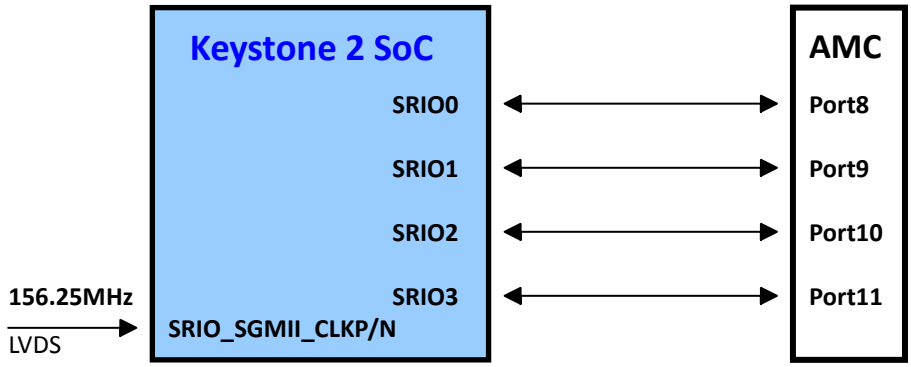


Figure 2.5: EVM SRIO Port Connections

2.9 DDR3 External Memory Interface

The EVM have Doubled **DDR3 interface** connects to one expansion SO-DIMM Socket on Rev 1.0 EVM and four 2Gbit (128Mega x 16) DDR3 1600 devices on Rev 1.0 EVM or 4Gbit (256Mega X 16) DDR3 devices on Rev 2.0 EVM. This configuration allows the use of both “narrow (16-bit)”, “normal (32-bit)”, and “wide (64-bit)” modes of the DDR3 EMIF.

SAMSUNG DDR3 K4B2G1646E-BCK0 SDRAMs (128Mx16; 800MHz) are used on the DDR3 EMIF on Rev 1.0 EVM and the K4B4G1646B-HCK0 chips (256Mx16; 800MHz) are installed on Rev 2.0 and later revision EVMs.

The figure 2.6 illustrates the implementation for the DDR3 SDRAM memory on Rev 1.0 EVM. Please note that the size of DDR3 memory is 2GB with four 4Gb chips on Rev 2.0 and later EVMs instead.

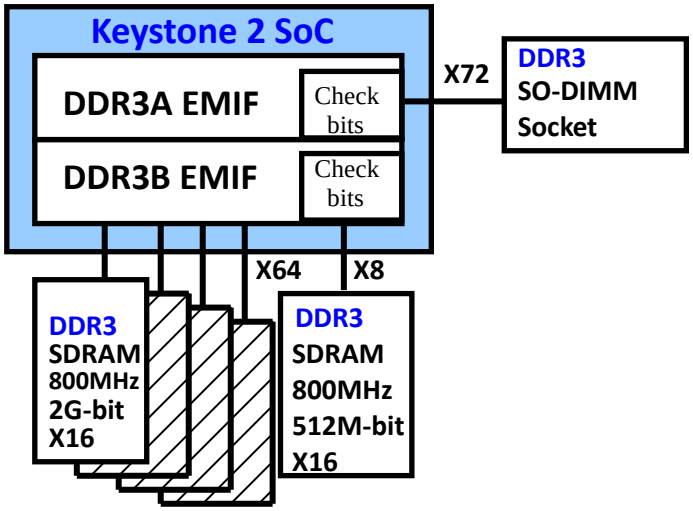


Figure 2.6: EVM SDRAM

2.10 16-bit Asynchronous External Memory Interface (EMIF-16)

The SoC **EMIF-16** interface connects to one 4Gbit (512MB) NAND flash device and 120-pin expansion header (CN3) on the EVM. The EMIF16 module provides an interface between SoC and asynchronous external memories such as NAND and NOR flash. For more information, see the External Memory Interface (EMIF16) for KeyStone Devices User Guide (literature number SPRUGZ3).

Micron MT29F4G08ABBDAHC NAND flash (512MB) is used on the EMIF-16.

The figure 2.7 illustrates the EMIF-16 connections on the EVM.

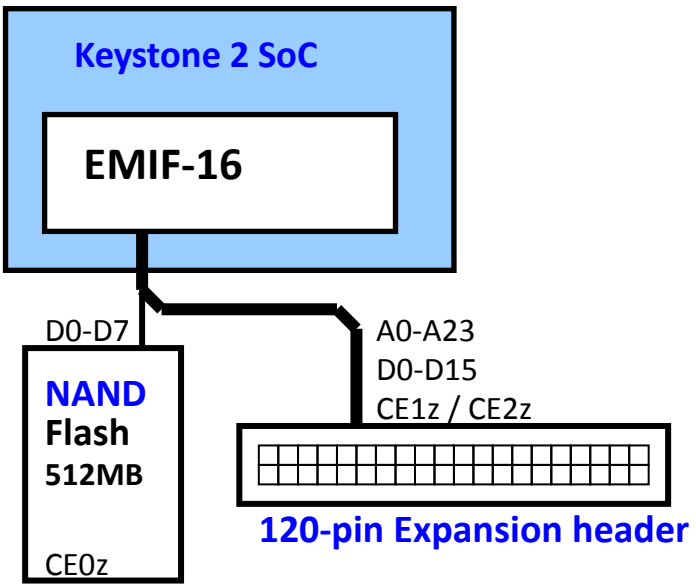


Figure 2.7: EVM EMIF-16 connections

2.11 HyperLink Interface

The SoC provides the TWO HyperLink bus for companion chip/die interfaces. Each group have a four-lane SerDes interface designed to operate at 12.5 Gbps per lane from pin-to-pin. The interface is used to connect with external accelerators.

The interface includes the Serial Station Management Interfaces used to send power management and flow messages between devices. This consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire output buses and two 2-wire input buses. Each 2-wire bus includes a data signal and a clock signal.

The figure 2.8 illustrates the Hyperlink bus connections on the EVM.

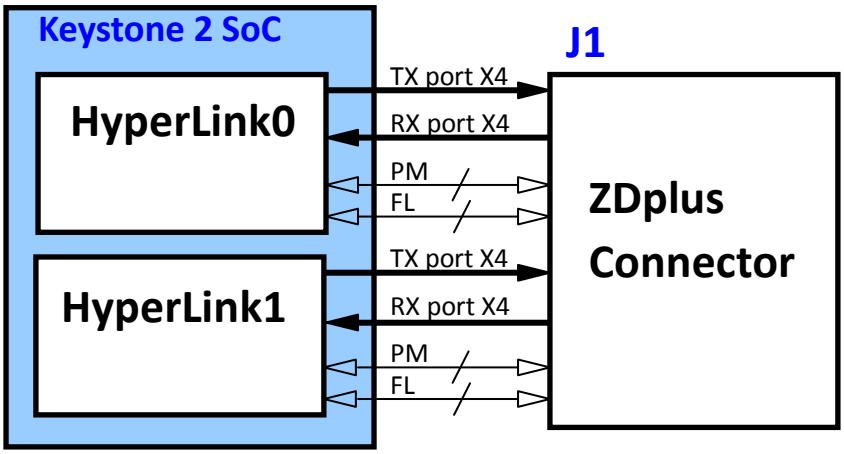


Figure 2.8: EVM HyperLink connections

2.12 PCIe Interface

The 2 lane PCI express (PCIe) interface on EVM provides a connection between the SoC and AMC edge connector. The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide (literature number SPRUGS6).

The EVM provides the PCIe connectivity to AMC backplane on the EVM, this is shown in figure 2.9.

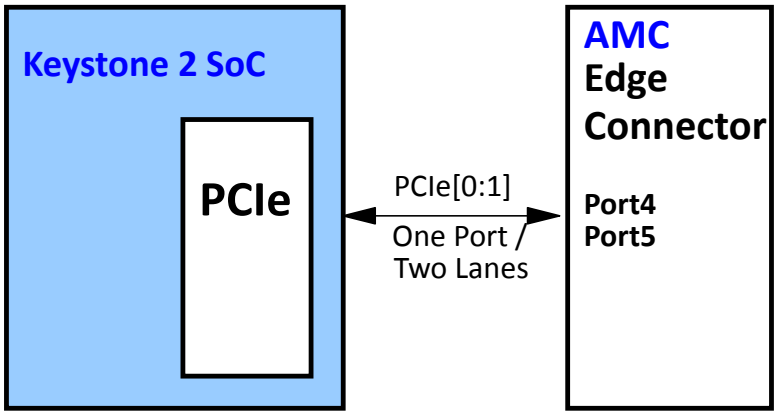


Figure 2.9: EVM PCIE Port Connections

2.13 Antenna Interface 2 (AIF2)

The AIF2 transfers data between the external RF units and the C66x CorePacs,RAC,TAC,and the FFTC modules via the TeraNet. For more information, see the Antenna Interface 2 (AIF2) for the keystone II Devices User Guide (literature number SPRUGV7).

The Six-lane SerDes-Baded AIF2 interface on EVM provides a connection between the SoC and AMC edge connector and ZDplus connector. The AIF2 interface provides high-speed data transfer at rates of 6.144 Gbps per lane on the serial links.

The figure 2.10 illustrates the AIF2 connections on the EVM. The AIF2 port[0:3] connectivity to ZDplus backplane and AIF2 port[4:5] connectivity to AMC backplane.

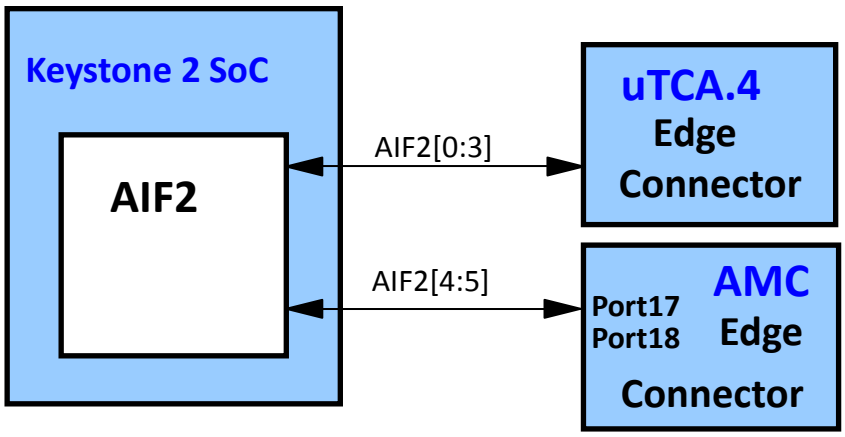


Figure 2.10: EVM AIF2 connections

2.14 UART Interface

A serial port is provided for UART communication by SoC . This serial port can be accessed either through USB connector (FTDI_USB) or through 4-pin (Tx, Rx ,detect and Gnd) serial port header (SOC & MCU). The selection can be made through UART Cable detect signal to Selector.

The figure 2.11 illustrates the UART connections on the EVM.

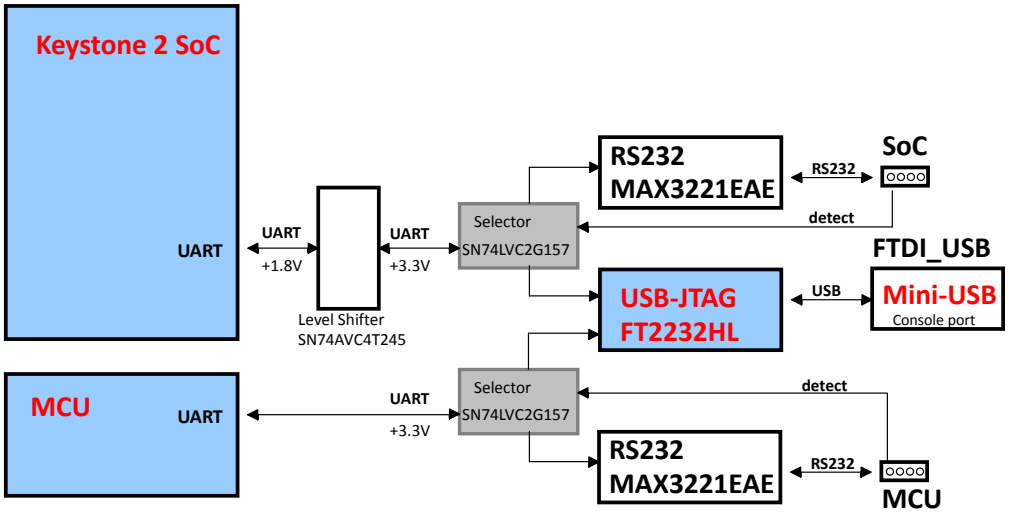


Figure 2.11: EVM UART Connections

2.15 XFI (10-GbE)

Not supported on all EVMs.

The EVM provides connectivity for both XFI 10-Gigabit Ethernet ports on the EVM. For more information, see the Gigabit Ethernet (GbE) Switch Subsystem (10 GB) for KeyStone II Devices User Guide (literature number SPRUHJ5).These are shown in figure below:

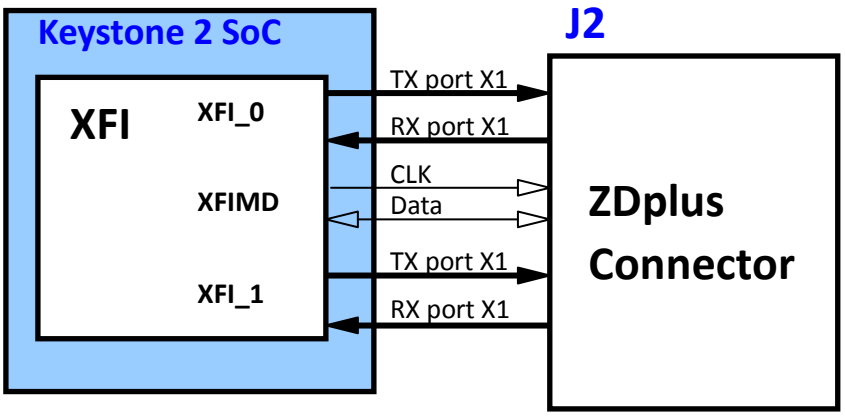


Figure 2.12: EVM XFI Connections

2.16 Expansion Header

The EVM contains an 120-pin header (CN3) which has EMIF, I2C, TIMI[1:0], TIMO[0:1], SPI, GPIO[16:0] and UART signal connections. It should be noted that EMIF, I2C, TIMI[1:0], TIMO[0:1], and SPI, GPIO[16:0] connections to this header (CN3) are of 1.8V level whereas UART signals are of 3.3V level.

2.17 Universal Serial Bus 2.0/3.0(USB2.0/3.0)

The EVM supports new peripherals that have been added include the USB2.0/3.0 controller. There are total one USB ports available on SoC . The USB ports are routed to USB3.0 connector on board and data transfer at rates of 5.0 Gbps on the serial links.For more information, see the Universal Serial Bus 3 (USB3) for KeyStone II Devices User Guide (literature number SPRUHJ7).Below figure shows USB connections between the SoC and USB3.0 connector.

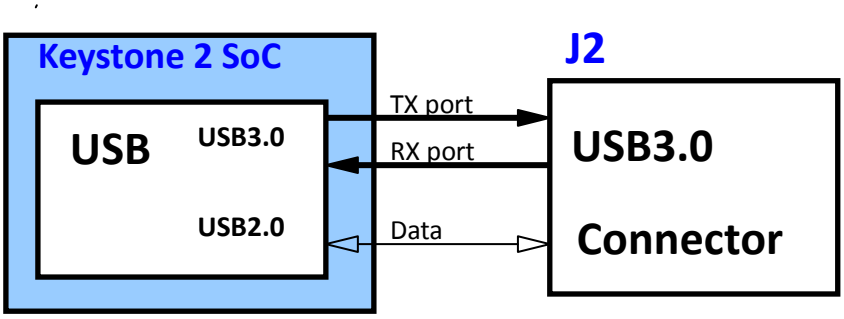


Figure 2.13: EVM USB3.0 Connections

3. EVM Board Physical Specifications

This chapter describes the physical layout of the EVM board and its connectors, switches and test points. It contains:

3.1 Board Layout

The EVM board dimension is 7.14” x 5.84” (181.5mm x 148.5mm). It is a 12-layer board and powered through connector DC_IN1. Figure 3-1 and 3-2 shows assembly layout of the EVM Board.

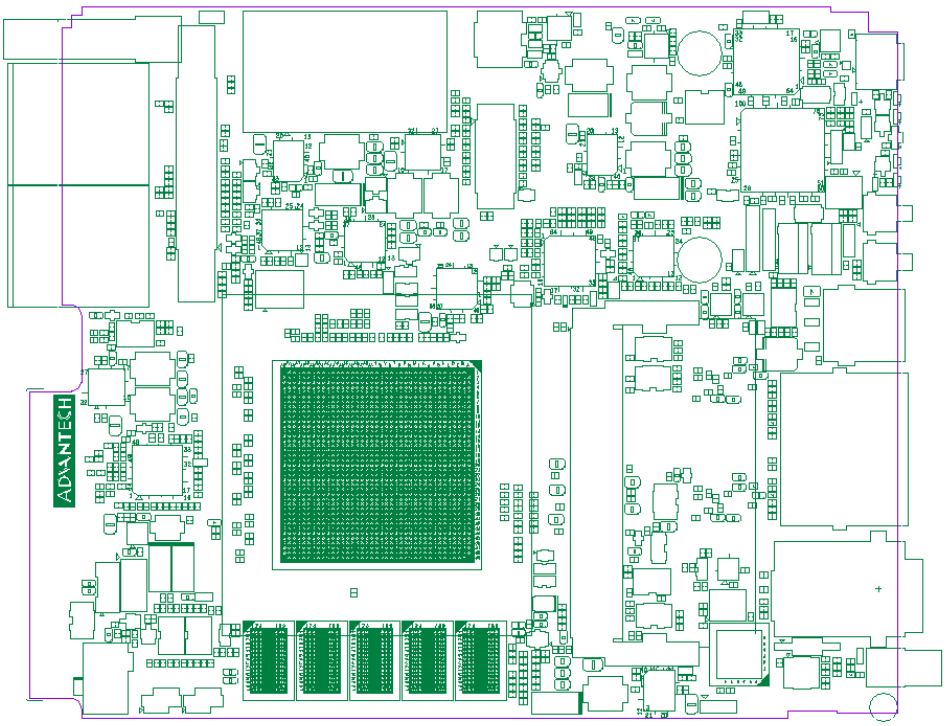


Figure 3.1: EVM Board Assembly Layout – TOP view

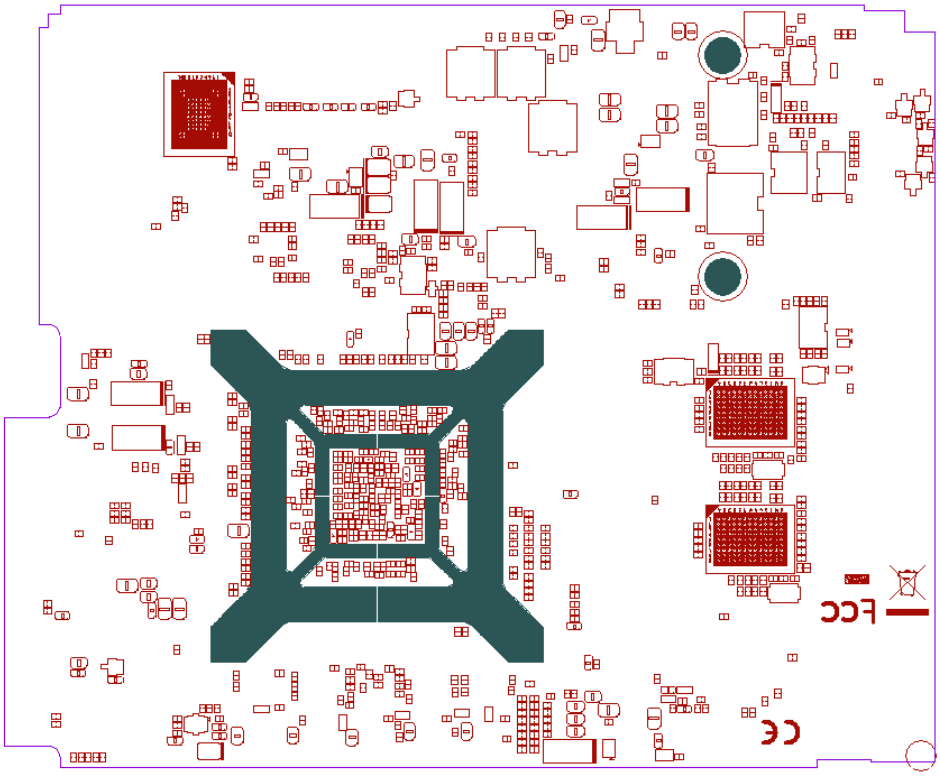


Figure 3.2: EVM Board layout – Bottom view

3.2 Connector Index

The EVM Board has several connectors which provide access to various interfaces on the board.

Table 3.1 : EVM Board Connectors

Connector	Pins	Function
AMC1	170	AMC Edge Connector
CN2	3	MCU VBAT Supply
CN3	120	EMIF, SPI, I2C, GPIO, TIMI[1:0], TIMO[1:0], and UART1 connections
CN8	3	MCU wake up
CN9	2	MCU Boot select
CN15	2	EXT TIMO1 and EXTRAMEEVENT test pin
CN16	33	Gigabit Ethernet RJ-45 Connector
CN17	8	Synchronization Event
CN18	5	GPS Input
CN19	4	Smart Reflex test pin
CN20	4	Reserve
CN21	3	SIM Power Value Select pin
CN22	10	MCU JTAG Connector

CN24	2	Standby Power Control for UCD9090 Flash
DIMM1	204	DDR3 SO-DIMM Socket
DC_IN1	3	DC Power Input Jack Connector
EMU1	60	MIPI 60-Pin SoC JTAG Connector
FAN1	4	FAN connector for +12V DC FAN
FTDI_USB	5	Mini-USB Connector
J1	160	uTCA.4 Edge Connector for Hyperlink SerDes
J2	160	uTCA.4 Edge Connector for XFI and AIF
MCU,SoC	4	UART 3-Pin Connector
PMBUS1	5	PMBUS for Smart-Reflex connected to UCD9244 and Power Sequence control connected to UCD9090
SoC_USB	9	USB3.0 TypeA
SIM1	8	USIM Connector

3.2.1 AMC1, AMC Edge Connector

The AMC card edge connector plugs into an AMC compatible carrier board and provides 4 Serial RapidIO lanes, 2 PCIe lanes, 2 SGMII port, 2 AIF lanes and system interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below:

Table 3.2: AMC Edge Connector

Pin	Signal	Pin	Signal
1	GND	170	GND
2	VCC12	169	AMC_JTAG_TDI
3	MMC_PS_N1#	168	AMC_JTAG_TDO
4	VCC3V3_MP_AMC	167	AMC_JTAG_RST#
5	MMC_GA0	166	AMC_JTAG_TMS
6	RSVD	165	AMC_JTAG_TCK
7	GND	164	GND
8	RSVD	163	AMC_RP1CLKP
9	VCC12	162	AMC_RP1CLKN
10	GND	161	GND
11	AMC0_SGMII2_TX_DP	160	EXP_SCL2_3V3
12	AMC0_SGMII2_TX_DP	159	EXP_SDA2_3V3
13	GND	158	GND
14	AMC0_SGMII2_RX_DP	157	AMC_RP1FBP
15	AMC0_SGMII2_RX_DN	156	AMC_RP1FBN
16	GND	155	GND
17	MMC_GA1	154	PHYSYNC
18	VCC12	153	RADSYNC
19	GND	152	GND

Pin	Signal	Pin	Signal
20	AMC0_SGMII3_TX_DP	151	AMCC_P18_AIF5_TXP
21	AMC0_SGMII3_TX_DP	150	AMCC_P18_AIF5_TXN
22	GND	149	GND
23	AMC0_SGMII3_RX_DP	148	AMCC_P18_AIF5_RXP
24	AMC0_SGMII3_RX_DN	147	AMCC_P18_AIF5_RXN
25	GND	146	GND
26	MMC_GA2	145	AMCC_P18_AIF4_TXP
27	VCC12	144	AMCC_P18_AIF4_TXN
28	GND	143	GND
29	NC	142	AMCC_P18_AIF4_RXP
30	NC	141	AMCC_P18_AIF4_RXN
31	GND	140	GND
32	NC	139	TCLKD_P
33	NC	138	TCLKD_N
34	GND	137	GND
35	NC	136	AMC_TIMO0
36	NC	135	SOC_TIMO0
37	GND	134	GND
38	NC	133	NC
39	NC	132	NC
40	GND	131	GND
41	MMC_ENABLE_N	130	NC
42	VCC12	129	NC
43	GND	128	GND
44	AMCC_P4_PCIe_TX1P	127	NC
45	AMCC_P4_PCIe_TX1N	126	NC
46	GND	125	GND
47	AMCC_P4_PCIe_RX1P	124	NC
48	AMCC_P4_PCIe_RX1N	123	NC
49	GND	122	GND
50	AMCC_P5_PCIe_TX2P	121	NC
51	AMCC_P5_PCIe_TX2N	120	NC
52	GND	119	GND
53	AMCC_P5_PCIe_RX2P	118	NC
54	AMCC_P5_PCIe_RX2N	117	NC
55	GND	116	GND
56	SMB_SCL_IPMBL	115	NC
57	VCC12	114	NC
58	GND	113	GND
59	NC	112	NC
60	NC	111	NC
61	GND	110	GND
62	NC	109	AMCC_P11_SRIO4_TXP
63	NC	108	AMCC_P11_SRIO4_TXN
64	GND	107	GND

Pin	Signal	Pin	Signal
65	NC	106	AMCC_P11_SRIO4_RXP
66	NC	105	AMCC_P11_SRIO4_RXN
67	GND	104	GND
68	NC	103	AMCC_P10_SRIO3_TXP
69	NC	102	AMCC_P10_SRIO3_TXN
70	GND	101	GND
71	SMB_SDA_IPMBL	100	AMCC_P10_SRIO3_RXP
72	VCC12	99	AMCC_P10_SRIO3_RXN
73	GND	98	GND
74	NC	97	AMCC_P9_SRIO2_TXP
75	NC	96	AMCC_P9_SRIO2_TXN
76	GND	95	GND
77	TCLKB_P	94	AMCC_P9_SRIO2_RXP
78	TCLKB_N	93	AMCC_P9_SRIO2_RXN
79	GND	92	GND
80	PCIe_REF_CLK_P	91	AMCC_P8_SRIO1_TXP
81	PCIe_REF_CLK_N	90	AMCC_P8_SRIO1_TXN
82	GND	89	GND
83	MMC_PS_N0	88	AMCC_P8_SRIO1_RXP
84	VCC12	87	AMCC_P8_SRIO1_RXN
85	GND	86	GND

3.2.2 CN2, MCU VBAT Supply

CN2 is 3-pin male connector for MCU Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply. A jumper to pull up VCC3V3_MP is supplied with EVM to normal work.

Table 3.3: VBAT Supply Connector pin out

Pin #	Signal Name
1	VCC3V3_MP
2	VBAT
3	Ground

3.2.3 CN3, Expansion Header (EMIF-16, SPI, GPIO, Timer I/O, I2C, and UART)

CN3 is an expansion header for several interfaces on the SoC. They are 16-bit EMIF, SPI, GPIO, Timer, I2C, and UART. The signal connections to the test header are as shown in a table below:

Table 3.4 : Expansion Header pin out

Pin	Signal	Description	Pin	Signal	Description
1	VCC1V8	1.8V Supply	2	VCC1V8	1.8V Supply
3	GND	Ground	4	GND	Ground
5	EXP_SDA_3V3	SoC I2C data	6	SoC_EMIFA00	EMIF addr0
7	EXP_SCL_3V3	SoC I2C clock	8	SoC_EMIFA01	EMIF addr1
9	SoC_EMIFD0	EMIF data0	10	SoC_EMIFA02	EMIF addr2
11	SoC_EMIFD1	EMIF data1	12	SoC_EMIFA03	EMIF addr3
13	SoC_EMIFD2	EMIF data2	14	SoC_EMIFA04	EMIF addr4
15	SoC_EMIFD3	EMIF data3	16	SoC_EMIFA05	EMIF addr5
17	SoC_EMIFD4	EMIF data4	18	SoC_EMIFA06	EMIF addr6
19	SoC_EMIFD5	EMIF data5	20	SoC_EMIFA07	EMIF addr7
21	SoC_EMIFD6	EMIF data6	22	SoC_EMIFA08	EMIF addr8
23	SoC_EMIFD7	EMIF data7	24	SoC_EMIFA09	EMIF addr9
25	SoC_EMIFD8	EMIF data8	26	SoC_EMIFA10	EMIF addr10
27	SoC_EMIFD9	EMIF data9	28	SoC_EMIFA11	EMIF addr11
29	SoC_EMIFD10	EMIF data10	30	SoC_EMIFA12	EMIF addr12
31	SoC_EMIFD11	EMIF data11	32	SoC_EMIFA13	EMIF addr13
33	SoC_EMIFD12	EMIF data12	34	SoC_EMIFA14	EMIF addr14
35	SoC_EMIFD13	EMIF data13	36	SoC_EMIFA15	EMIF addr15
37	SoC_EMIFD14	EMIF data14	38	SoC_EMIFA16	EMIF addr16
39	SoC_EMIFD15	EMIF data15	40	SoC_EMIFA17	EMIF addr17
41	NC	Reserve	42	SoC_EMIFA18	EMIF addr18
43	SoC_EMIFCE1z	EMIF Space Enable1	44	SoC_EMIFA19	EMIF addr19
45	SoC_EMIFCE2z	EMIF Space Enable2	46	SoC_EMIFA20	EMIF addr20
47	SoC_EMIFCE3z	EMIF Space Enable3	48	SoC_EMIFA21	EMIF addr21
49	SoC_EMIFBE0z	EMIF Byte Enable0	50	SoC_EMIFA22	EMIF addr22
51	SoC_EMIFBE1z	EMIF Byte Enable1	52	SoC_EMIFA23	EMIF addr23
53	SoC_EMIFOEz	EMIF Output Enable	54	SoC_GPIO_00	SoC GPIO0
55	SoC_EMIFWEz	EMIF Write Enable	56	SoC_GPIO_01	SoC GPIO1
57	GND	Ground	58	GND	Ground
59	VCC5	5V Supply	60	VCC5	5V Supply
61	VCC3V3_AUX	3.3V Supply	62	VCC3V3_AUX	3.3V Supply
63	GND	Ground	64	GND	Ground
65	SoC_EMIFRNW	EMIF Read/Write	66	SoC_GPIO_02	SoC GPIO2
67	NC	Reserve	68	SoC_GPIO_03	SoC GPIO3
69	SoC_EMIFWAIT1	EMIF Wait	70	SoC_GPIO_04	SoC GPIO4
71	SoC_TIMO0	Timer input 0	72	SoC_GPIO_05	SoC GPIO5
73	EXP_TIMO0	Timer output 0	74	SoC_GPIO_06	SoC GPIO6
75	SoC_TIMO1	Timer input 1	76	SoC_GPIO_07	SoC GPIO7
77	EXP_TIMO1	Timer output 1	78	SoC_GPIO_08	SoC GPIO8
79	SoC_SSP2_MOSI	SPI data input	80	SoC_GPIO_09	SoC GPIO9
81	SoC_SSP2_MISO	SPI data output	82	SoC_GPIO_10	SoC GPIO10
83	SoC_SSP2_CS0	SPI chip select	84	SoC_GPIO_11	SoC GPIO11
85	SoC_SSP2_CS1	SPI chip select	86	SoC_GPIO_12	SoC GPIO12
87	SoC_SSP2_CS2	SPI chip select	88	SoC_GPIO_13	SoC GPIO13
89	SoC_SSP2_CS3	SPI chip select	90	SoC_GPIO_14	SoC GPIO14
91	SoC_SSP2_CLK	SPI clock	92	SoC_GPIO_15	SoC GPIO15
93	EXP_UART1_TXD_3V3	UART Serial Data Out (+3.3v)	94	SoC_GPIO_16	SoC GPIO16
95	EXP_UART1_RXD_3V3	UART Serial Data In (+3.3v)	96	EXP_TP0	Test point
97	SoC_UARTRTS	UART Request To	98	EXP_TP1	MCU Resetstatz

Pin	Signal	Description	Pin	Signal	Description
		Send (+3.3v)			
99	SoC_UARTCTS	UART Cear To Send (+3.3v)	100	EXP_TP2	EXT_PS#
101	TSRX_CLK0N	SerDes recovered clock for SyncE	102	BD_PRESENT	Board Present
103	TSRX_CLK0P	SerDes recovered clock for SyncE	104	BD_ID0	Board ID
105	TSRX_CLK1N	SerDes recovered clock for SyncE	106	BD_ID1	Board ID
107	TSRX_CLK1P	SerDes recovered clock for SyncE	108	BD_ID2	Board ID
109	TSPUSHEVt0_E	PPS push event from GPS for IEEE1588	110	RSV_CLKN	Output Clock
111	TSPUSHEVt1_E	Push event from BCN for IEEE1588	112	RSV_CLKP	Output Clock
113	TSCOMPOUT_E	IEEE1588 compare output.	114	TSPUSHEVt0	PPS push event from GPS for IEEE1588
115	TSSYNCEVT_E	IEEE1588 sync event output.	116	TSCOMPOUT_E	IEEE1588 compare output.
117	GND	Ground	118	GND	Ground
119	VCC3V3_AUX	3.3V Supply	120	VCC3V3_AUX	3.3V Supply

3.2.4 CN8, MCU wake up

CN8 is 3-pin male connector for MCU wake up from sleep mode. It is through jumper to enable .Normally is jumper to GND.

Table 3.5: wake up Connector pin out

Pin #	Signal Name
1	FULL_RESETz
2	MCU_WAKEz
3	Ground

3.2.5 CN9, MCU Boot select

CN9 is 2-pin male connector for MCU boot select. It is through jumper to enable .Normally is jumper to GND.

Table 3.6: wake up Connector pin out

Pin #	Signal Name
1	MCU_Bootselect
2	Ground

3.2.6 CN15, EXT TIMO1 and EXTRAMEEVENT test pin

CN15 is 2-pin male connector for Timer and Frame sync clock output external measurement.

Table 3.7: EXT TIM01 and EXTRAMEEVENT test pin out

Pin #	Signal Name
1	EXT_TIMO1
2	EXTFRAMEEVENT

3.2.7 CN16, Ethernet Connector

CN16 is double Gigabits RJ45 Ethernet connector with integrated magnetics. It is driven by Two Marvell Gigabit Ethernet transceiver 88E1111. The connections are shown in the table below:

Table 3.8 : Ethernet Connector pin out

Pin #	Signal Name	Pin #	Signal Name
A1	LAN0 MD0+	B1	LAN1 MD0+
A2	LAN0 MD0-	B2	LAN1 MD0-
A3	LAN0 MD1+	B3	LAN1 MD1+
A4	LAN0 MD1-	B4	LAN1 MD1-
A5	Center Tap	B5	Center Tap
A6	GND	B6	GND
A7	LAN0 MD2+	B7	LAN1 MD2+
A8	LAN0 MD2-	B8	LAN1 MD2-
A9	LAN0 MD3+	B9	LAN1 MD3+
A10	LAN0 MD3-	B10	LAN1 MD3-
A11	LAN0 ACT_LED1-	B11	LAN1 ACT_LED1-
A12	LAN0 ACT_LED1+	B12	LAN1 ACT_LED1+
A13	LAN0 LINK100_LED2	B13	LAN1 LINK100_LED2
A14	LAN0 LINK1000_LED2	B14	LAN1 LINK1000_LED2
H1	Shield 1	H2	Shield 2
H3	Shield 3	H4	Shield 4

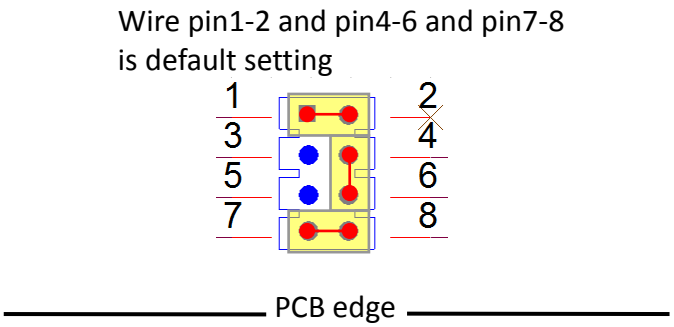
3.2.8 CN17, Synchronization Event

CN17 is 5-pin male header for synchronization event signal. The connections are shown in the table below:

Table 3.9: Sync Evant Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	GPS_PPS	2	NC
3	TSPUSHEVt0	4	SOC_TIMO1
5	TSCOMPOUT_E	6	RADSYNC
7	TSCOMPOUT_E	8	PHYSYNC

Figure 3.3: Sync Event Jumper setting



3.2.9 CN18, GPS Input SMA Jack

CN18 is 8-pin SMA Jack for GPS input signal. The connections are shown in the table below:

Table 3.10: Sync Event Connector pin out

Pin #	Signal Name
1	GPS_RF
2 -5	Ground

3.2.10 CN19, Smart Reflex test pin

CN19 is 4-pin header for Smart Reflex signal measuring. The connections are shown in the table below:

Table 3.11: Smart Reflex header pin out

Pin #	Signal Name
1	DSP_VCL_R
2	DSP_VD_R
3	ARM0_VCL_R
4	ARM0_VD_R

3.2.11 CN20, Reserve pin header

CN20 is 4-pin header for Reserve signal. The connections are shown in the table below:

Table 3.12: Reserve signal header pin out

Pin #	Signal Name
1	RSV015
2	RSV017
3	RSV016
4	RSV018

3.2.12 CN21, SIM Power Value select header

CN21 is 3-pin header for program VSIM value. The selection have two output voltage as follows:

- VCC_SIM Value = 2.95V: installed over CN21(1-2)
- VCC_SIM Value = 1.8V (Default): installed over CN21(2-3)

The connections are shown in the table below:

Table 3.13: SIM SEL header pin out

Pin #	Signal Name
1	VCC1V8
2	SIM_SEL
3	GND

3.2.13 CN22, MCU JTAG Connector

CN22 is a 10-pin JTAG connector for ICDI(In Circuit Debug Interface) of MCU emulation. Whenever an external emulator is plugged into CN22. The pin out for the connector is shown in figure below:

Table 3.14: MCU JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	VCC3V3_MP	2	BSC_JTAG_TMS
3	Ground	4	BSC_JTAG_TCK
5	Ground	6	BSC_JTAG_TDO
7	NC	8	BSC_JTAG_TDI
9	Ground	10	BSC_JTAG_SRSTN

3.2.14 CN24, Standby power control for UCD9090 flash

CN24 is 2-pin header for burned into UCD9090 register code at first initialization.The selection have two mode as follows:

- Installed Jumper(Default): For correct Power sequence
- Remove Jumper: For burned into UCD9090 register code

Table 3.15: CN24 Connector pin out

Pin #	Signal Name
1	VCC3V3_AUX_EN_R
2	VCC3V3_AUX_EN

3.2.15 DIMM1, DDR3 SO-DIMM Socket

DIMM1 is 204-pin DDR3 Socket type for external expansion. For compatibility ,you can only use the DDR3 SO-DIMM of ECC type. If you use the general standard type will cause not compatible. ECC and non-ECC different pin definitions , please refer to the specification of the SO-DIMM module.

3.2.16 DC_IN1, DC Power Input Jack Connector

DC_IN1 is a DC Power-in Jack Connector for the stand-alone application of EVM. It is a 2.5mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into MicroTCA chassis or AMC carrier backplane.

3.2.17 EMU1, MIPI 60-Pin SoC JTAG Connector

EMU1 is a high speed system trace capable MIPI 60-pin JTAG connector for XDS200 type of SoC emulation. The on board switch multiplexes this interface with external type emulator through AMC edge. Whenever an external emulator is plugged into EMU1, the external emulator connection will be switched to the SoC. The I/O voltage level on these pins is 1.8V. So any 1.8 V level compatible emulator can be used to interface with the SoC. It should be noted that when an external emulator is plugged into this connector (EMU1), from AMC edge type emulation circuitry will be disconnected from the SoC. The pin out for the

connector is shown in figure below:

Table 3.16: SoC JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	TVD (+1.8V)	2	TMS
3	TCLK	4	TDO
5	TDI	6	TRGRST#
7	TCLKRTN	8	EMU_TRST#
9	nTRST(NC)	10	NC
11	NC	12	TVD
13	EMU2	14	TRC_CLK1(NC)
15	TDIS	16	Ground
17	EMU3	18	EMU21
19	EMU0	20	EMU22
21	EMU1	22	EMU23
23	EMU4	24	EMU24
25	EMU5	26	EMU25
27	EMU6	28	EMU26
29	EMU7	30	EMU27
31	EMU8	32	EMU28
33	EMU9	34	EMU29
35	EMU10	36	EMU30
37	EMU11	38	EMU31
39	EMU12	40	EMU32
41	EMU13	42	EMU33
43	EMU14	44	NC
45	EMU15	46	NC
47	EMU16	48	NC
49	EMU17	50	NC
51	EMU18	52	NC
53	EMU19	54	NC
55	EMU20	56	NC
57	Ground	58	EXT_EMU_DET
59	TRC_CLK(NC)	60	NC

3.2.18 FAN1, FAN Connector

The EVM incorporates a dedicated cooling fan. This fan has the capability of easily being removed when the EVM is inserted into an AMC backplane which uses forced air cooling.

The fan selected provides maximum cooling (CFM) and operates on 12Vdc. FAN1 will be connected to provide 12Vdc to the fan. It should be noted that we will support the adjustment of the fan speed from the UCD9090 FAN Duty cycle control.

Table 3.17 : FAN1 Connector pin out

Pin #	Signal Name
1	GNG
2	+12Vdc
3	NC
4	FAN_PWM

3.2.19 FTDI_USB, Mini-USB Connector

FTDI_USB is a 5-pin Mini-USB connector to connect Code Composer Studio with SoC using UART Console type on-board emulation circuitry. Below table shows the pin outs of the Mini-USB connector.

Table 3.18 : Mini-USB Connector pin out

Pin #	Signal Name
1	VBUS
2	USB D-
3	USB D+
4	GRound
5	Ground

3.2.20 J1, uTCA.4 Edge Connector for Hyperlink SerDes

J1 is an ZD3 Plus connector. The RTM edge connector plugs into an RTM compatible carrier board and provides 2 Hyperlink Group and system interfaces to the carrier board. This connector is the 160 pin style. The signals on this connector are shown in the table below:

Table 3.19 : J1 ZD3 Plus pin out

Pin	Signal	Description	Pin	Signal	Description
GA1	GND	Ground	A3	HyperLink0_TXP0	HyperLink0 transmit data
GA2	GND	Ground	B3	HyperLink0_TXN0	
GA3	GND	Ground	A4	HyperLink0_RXP0	HyperLink0 receive data
GA4	GND	Ground	B4	HyperLink0_RXP0	
GA5	GND	Ground	A5	HyperLink0_TXP1	HyperLink0 transmit data
GA6	GND	Ground	B5	HyperLink0_TXN1	

Pin	Signal	Description	Pin	Signal	Description
GA7	GND	Ground	A6	HyperLink0_RXP1	HyperLink0 receive data
GA8	GND	Ground	B6	HyperLink0_RXP1	
GA9	GND	Ground	A7	HyperLink0_TXP2	HyperLink0 transmit data
GA10	GND	Ground	B7	HyperLink0_TXN2	
GB1	GND	Ground	A8	HyperLink0_RXP2	HyperLink0 receive data
GB2	GND	Ground	B8	HyperLink0_RXP2	
GB3	GND	Ground	A9	HyperLink0_TXP3	HyperLink0 transmit data
GB4	GND	Ground	B9	HyperLink0_TXN3	
GB5	GND	Ground	A10	HyperLink0_RXP3	HyperLink0 receive data
GB6	GND	Ground	B10	HyperLink0_RXP3	
GB7	GND	Ground	E3	HyperLink1_TXP0	HyperLink1transmit data
GB8	GND	Ground	F3	HyperLink1_TXN0	
GB9	GND	Ground	E4	HyperLink1_RXP0	HyperLink1 receive data
GB10	GND	Ground	F4	HyperLink1_RXP0	
GC1	GND	Ground	E5	HyperLink1_TXP1	HyperLink1 transmit data
GC2	GND	Ground	F5	HyperLink1_TXN1	
GC3	GND	Ground	E6	HyperLink1_RXP1	HyperLink1 receive data
GC4	GND	Ground	F6	HyperLink1_RXP1	
GC5	GND	Ground	E7	HyperLink1_TXP2	HyperLink1 transmit data
GC6	GND	Ground	F7	HyperLink1_TXN2	
GC7	GND	Ground	E8	HyperLink1_RXP2	HyperLink1 receive data
GC8	GND	Ground	F8	HyperLink1_RXP2	
GC9	GND	Ground	E9	HyperLink1_TXP3	HyperLink1 transmit data
GC10	GND	Ground	F9	HyperLink1_TXN3	
GD1	GND	Ground	E10	HyperLink1_RXP3	HyperLink1 receive data
GD2	GND	Ground	F10	HyperLink1_RXP3	
GD3	GND	Ground	C3	HyperLink0_RXFLCLK	HyperLink0 sideband signals
GD4	GND	Ground	D3	HyperLink0_RXFLDAT	
GD5	GND	Ground	C4	HyperLink0_TXFLCLK	
GD6	GND	Ground	D4	HyperLink0_TXFLDAT	
GD7	GND	Ground	C5	HyperLink0_RXPMCLK	
GD8	GND	Ground	D5	HyperLink0_RXPMDAT	
GD9	GND	Ground	C6	HyperLink0_TXPMCLK	
GD10	GND	Ground	D6	HyperLink0_TXPMDAT	
GE1	GND	Ground	C7	HyperLink1_RXFLCLK	HyperLink1 sideband signals
GE2	GND	Ground	D7	HyperLink1_RXFLDAT	
GE3	GND	Ground	C8	HyperLink1_TXFLCLK	
GE4	GND	Ground	D8	HyperLink1_TXFLDAT	
GE5	GND	Ground	C9	HyperLink1_RXPMCLK	
GE6	GND	Ground	D9	HyperLink1_RXPMDAT	
GE7	GND	Ground	C10	HyperLink1_TXPMCLK	
GE8	GND	Ground	D10	HyperLink1_TXPMDAT	
GE9	GND	Ground	G3	NC	
GE10	GND	Ground	H3	NC	
GF1	GND	Ground	G4	NC	
GF2	GND	Ground	H4	NC	
GF3	GND	Ground	G5	NC	
GF4	GND	Ground	H5	NC	
GF5	GND	Ground	G6	NC	
GF6	GND	Ground	H6	NC	
GF7	GND	Ground	G7	NC	
GF8	GND	Ground	H7	NC	
GF9	GND	Ground	G8	NC	

Pin	Signal	Description	Pin	Signal	Description
GF10	GND	Ground	H8	NC	
GG1	GND	Ground	A1	VCC12V	RTM PWR (12V)
GG2	GND	Ground	B1	VCC12V	RTM PWR (12V)
GG3	GND	Ground	A2	VCC12V	RTM PWR (12V)
GG4	GND	Ground	B2	VCC12V	RTM PWR (12V)
GG5	GND	Ground	C1	uRTM_PS#	PS#
GG6	GND	Ground	D1	EXP_SDA2_3V3	I2C SDA
GG7	GND	Ground	C2	VCC3V3_MP_AMC	RTM MP (3.3V)
GG8	GND	Ground	D2	EXP_SCL2_3V3	I2C SCL
GG9	GND	Ground	E1	NC	
GG10	GND	Ground	F1	NC	
GH1	GND	Ground	E2	NC	
GH2	GND	Ground	F2	NC	
GH3	GND	Ground	G1	NC	
GH4	GND	Ground	H1	NC	
GH5	GND	Ground	G2	NC	
GH6	GND	Ground	H2	NC	
GH7	GND	Ground	G9	NC	
GH8	GND	Ground	H9	NC	
GH9	GND	Ground	G10	NC	
GH10	GND	Ground	H10	NC	

3.2.21 J2, uTCA.4 Edge Connector for XFI and AIF SerDes

J2 is an ZD3 Plus connector. The RTM edge connector plugs into an RTM compatible carrier board and provides 2 XFI port and 4 AIF lanes to the carrier board. This connector is the 160 pin style. The signals on this connector are shown in the table below:

Table 3.20 : J2 ZD3 Plus pin out

Pin	Signal	Description	Pin	Signal	Description
GA1	GND	Ground	A1	NC	
GA2	GND	Ground	B1	NC	
GA3	GND	Ground	A2	NC	
GA4	GND	Ground	B2	NC	
GA5	GND	Ground	A3	NC	
GA6	GND	Ground	B3	NC	
GA7	GND	Ground	A4	NC	
GA8	GND	Ground	B4	NC	
GA9	GND	Ground	A5	NC	
GA10	GND	Ground	B5	NC	
GB1	GND	Ground	A6	NC	
GB2	GND	Ground	B6	NC	
GB3	GND	Ground	A7	NC	
GB4	GND	Ground	B7	NC	
GB5	GND	Ground	A8	NC	
GB6	GND	Ground	B8	NC	
GB7	GND	Ground	A9	SOC_MDIO_3V3	SGMII MDIO Data
GB8	GND	Ground	B9	SOC_MDC_3V3	SGMII MDIO CLK
GB9	GND	Ground	C1	SOC_XFI_TX_DP0	Ethernet MAC XGMII

Pin	Signal	Description	Pin	Signal	Description
GB10	GND	Ground	D1	SOC_XFI_TX_DN0	port 0 receive data
GC1	GND	Ground	C2	SOC_XFI_RX_DP0	Ethernet MAC XGMII
GC2	GND	Ground	D2	SOC_XFI_RX_DN0	port 0 transmit data
GC3	GND	Ground	C3	SOC_XFI_TX_DP1	Ethernet MAC XGMII
GC4	GND	Ground	D3	SOC_XFI_TX_DN1	port 1 receive data
GC5	GND	Ground	C4	SOC_XFI_RX_DP1	Ethernet MAC XGMII
GC6	GND	Ground	D4	SOC_XFI_RX_DN1	port 1 transmit data
GC7	GND	Ground	C5	NC	
GC8	GND	Ground	D5	NC	
GC9	GND	Ground	C6	NC	
GC10	GND	Ground	D6	NC	
GD1	GND	Ground	C7	NC	
GD2	GND	Ground	D7	NC	
GD3	GND	Ground	C8	NC	
GD4	GND	Ground	D8	NC	
GD5	GND	Ground	C9	SOC_XFI_MDIO_3V3	XGMII MDIO Data
GD6	GND	Ground	D9	SOC_XFIMD_CLK_3V3	XGMII MDIO CLK
GD7	GND	Ground	F2	ZD3_AIF0_TXP	Antenna Interface
GD8	GND	Ground	E2	ZD3_AIF0_TXN	transmit data
GD9	GND	Ground	F1	ZD3_AIF0_RXP	Antenna Interface
GD10	GND	Ground	E1	ZD3_AIF0_RXN	receive data
GE1	GND	Ground	F4	ZD3_AIF1_TXP	Antenna Interface
GE2	GND	Ground	E4	ZD3_AIF1_TXN	transmit data
GE3	GND	Ground	F3	ZD3_AIF1_RXP	Antenna Interface
GE4	GND	Ground	E3	ZD3_AIF1_RXN	receive data
GE5	GND	Ground	F6	ZD3_AIF2_TXP	Antenna Interface
GE6	GND	Ground	E6	ZD3_AIF2_TXN	transmit data
GE7	GND	Ground	F5	ZD3_AIF2_RXP	Antenna Interface
GE8	GND	Ground	E5	ZD3_AIF2_RXN	receive data
GE9	GND	Ground	F8	ZD3_AIF3_TXP	Antenna Interface
GE10	GND	Ground	E8	ZD3_AIF3_TXN	transmit data
GF1	GND	Ground	F7	ZD3_AIF3_RXP	Antenna Interface
GF2	GND	Ground	E7	ZD3_AIF3_RXN	receive data
GF3	GND	Ground	G1	NC	
GF4	GND	Ground	H1	NC	
GF5	GND	Ground	G2	NC	
GF6	GND	Ground	H2	NC	
GF7	GND	Ground	G3	NC	
GF8	GND	Ground	H3	NC	
GF9	GND	Ground	G4	NC	
GF10	GND	Ground	H4	NC	
GG1	GND	Ground	G5	NC	
GG2	GND	Ground	H5	NC	
GG3	GND	Ground	G6	NC	
GG4	GND	Ground	H6	NC	
GG5	GND	Ground	G7	NC	
GG6	GND	Ground	H7	NC	
GG7	GND	Ground	G8	NC	
GG8	GND	Ground	H8	NC	
GG9	GND	Ground	A10	NC	
GG10	GND	Ground	B10	NC	
GH1	GND	Ground	C10	NC	
GH2	GND	Ground	D10	NC	

Pin	Signal	Description	Pin	Signal	Description
GH3	GND	Ground	E9	NC	
GH4	GND	Ground	F9	NC	
GH5	GND	Ground	E10	NC	
GH6	GND	Ground	F10	NC	
GH7	GND	Ground	G9	NC	
GH8	GND	Ground	H9	NC	
GH9	GND	Ground	G10	NC	
GH10	GND	Ground	H10	NC	

3.2.22 MCU and SoC, UART4 Pin Connector

MCU and SoC is 4-pin male connector for RS232 serial interface. A 4-Pin female to 9-Pin DTE female cable is supplied with EVM to connect with the PC.

Table 3.21: UART Connector pin out

Pin #	Signal Name
1	Receive
2	Transmit
3	Ground
4	Detect

3.2.23 PMBUS1, PMBUS Connector for Smart-Reflex and sequence Control

The SoC core power is supplied by Sequence control UCD9090 and Smart-Reflex power controller UCD9244 with the Integrated FET Driver UCD7242, 74120,UCD74111 and UCD74106. PMBUS1 provides a connection between UCD9244 and remote connection during development. Through the USB to GPIO pod provided by TI, the user can trace and configure the parameters in UCD9244 with the Smart-Fusion GUI. The pin out of PMBUS1 is shown in table 3.22.

Table 3.22 : PMBUS1 pin out

Pin #	Signal Name
1	PMBUS_CLK
2	PMBUS_DAT
3	PMBUS_ALT
4	PMBUS_CTL
5	GND

3.2.24 SoC_USB, USB3.0 TypeA Connector

SoC_USB is an 9-pin USB3 typeA connector for the USB interface The pin out for the connector is shown in the figure below:

Table 3.23 : USB3 Connector pin out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+

3.2.25 SIM1, USIM connector

SIM1 is a 8-pin SIM Card connector for Universal Subscriber Identity Module(USIM) interface . The USIM is compatible with ISO, ETSI/GSM, and 3GPP standards. The pin out for the connector is shown in the figure below:

Table 3.24 : USIM Connector pin out

Pin #	Signal Name
C1	SIM VCC
C2	SIM RST
C3	SIM CLK
C5	GND
C6	NC
C7	SIM IO
SW1	VCC1V8
SW2	SIM Enable

3.3 DIP and Pushbutton Switches

The EVM has 3 push button switches , one Jumper header and one sliding actuator DIP switches. The PRW, ATT and MCU_RESET are push button switches , CN8 is Jumper header while SW1 are DIP switches. The function of each of the switches is listed in the table below:

Table 3.25 : EVM Board Switches

Switch	Function

PWR	Full Reset Event
MCU_RESET	MCU Reset Event
ATT	Warm Reset Event
CN8	MCU Wake Evant
SW1	SoC Boot mode Configuration

3.3.1 PWR, Full Reset

Pressing the PWR button performs different functions based on how many times the button was pressed. The button must be pressed again within 0.5 seconds for it to register as a sequential click:

1 press: Graceful Shutdown

2 presses: Warm Reset

3 presses: Full Reset

4 presses: Cancel action

If the button is pressed and held for longer than 3 seconds, the board will be forcefully shutdown.

3.3.2 MCU_RESET, MCU Reset

Pressing the MCU_RESET button switch will issue a RST# to the MCU. It'll reset MCU and other peripherals.

3.3.3 ATT, Warm Reset

Not currently implemented.

3.3.4 CN8, Wake

The button is reserved for future use.

3.3.5 SW1, SoC Boot mode Configurations

SW1 are 4-position DIP switches, which are used for Boot Device, Boot Configuration.

For the details about the SoC Boot modes and their configuration, please refer to the SoC Data Manual.

The diagram of the DSP no-boot setting on these switches is shown below:

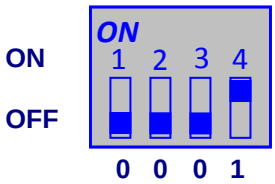


Figure 3.4: SW1 DSP no-boot settings

The following table describes the positions and corresponding functions on SW1.

Table 3.26: SW1, Boot mode Configurations Switch

DIP Switch (p1, p2, p3, p4)	Bootmode
0000	Reserved
0001	No Boot/JTAG DSP Little Endian Boot mode
0010	Uboot mode/NOR SPI Boot
0011	Reserved
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved
1000	User Programmable
1001	User Programmable
1010	User Programmable
1011	User Programmable
1100	User Programmable
1101	User Programmable
1110	User Programmable
1111	User Programmable

For more information and options on boot modes please visit:
http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup

3.4 Test Points

The EVM Board has 63 test points. The position of each test point is shown in the figures below:

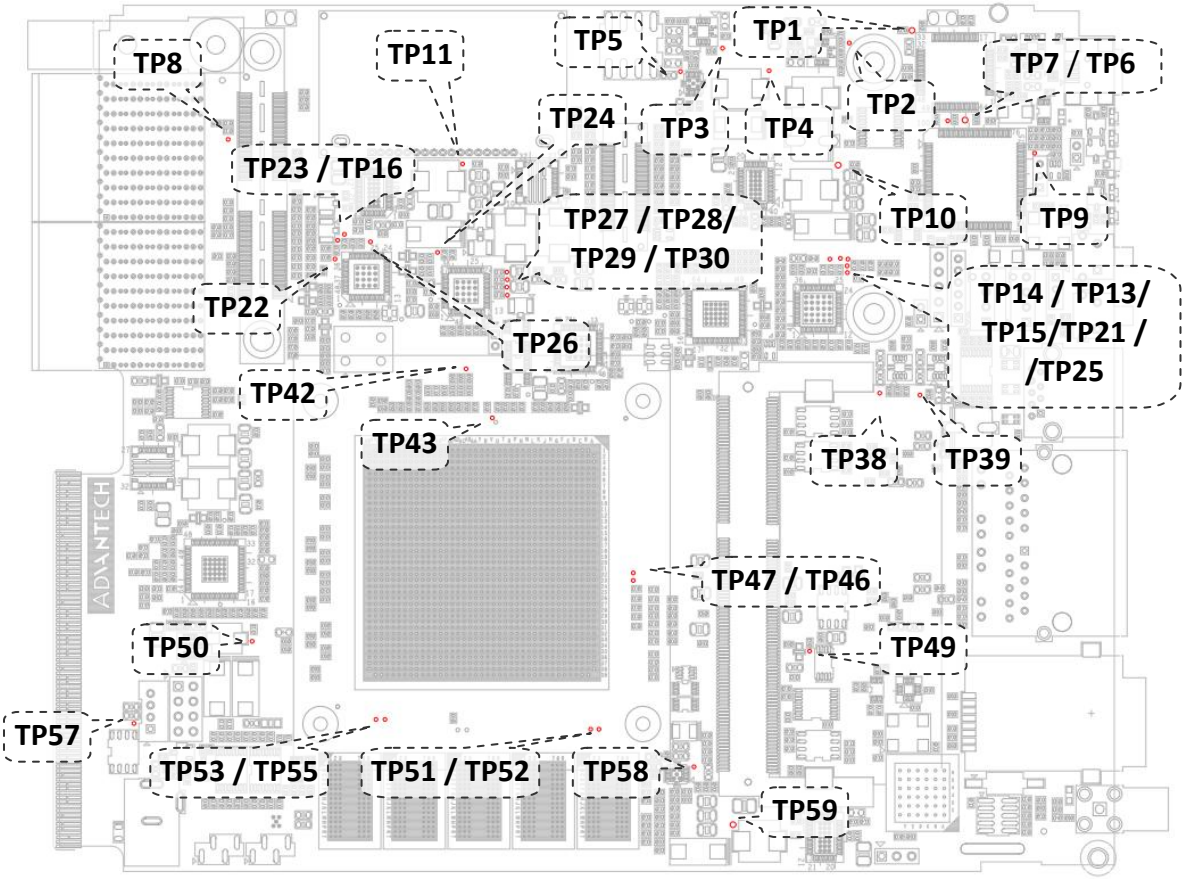


Figure 3.5 : EVM test points on top side

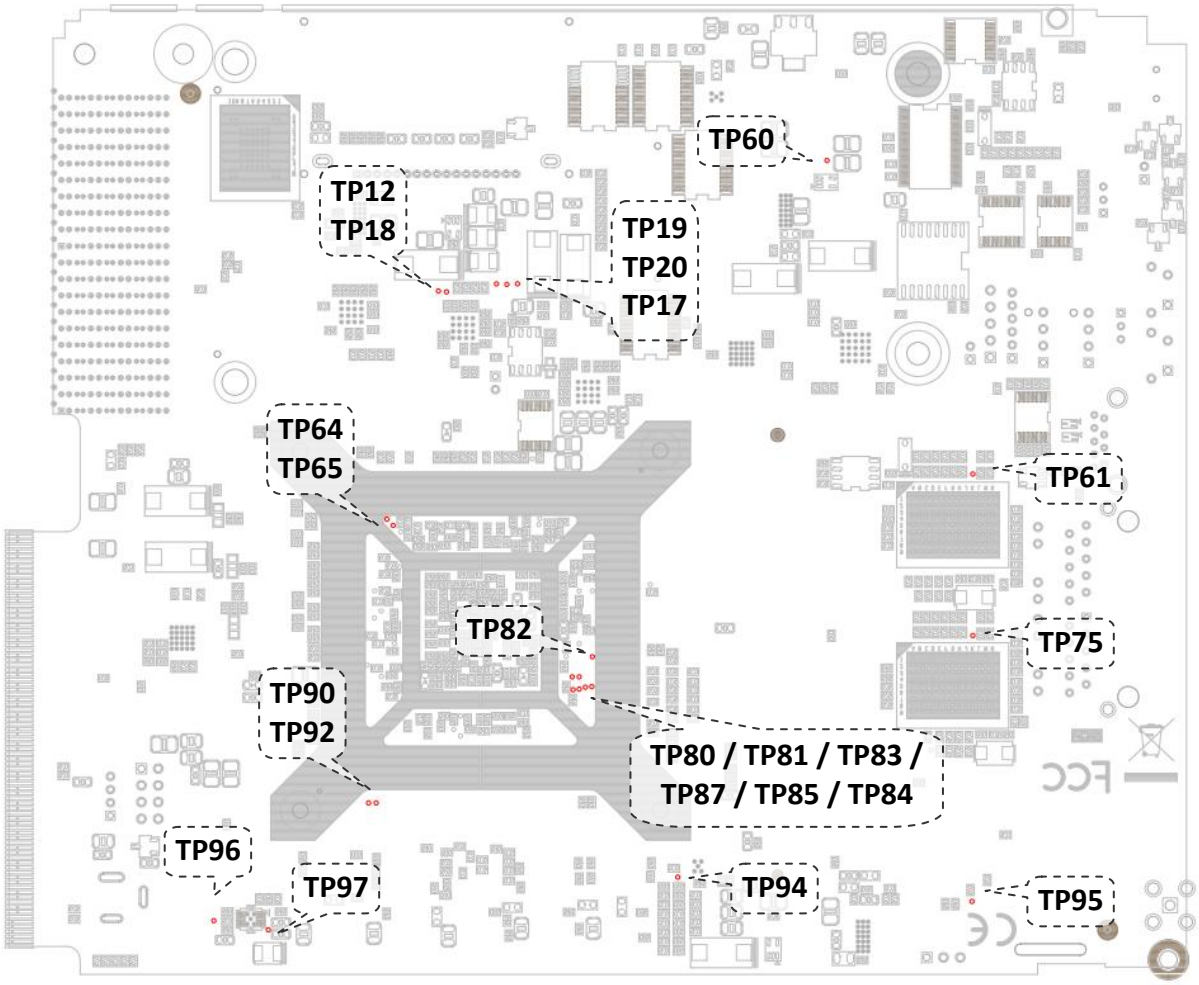


Figure 3.6 : EVM test points on the bottom side

Table 3.27 : EVM Board Test Points

Test Point	Signal
TP1	Test point for SoC SUSPEND#
TP2	Test point for VCC3_AUX_PGOOD
TP3	Test point for VCC5_PGOOD
TP4	Test point for VCC5
TP5	Test point for VPP1V8
TP6	Test point for SoC PWREN#
TP7	Reserved for U7 pin95 (MCU_SPI1_MISO)
TP8	Reserved for expansion header pin96 (EXP_TP0)
TP9	Reserved for U7 pin67 (MCU_U1TX)
TP10	Test point for VCC1V5
TP11	Test point for CVDD
TP12	Test point, TI CDCE6208, CLK2 output Y7p
TP13	Reserved for UCD9090 JTAG pin 30 (JTAG_TMS).
TP14	Reserved for UCD9090 JTAG pin 31 (TRST#).
TP15	Reserved for UCD9090 JTAG pin 29 (JTAG_TDI).
TP16	Test point, TI CDCE6208, CLK1 output Y6n

TP17	Test point, TI CDCE6208, CLK2 output Y5n
TP18	Test point, TI CDCE6208, CLK2 output Y6n
TP19	Test point, TI CDCE6208, CLK2 output Y6p
TP20	Test point, TI CDCE6208, CLK2 output Y5p
TP21	Reserved for UCD9090 JTAG pin 28 (JTAG_TDO).
TP22	Test point, TI CDCE6208, CLK1 output Y7n
TP23	Test point, TI CDCE6208, CLK1 output Y7p
TP24	Test point, TI CDCE6208, CLK2 output Y7n
TP25	Reserved for UCD9090 JTAG pin 27 (JTAG_TCK).
TP26	Test point, TI CDCE6208, CLK1 output Y6p
TP27	Test point, TI CDCE6208, CLK2 output Y3p
TP28	Test point, TI CDCE6208, CLK2 output Y3n
TP29	Test point, TI CDCE6208, CLK2 output Y2n
TP30	Test point, TI CDCE6208, CLK2 output Y2p
TP38	Test point for VCC1V2
TP39	Test point for VCC2V5
TP42	Test point for SoC SYSCLKOUT
TP43	Test point for SoC USBID0
TP46	Reserved
TP47	Reserved
TP49	Test point for DAC_VOUT
TP50	Test point for VCC1V8
TP51	Reserved
TP52	Reserved
TP53	Reserved
TP55	Reserved
TP57	Test point for VCC12
TP58	Test point for VCCA0V75
TP59	Test point for CVDDT
TP60	Test point for VCC3V3_AUX
TP61	PHY2 (88E1111) 125MHz clock (default: disable)
TP64	Reserved
TP65	Reserved
TP75	PHY1 (88E1111) 125MHz clock (default: disable)
TP80	Reserved for SoC SPI0SCS1
TP81	Reserved for SoC SPI0SCS3
TP82	Reserved for SoC SPI0SCS2
TP83	Reserved for SoC SPI1DIN
TP84	Reserved for SoC SPI1SCS1
TP85	Reserved for SoC SPI1SCS2
TP87	Reserved for SoC SPI1SCS3
TP90	Reserved
TP92	Reserved
TP94	Test point for VCCA0V75_PGOOD
TP95	Reserved for GPS1 pin C2 (TCXO_CLK)
TP96	Test point for VCC0V75_PGOOD
TP97	Test point for VCCB0V75

3.5 System LEDs

The EVM board has seven LEDs. Their positions on the board are indicated in figure 3.5. The description of each LED is listed in table below:

Table 3.28: EVM Board LEDs

LED#	Color	Description
D3	Red	Failure and Out of service status in AMC chassis
D4	Green	PLLLOCK LED
D5	Blue	Hot Swap status in AMC chassis
D6	Red	SoC RESETSTATZ
Dbg_D1	Red Green	SoC Debug LEDs.
Dbg_D2- DBG_D3	Blue	SoC Debug LEDs.

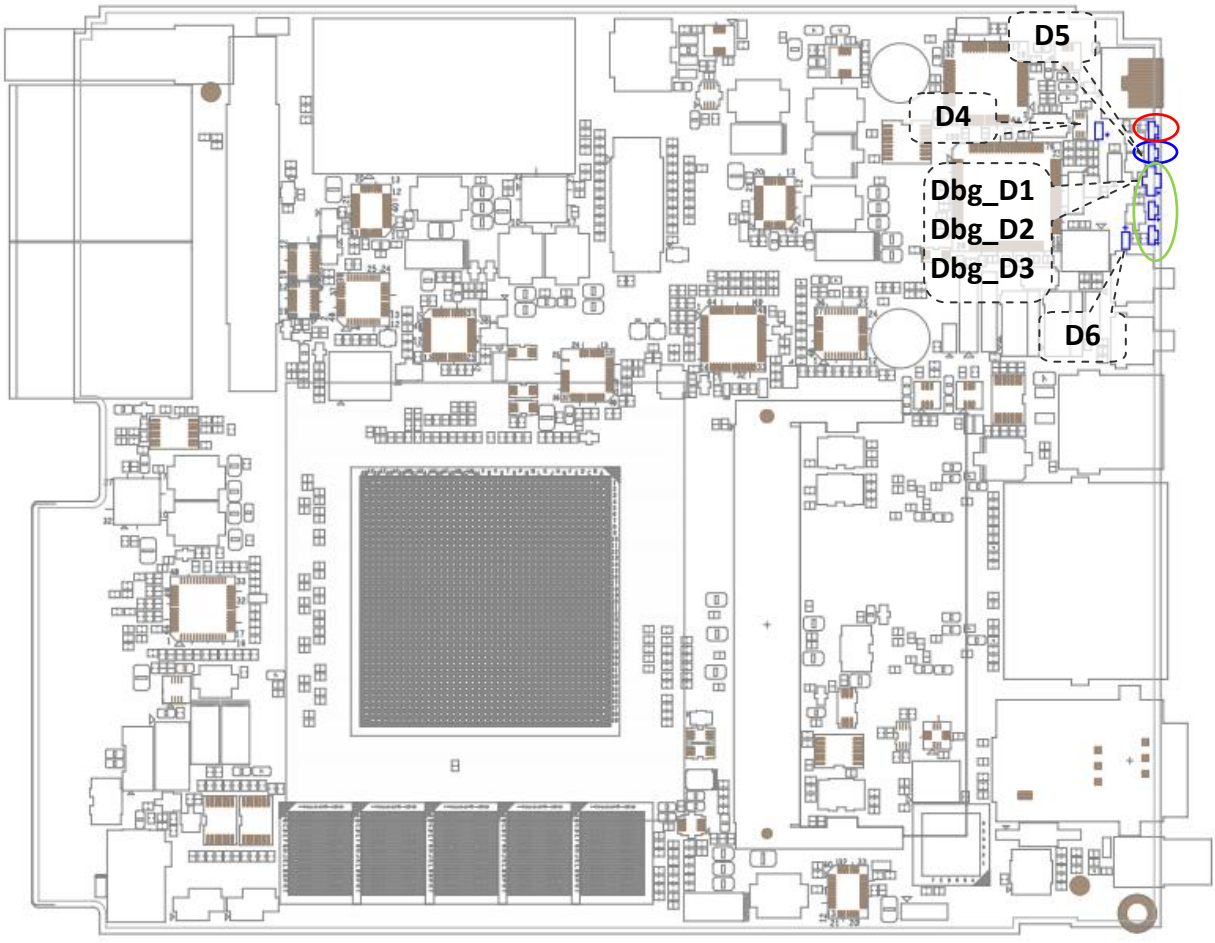


Figure 3.7 : EVM Board LEDs

4. System Power Requirements

This chapter describes the power design of the EVM board. It contains:

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units.

The maximum EVM power requirements are estimated to be:

- EVM MCU – 0.45W;
- SoC Cooling Fans – 1.2W (+12Vdc/0.1A);
- Clock Generators & clock sources – 3.13W;
- SoC – 52.09W;[worse case]
  - Core supplies: 35.5W;
  - Peripheral supplies: 16.59W;
- DDR3 – 10.5W;
  - 5 SDRAMs to support 72-bit with ECC of the SoC
  - 1 SO-DIMM to support 72-bit with ECC of the SoC
- Misc – 0.33W;
- USB3.0 – 4.5W;
- SGMII PHY – 2.15W;
- LCD Display – 0.135W;
- USB Emulator – 0.84W;

EVM board total: 75.28W;

The selected AC/DC 12V adapter should be rated for a minimum of 84 Watts.

The power planes in EVM are identified in the following table:

Table 4.1: EVM Voltage Table

Device	Net name	Voltage	Description
Input	VCC3V3_MP_AMC	+3.3V	Management Power for MMC
	VCC12	+12V	Payload Power to AMC
	VCC5_VBUS	+5V	USB Emulation Power (FT2232H)
Management	VCC3V3_AUX	+3.3V	3.3V Power Rail for all support devices on EVM
	VCC1V2	+1.2V	1.2V Power Rail for all support devices on EVM
SoC	CVDD	+0.75V~1.0V	DSP and ARM Array Variable Smart-Reflex
	CVDD1	+0.95V	DSP Array SRAM
	CVDDT1	+0.95V	ARM Array SRAM
	VCC1V8	+1.8V	SoC I/O and SERDES power
	VCC1V5	+1.5V	SoC DDR3 Power
	VCC0V85	+0.85V	SERDES and USB Analog power
	VDD33	+3.3V	USB Digital and Analog power
	VPP1V8	+1.8V	(Reserve)
DDR3 Memory	VCC1V5	+1.5V	DDR3 RAM and DIMM Power
	VCCA0V75	+0.75V	DDR3A DIMM Termination Power
	VCCB0V75	+0.75V	DDR3B RAM Termination Power
NAND Flash	VCC1V8	+1.8V	NAND Flash Power
NOR Flash (SPI)	VCC1V8	+1.8V	SPI NOR Flash Power
CDCM6208	VCC3V3_AUX	+3.3V	Clock Gen Power
PHY (88E111)	VCC2V5	+2.5V	PHY Analog and I/O Power
	VCC1V2	+1.2V	PHY Core Power (instead of 1.0V)
USB Emulator	VCC3V3_U	+3.3V	USB Emulation Power (FT2232H)
	VCC18_U	+1.8V	USB Emulation Power (FT2232H)
MMC (MCU)	VCC3V3_MP	+3.3V	MMC Power
	VCC3V3_MP_ALT	+3.3V	MCU Power
Misc. Logic	VCC3V3_AUX	+3.3V	Translator and Logic Power
	VCC1V8_AUX	+1.8V	Translator and Logic Power
UCD9090	VCC3V3_MP	+3.3V	Power Sequence Controller Power
USB3.0	VCC5	+5V	USB3.0 power
LCD	VCC3_LCD	+3V	LCD Power

The following table identifies the expected power requirements for each power plane of the devices on the EVM.

Table 4.2: Each Current Requirements on each device of EVM board

Keystone 2	V(V)	I(A)	Qty	Pd (W)	
CVDD	1.00	26.00	1	26.00	52.09
CVDD1	0.95	5.00	1	4.75	
CVDDT1	0.95	5.00	1	4.75	
VCC1V8	1.80	2.3	1	4.14	
VDD33	3.3	2	1	6.6	
VCC1V5	1.50	2.2	1	3.3	
VCC0V85	0.85	3	1	2.55	
DDR3A	V(V)	I(A)	Qty	Pd(W)	
VCC1V5	1.50	3	1	4.5	5.25
VCC0V75	0.75	1	1	0.75	
DDR3B	V(V)	I(A)	Qty	Pd(W)	
VCC1V5	1.50	0.60	5	4.5	5.25
VCC0V75	0.75	0.20	5	0.75	
USB3.0	V(V)	I(A)	Qty	Pd(W)	
VCC5	5.00	0.9	1	4.5	4.5
CDCM6208	V(V)	I(A)	Qty	Pd(W)	
VCC3V3_AUX	3.30	0.316	3	3.128	3.128
PHY (88E1111)	V(V)	I(A)	Qty	Pd(W)	
VCC2V5_AUX	3.30	0.19	2	1.254	2.154
VCC1V2_AUX	1.80	0.25	2	0.9	
FT2232	V(V)	I(A)	Qty	Pd(W)	
VCC3V3_AUX	3.30	0.21	1	0.69	0.84
VCC1V8_AUX	1.80	0.08	1	0.14	
LCD	V(V)	I(A)	Qty	Pd(W)	
VCC3_LCD	3.0	0.045	1	0.135	0.135
MCU	V(V)	I(A)	Qty	Pd(W)	
VCC3V3_MP	3.30	0.135	1	0.4455	0.4455

4.2 The Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1. It is also shown on the schematic.

In Figure 4.1, the Auxiliary power rails are always on after payload power is supplied. These

regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX
- VCC3V3_MP_ALT

The maximum allowable power is 84W from the external AC brick supply or from the 8 AMC header pins and 4 uTCA.4 connector pins.

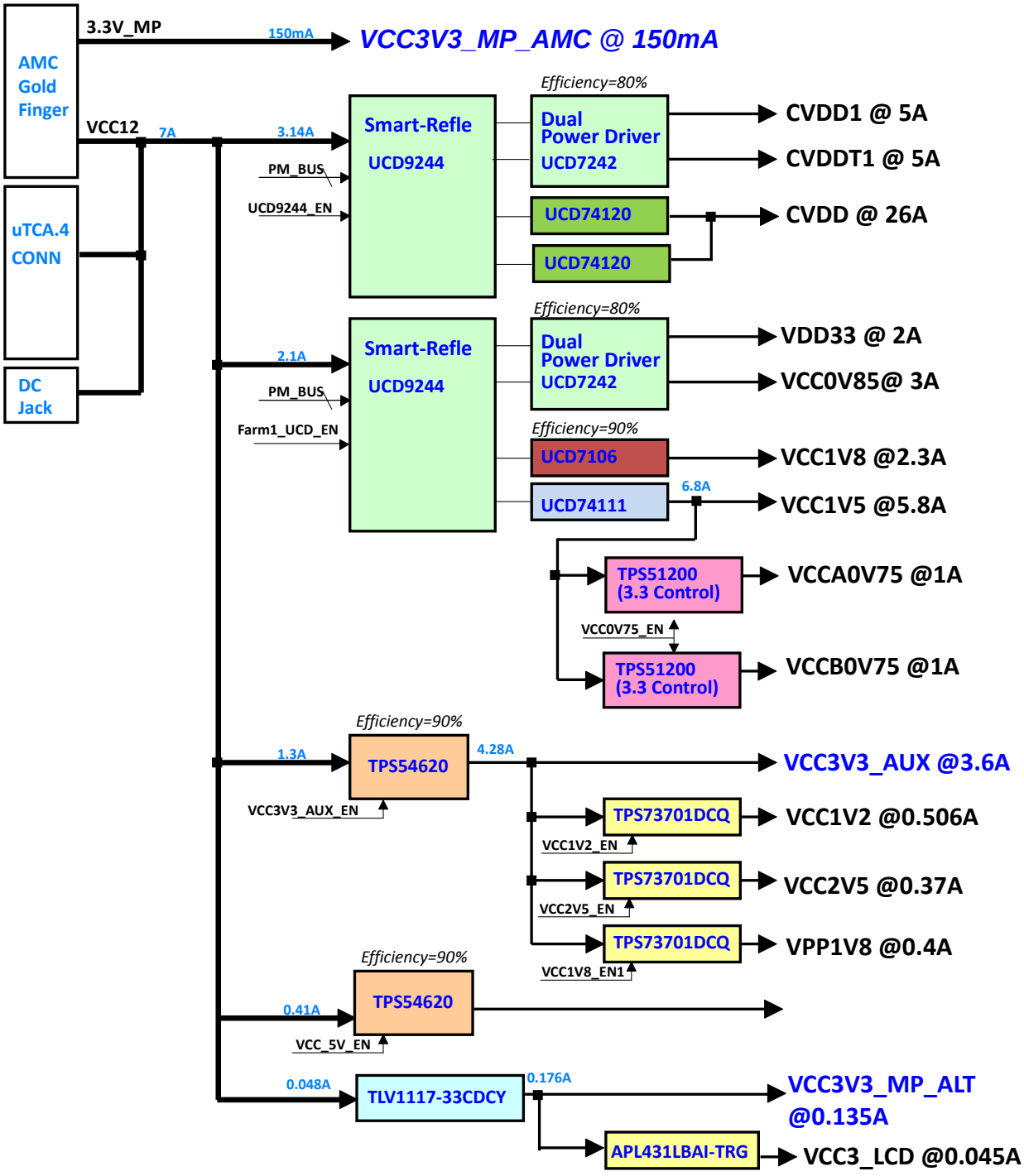


Figure 4.1: All the AMC power supply on EVM

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (Refer to section 4.3 for specific details). The goal of all power supply designs is to support the ambient temperature range of 0°C to 45°C.

The Keystone 2 core power is supplied using a dual digital controller coupled to a high performance FET driver IC. Additional SoC supply voltages are provided by discrete TI Swift power supplies. The Keystone 2 supports two VID interface to enable Smart-Reflex® power supply control for its primary core (DSP and ARM) logic supply. Refer to the Keystone 2 Data Manual and other documentation for an explanation of the Smart-Reflex® control.

Figure 4.1 shows that the EVM power supplies are a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching supplies are implemented for larger loads. The switching supplies are listed below followed by explanations of critical component selection:

- CVDD (AVS core power for Keystone 2)
- CVDD1 and CVDDT1 (0.95V fixed core power for Keystone 2)
- VCC1V8(1.8V power for Keystone 2)
- VDD3V3(3.3V power for Keystone 2)
- VCC0V85(0.85V power for Keystone 2)
- VCC1V5 (1.5V DDR3 power for Keystone 2 and DDR3 memories)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC5 (5.0V power for the USB3.0 connector)

The **CVDD**、**CVDD1** and **CVDDT1** power rails are regulated by TI Smart-Reflex controller UCD9244 and two synchronous-buck power driver UCD74120 to supply SoC AVS core and the dual synchronous-buck power driver UCD7242 to supply SoC CVDD1 and CVDDT1 core power.

The **VCC1V8**、**VDD3V3**、**VCC0V85 and VCC1V5** power rails are regulated by TI Smart-Reflex controller UCD9244 and synchronous-buck power driver UCD74106 to supply SoC SERDES and the synchronous-buck power driver UCD74111 to supply the DSP DDR3 EMIF and DDR3 memory chips respectively and the dual synchronous-buck power driver UCD7242 to supply SoC USB/SERDES power.

The **VCC3V3_AUX** power rails are regulated by TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources .

The **VCC5** power rail is regulated by TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the power of the USB3.0 connector on EVM.

The high level diagrams and output components are shown in figure 4.2, figure 4.3, figure 4.4, and figure 4.5 as well as choosing the proper inductors and buck capacitors.

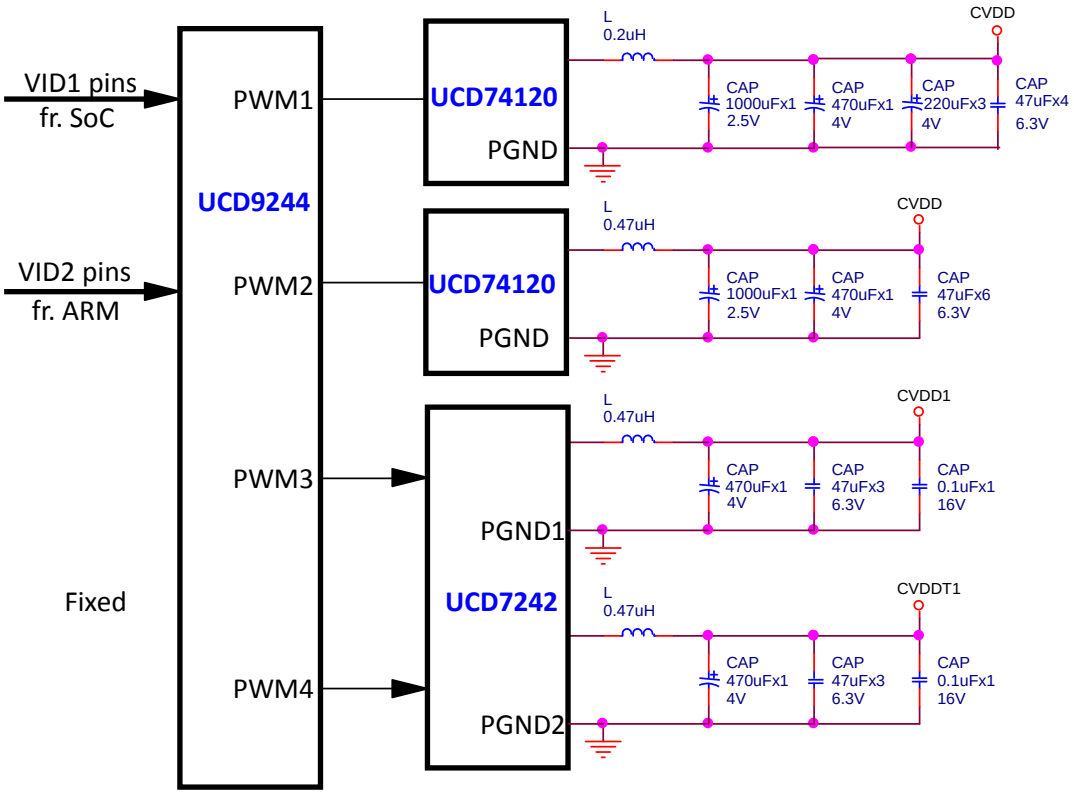


Figure 4.2: The CVDD and CVDD1 and CVDDT1 power design on EVM

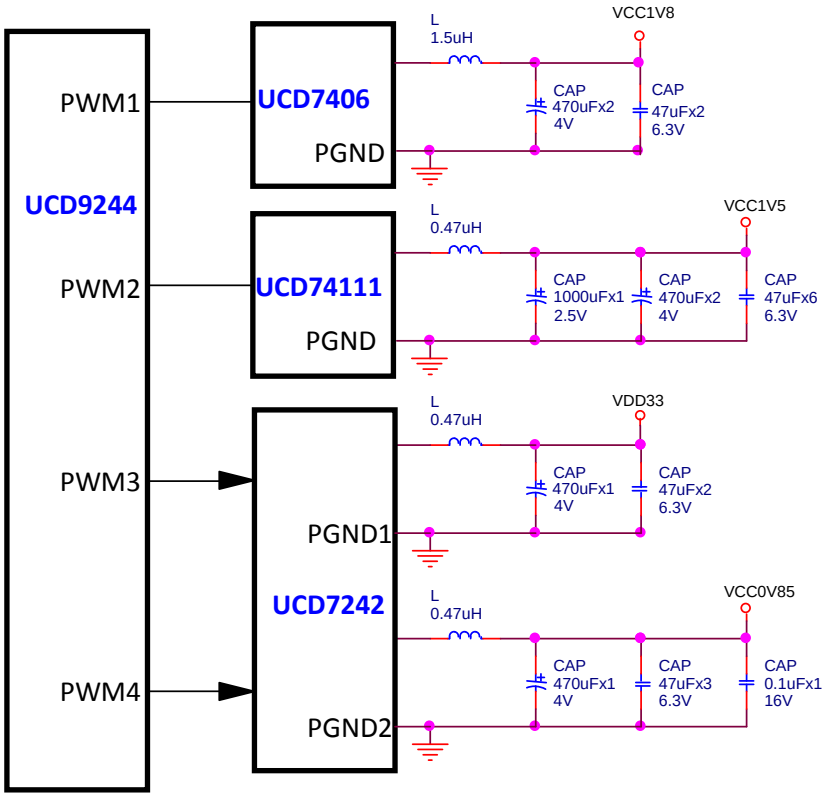
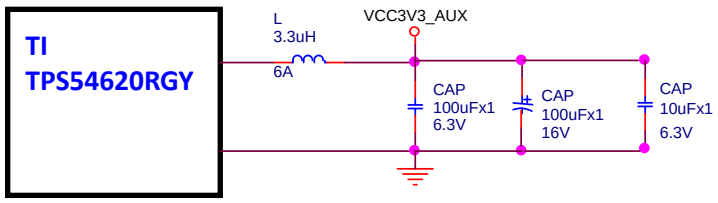


Figure 4.3: The VCC1V8 and VCC1V5 and VDD33 and VCC0V85 power design on EVM

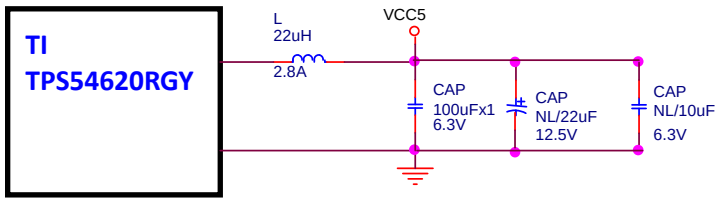


(Over all tolerance is 5% ,DC tolerance is 2.5%)

Output capacitor Calculation (KIND=0.3)
Cout>(2*delta(Iout))/(Fsw*delta(Vout))
Cout>(2*3)/(840kHz*0.0825)
Cout>(6)/(69300)
Cout>87uF
Reference Capacitor=100uF

Inductor Calculation
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12 - 3.3)/3 * Kind) * (3.3 / (12 * 840kHz))
L = ((8.7/3 * 0.3) * (3.3 / (10.08M))
L = (9.67) * (0.33u)
L = ~3.2uH
Reference Inductor 3.3uH

Figure 4.4: The VCC3_AUX power design on EVM



(Over all tolerance is 5% ,DC tolerance is 2.5%)

Output capacitor Calculation
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2)/(570kHz*0.125)
Cout=(4)/(71250)
Cout=56.14uF
Reference Capacitor=100uF

Inductor Calculation (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12 - 5)/2.3 * Kind) * (5/ (12*570kHz))
L = ((7/2.3 * 0.3) * (5 / (6.84M))
L = (7/0.69) * (0.73M)
L = 7.4uH
Reference Inductor 22uH

Figure 4.5: The VCC5 power design on EVM

4.3 The Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The Keystone 2 SoC requires specific power up and power down sequencing. Figure 4.2 and Figure 4.3 illustrate the proper boot up and down sequence. Table 4.3 provides specific timing details for Figure 4.6 and Figure 4.7.

Refer to the Keystone 2 SoC Data Manual for confirmation of specific sequencing and timing requirements.

Table 4.3: The power-up and down timing on the Keystone 2

Step	Power rails	Timing	Descriptions
	Power-Up		
1	VCC12 (AMC Payload power), VCC3V3_MP_ALT, VCC3_LCD	Auto	When the 12V power is supplied to the EVM, the 3.3V supplies to the MCU and UCD9090 power will turn on, the 3V supplies to the LCD power will turn on. MCU outputs to the SoC will be locked (held at ground)..
2	VCC3V3_AUX	0ms	Turn on VCC3V3_AUX from MCU Main power start.
3	VCC1V2,	5mS	Turn on VCC1V2 after VCC3V3_AUX stable for 5mS.
4	VCC2V5	5mS	Turn on VCC2V5 after VCC1V2 stable for 5mS.
5	CVDD (SoC AVS core power)	15mS	Enable the CVDD and CVDD1 and CVDDT1, the UCD9244 power rail#1 & 2 is for CVDD and go first after VCC2V5 are stable for 15mS.
6	CVDD1 (DSP fixed core power) CVDDT1 (ARM fixed core power)	5mS	Turn on CVDD1 and CVDDT1, the UCD9244 power rail#3 & 4. The CVDD1 and CVDDT1 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9244 configuration file.
7	VCC0V85	5mS	Turn on VCC0V85, the UCD9244 power rail#4 . The VCC0V85 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9244 configuration file.
8	VDD33	5mS	Turn on VDD33, the UCD9244 power rail#3 . The VDD33 will start the regulating power rail after enable it after 5mS, the

			start-delay time is set by the UCD9244 configuration file.
9	VCC1V8 (SoC IO power)	5mS	Turn on VCC1V8, the UCD9244 power rail#1 . The VCC1V8 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9244 configuration file.
10	VCC1V5 (SoC DDR3 power)	5mS	Turn on VCC1V5, the UCD9244 power rail#2 . The VCC1V5 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9244 configuration file.
11	VCCA0V75, VCCB0V75,	5mS	Turn on VCCA0V75 and VCCB0V75 after VCC1V5 stable for 5mS.
12	VCC5	5mS	Turn on VCC5 after VCCA0V75 and VCCB0V75 stable for 5mS.
13	CDCM6208#1/#2/#3 initiations MCU outputs	5mS	Unlock the 5V outputs and initiate the CDCE6208s after VCC5 stable for 5mS. De-asserted CDCM6208 power down pins (PD#), initial the CDCM6208s.
14	RESETz Other reset and NMI pins	18mS	De-asserted RESETz and unlock other reset and NMI pins for the SoC after SOC_Power_GOOD stable and CDCE6208s PLLs locked for 5mS. In the meanwhile, the MCU will driving the boot configurations to the SoC GPIO pins.
15	PORz	5mS	De-asserted PORz after RESETz de-asserted for 5mS.
16	RESETFULLz	5mS	De-asserted RESETFULLz after PORz de-asserted for 5mS.
17	SoC GPIO pins for boot configurations	1mS	Release the SoC GPIO pins after RESETFULLz de-asserted for 1mS

	Power-Down		
18	RESETFULLz PORz	0mS	If there is any power failure events or the AMC payload power off, the MCU will assert the RESETFULLz and PORz signals to the SoC.
19	MCU 3.3V outputs CDCM6208 PD# pins	5mS	Locked 3.3V output pins on the MCU and pull the CDCM6208 PD# pins to low to disable SoC clocks.
20	VCC3V3_AUX VCC1V2 VCC2V5 CVDD CVDD1 CVDDT1 VCC0V85 VDD33 VCC1V8 VCC1V5 VCCA0V75 VCCB0V75 VCC5	0mS	Turn off all main power rails.

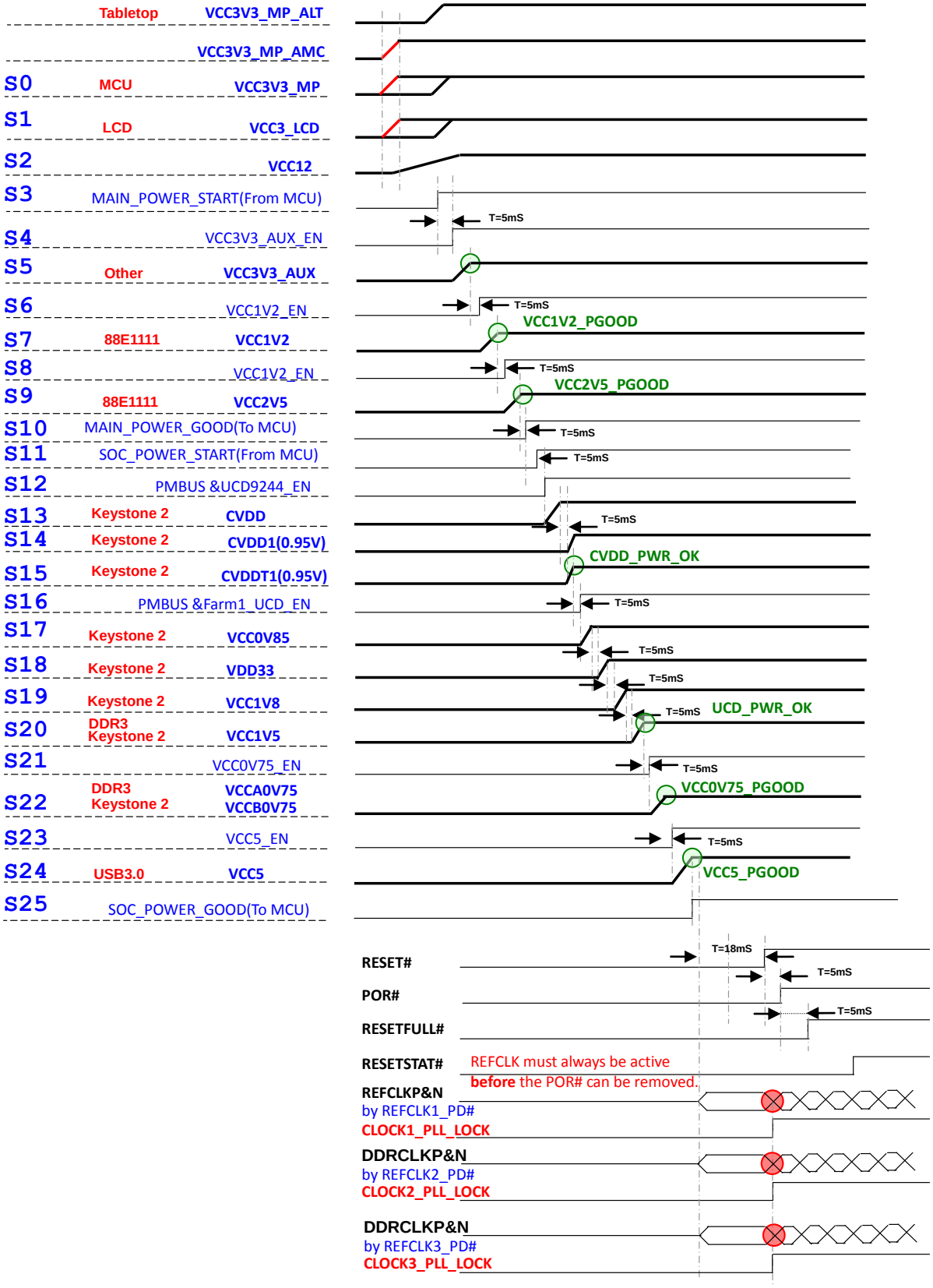


Figure 4.6: Initial Power Up Sequence Timing Diagram

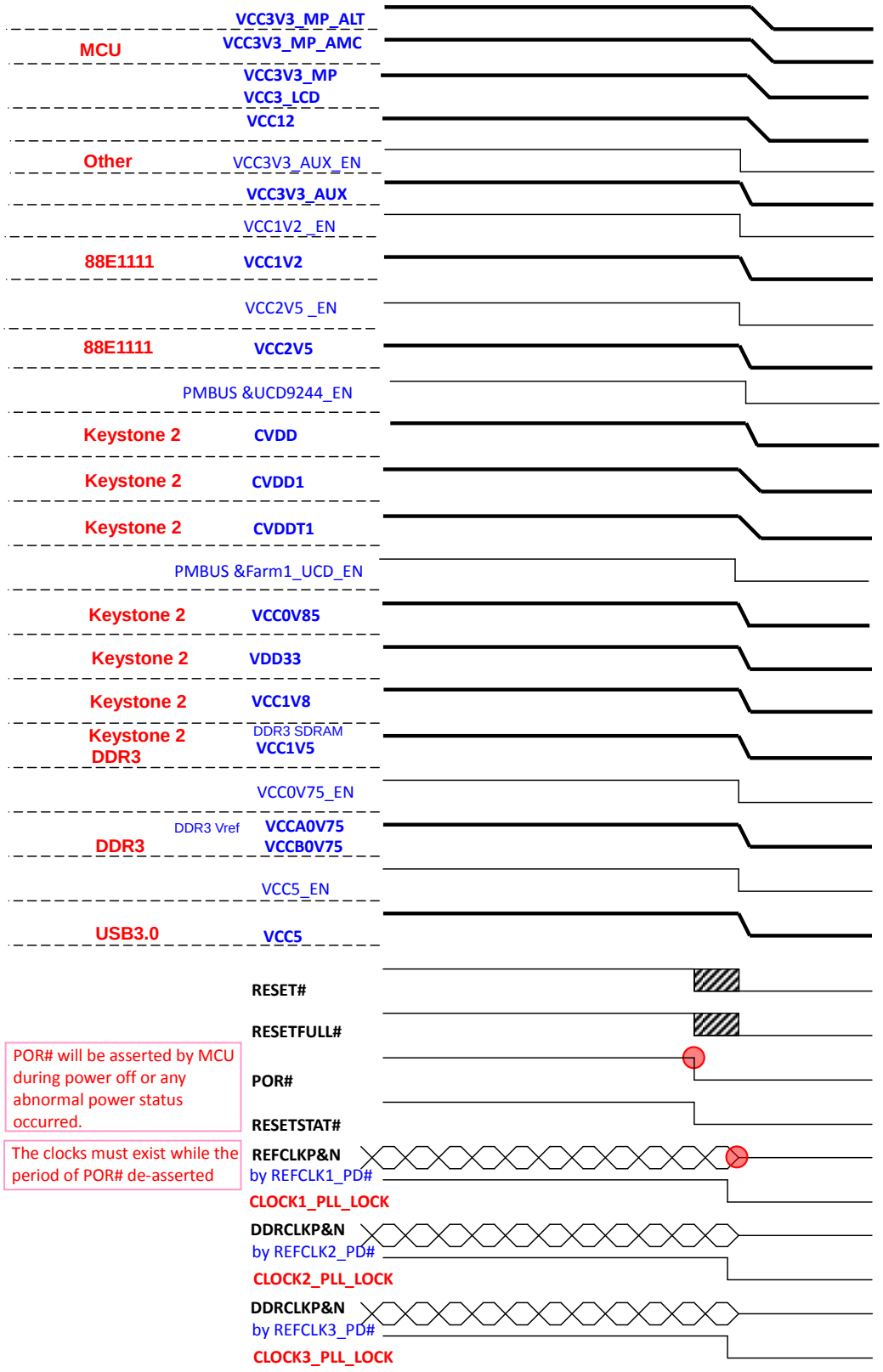


Figure 4.7: Initial Power Down Sequence Timing Diagram

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