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Enabling an Intelligent Planet

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1. TMDXEVM6670 EVM Version List

Multiple versions of the TMDXEVM6670 EVM are now in use. The following sections list the software, firmware and revisions for each production release. The first units shipped were defined as the Beta1 prototypes. The second batch of units shipped was referred to as Beta2 prototypes and these were formally known as Revision 1.0 units. The first large-volume production batch is defined as Revision 2.0 units. Additional enhancements are being incorporated in the design and these will be released as Revision 3.0 units.

1.1 Software Revisions

The Software versions on Beta1 and Beta2 EVMs are shown as the table below.

Item	Beta1	Beta2 / Production board, Rev 2.0
IBL (EEPROM, 0x51h)	2.0.0.03-ENG5	2.0.0.07-ENG2
POST (EEPROM, 0x50h)	1.0.0.02	1.0.0.02
NOR flash (SPI)	N/A	2.0.0.02 Beta2
NAND flash (thru. GPIOs)	N/A	2.0 - Alpha2

For Beta1 and Beta2, the CCS version on the DVD is 5.0.2. The MCSDK version on the DVD is 2.0.0.4.
For Rev 2.0 production EVM, the CCS version on the DVD is 5.0.3. The MCSDK version on the DVD is 2.0.0 beta2

1.2 Firmware Revisions

The Firmware versions on Beta1 and Beta2 EVMs are shown as the table below.

Item	Beta1	Beta2
UCD9222 (Firmware)	6.4.0.12747	6.4.0.12747
UCD9222 (Configuration file)	UCD9222 Nyquist EVM Project 01Apr11 ver4.xml	UCD9222 Nyquist EVM Project 16May11 ver6.xml
FPGA code	nyevm_fpga_v0005.bit	nyevm_fpga_v0005.bit
MMC	mmc430_20110301	mmc430_20110301
XDS100v1	XDS100_wUART_ft2232h.ept	XDS100_wUART_ft2232h.ept

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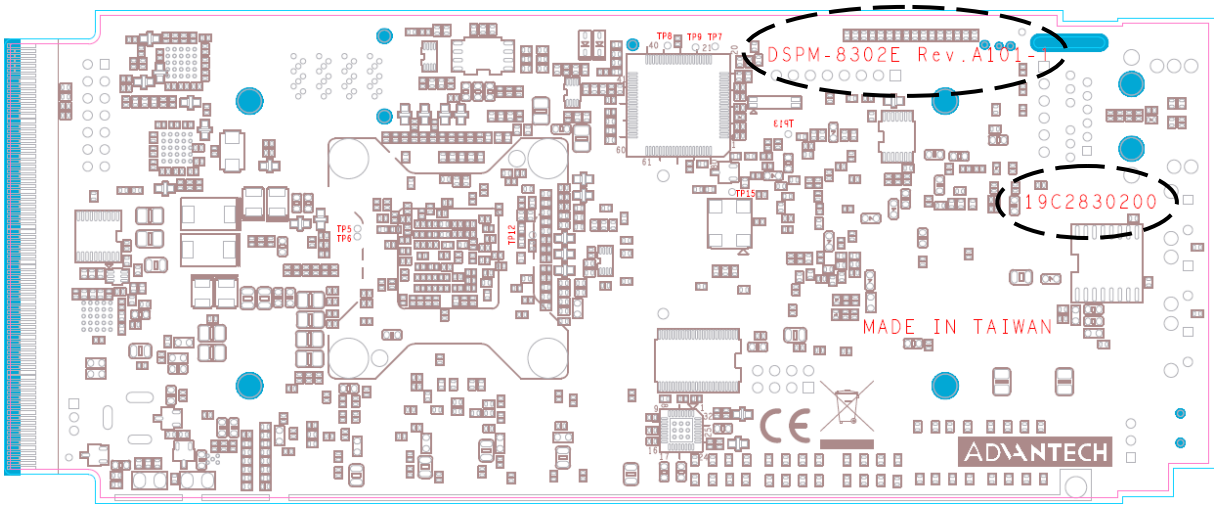
The Firmware versions on production EVM prototypes are shown as the table below.

Item	Production board, Rev 2.0
UCD9222 (Firmware)	6.4.0.12747
UCD9222 (Configuration file)	UCD9222_Project_02_1June_ver7.xml
FPGA code	nyevm_fpga_v0006.bit
MMC	mmc430_20110301
XDS100v1	XDS100_wUART_ft2232h.ept

Please note that the UCD9222 configuration file (.xml) on production board Rev. 2.0 EVM cannot be applied on Beta1 and Beta2 EVMs because of the different design of core power supplies.

1.3 Printed Circuit Board Revisions

The PCB number and version on Beta1 and Beta2 shipments of the TMDXEVM6670 EVM are 19C2830200 and A101-1.



The PCB number and version on Rev 2.0 production EVM shipment of the TMDXEVM6670 EVM are 19C2830201 and A102-1.

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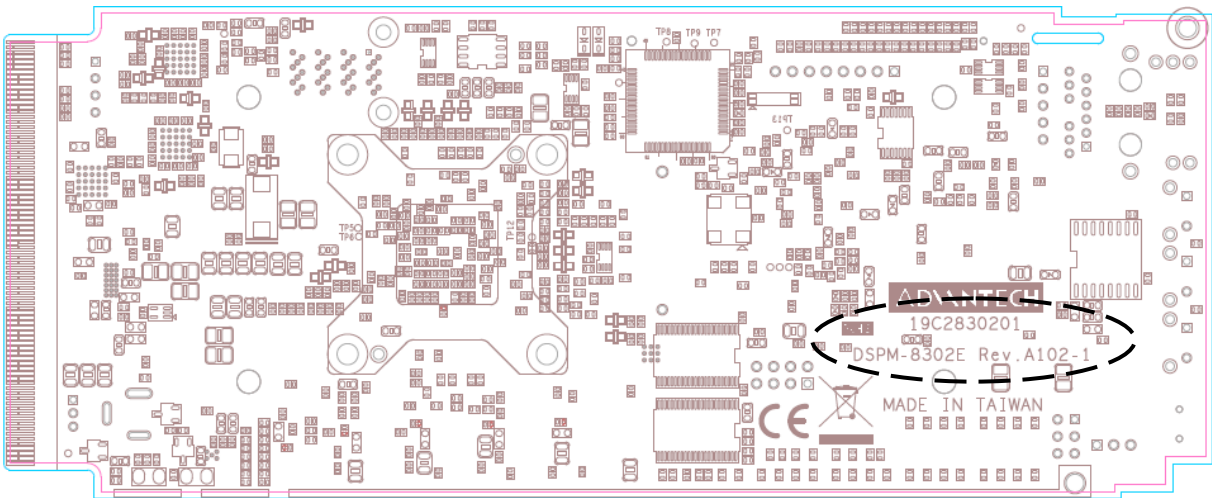

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2. TMDXEVM6670 Production EVM Enhancements

Several enhancements were implemented in the production EVM design released as Revision 2.0. These changes were implemented due to functional and feature deficiencies found in the Beta releases.

- Remove UCD9222 from FPGA JTAG chain to simplify this circuitry since the UCD9222 does not support boundary scan.
- Add pull-up resistor to PMBus_CTL as this signal being low prevents the FPGA from sequencing the CVDD and VCC1V0 supplies. This was resolved on the Beta boards by activating a pull-up resistor on this signal within the FPGA.
- Implement a 15A CVDD supply using the UCD74110 power stage device instead of the UCD7242 which is limited to 10A. This replaces half of the UCD7242 implemented on the Beta design. The UCD74106 power stage driver is implemented to replace the other half to supply the CVDD supply.

  Note that the CVDD design on Beta1 and Beta2 EVMs is limited to 10A maximum. Operation of the TMS320C6670 at temperatures above 75C and Antenna Interface higher speeds may require more than 10A.

  Customer designs must provide a CVDD supply that provides up to 15A such as the solution implemented on the production EVM design using the UCD74110.
- CVDD and CVDD1 layout modified with component placement and copper pours to keep majority of A/C ripple currents on top copper layer.
- Increased copper thickness to 1 oz. on top, bottom and all plane layers for the UCD74110 and UCD74106. This lowers the voltage drop due to the high output and ground currents flowing in the power supply and ground planes.
- HCSL support of the PCIE reference clock.

  Add a MUX buffer and selection method so that an FCLK from the AMC connector in the HCSL format can be used for PCIECLK as well as allowing the existing clock source to be selected. An FPGA upgrade is available that allows the user to set the sliding switch #4 bit 4 (BM_GPIO7) to switch the FCLK from the AMC to the DSP during PCIE boot.

  Note that the PCIE HCSL clock is not supported on Beta1 and Beta2 EVMs (PCB PN: 19C2830200, rev. A101-1).

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- UCD9222 temperature monitoring.

  On production EVM, there are three thermal sensors attached on UCD9222. Users can read these temperatures by using the "Fusion Digital Power Designer" program from TI through PMBus with the USB pod.

  - TEMP1 to an external sensor near CVDD power inductor to improve accuracy of load current estimates,
  - TEMP2 to the internal sensor within the UCD74106 and
  - IinMON (used as an auxiliary ADC input) connected to an external temperature sensor to monitor the PCB temperature near the DSP.

- Add pull-up resistors to the GPIO[15:1] pins and a pull-down resistor to GPIO[0] to keep them from floating after the FPGA stops driving them. Note that this change added a second pull-up resistor to the GPIO_11 net which already had a pull-up resistor for the NAND R/B functionality. Some production boards required R284 to be removed as the double pull-up prevented some boards from accessing NAND reliably.
- Add series termination resistors 22ohm at HyperLink sideband clock output pins.
- Correct footprint pin numbering of the HyperLink connector.
- Add circuitry so that JTAG emulation can also be driven from the AMC connector.
- Placement of the 3-pin UART connector was adjusted to avoid interference with the XDS560V2 mezzanine card.
- Correct HyperLink sideband signal directions in schematic – no layout changes.
- Move LEDs to side of board to prevent mezzanine and heatsink from covering them.
- Correct DIP switch order so that the individual switches number sequentially.

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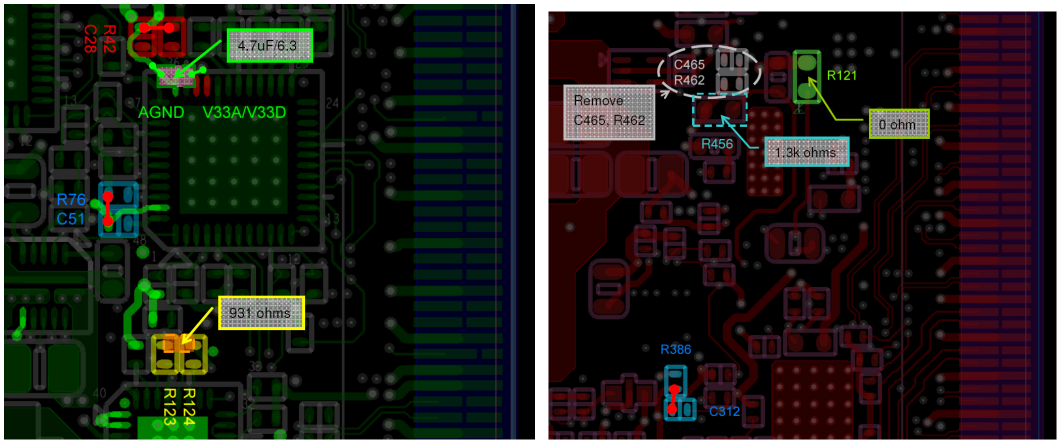
3. TMDXEVM6670 Production EVM Issues

A few of the Production EVM changes listed above caused other problems. These issues are listed below. All Production EVMs received ECNs at the factory to overcome these issues before they were shipped. Robust layout corrections have been implemented in the PCB design so that the next release does not have these problems.

3.1 CVDD / VCC1V0 Power-up issue on the EVM

The C6670 Rev 2.0 production EVMs (PCB number is 19C2830201 and the PCB version A102-1) had a power-up problem with the UCD9222, UCD74110 and UCD74106 power solution because of noise caused by UCD74110 grounding return path. The design of the power supplies on CVDD and VCC1V0 (CVDD1) rails needs below workarounds to fix the problem. All production boards received these corrections prior to shipment.

1. Connecting several AGND (named UCD9222_AGND) and digital ground (GND) points need to be done to reduce the noise on analog ground from the PowerPAD of UCD74110.
   a) AGND on C28 (AGND pin of UCD9222) and digital GND on R42 (topside of the PCB)
   b) AGND on C51 (AGND pin of UCD9222) and digital GND on R76 (topside of the PCB)
   c) AGND on C312 (CS1 pin of UCD9222 for sensing UCD74110 current) and digital GND on R386 (backside of the PCB)



2. The current sensing circuitry on UCD74110 was changed to match the DCR of the output inductor. This was required for proper current monitoring of the UCD74110 by the UCD9222.

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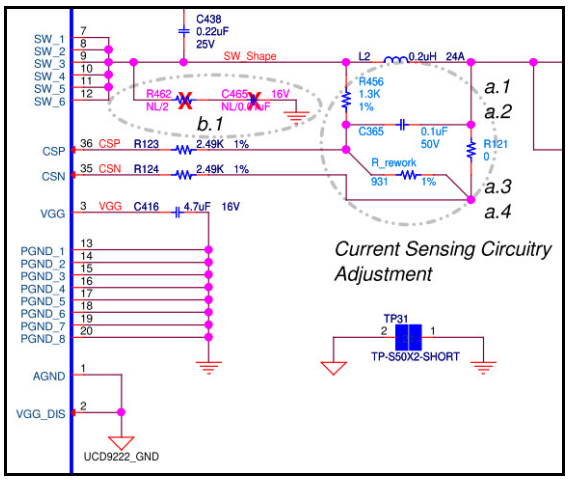
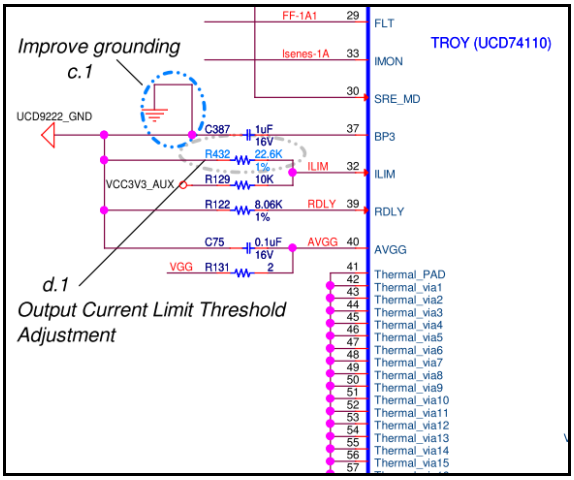
a) Modify R456 to 1.3k-ohm, C365 to 0.1uF, R121 to 0-ohm, and additional 931-ohm across the ends of R123 and R124 near C365 and R121 side for the correct current sensing;
b) Modify R432 to 22.6k-ohm for current limitation;
c) Remove R462 and C465.





3. Correct the ISENSE resistor to allow the UCD9222 to correctly sample the current estimate from the UCD74110.

   a) Modify R116 to 10k-ohm for correct current feedback from UCD74106.

4. Improve decoupling of the V33A pin of the UCD9222. Add an additional 4.7uF capacitor across the V33A and AGND pins. *Please note that the additional cap is not needed if there is a cap, such as C272 in below figure, placed on the same side with UCD9222 and adjacent the V33A and AGND pins of UCD9222*.

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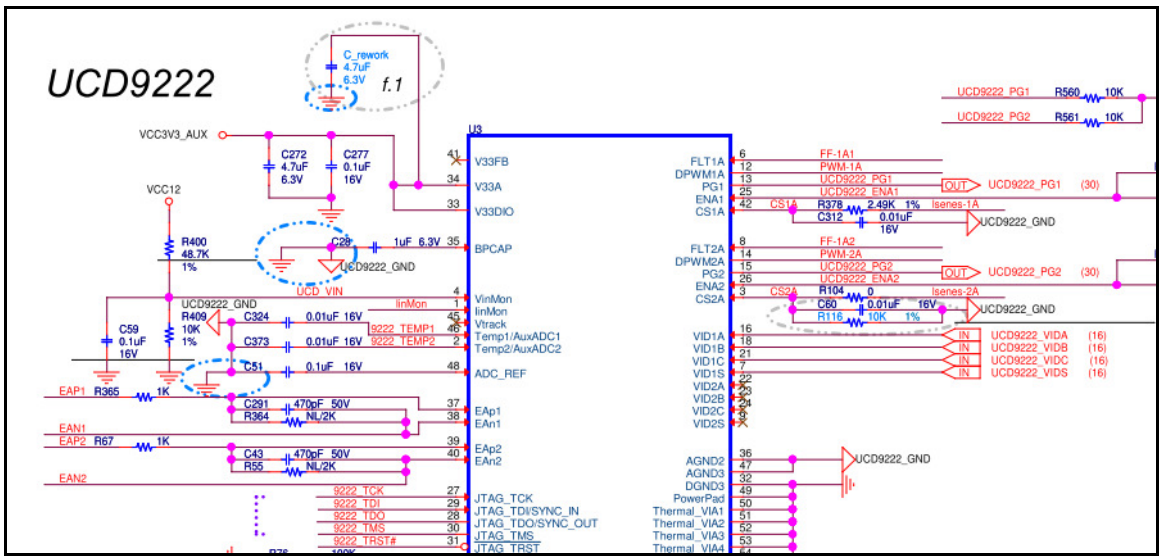
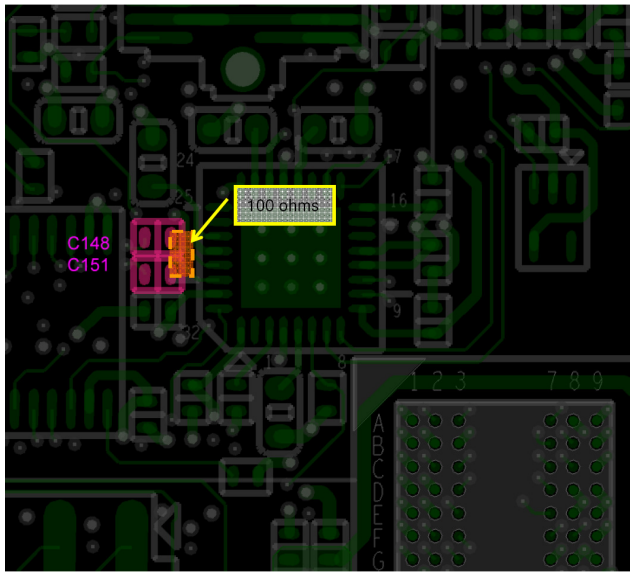


3.2 CDCE62002 PLL locking issue on the EVM

The C6670 Rev2.0 production EVMs require a termination resistor across the reference clock input of the CDCE62002. Lack of the termination allowed noise to be coupled onto the differential clock signal which prevented the PLL from locking robustly. This LVPECL clock signal should have a 100-ohm termination but it was omitted in the design.

The ECN is adding a 100-ohm resistor across the ends of C148 and C151 nearby the input of CDCE62002 to reduce the noise. It makes the output clock stable and PLL robustly locked.



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4. TMDXEVM6670 Revision 3 Enhancements Planned

Enhancements are being added to support development environments where AIF and HyperLink clock synchronization is needed between two EVMs. Those changes support these requirements.

4.1 AIF SERDES timing synchronization

a) The SNYC pin on CDCE62005 of CLK#3 connects to 80-pin expansion header to synchronize the RP1CLK outputs between two EVM boards for common timing;
b) The TCLKD LVDS clock from the AMC edge connector is driven into the CLK#3 PRIREF input to provide common reference timing for the AIF clocks between two EVM boards;
c) The TCLKC pins on the AMC connector can also be used for Timer 0 Input and Timer 0 Output for AIF timing alignment. TCLKC_P can be reused for the Timer 0 Output (TIMO0_AMC). TCLKC_N can be reused for the Timer 0 Input (TIMI0_AMC). The signal multiplexing is done in the FPGA so that the signals at the AMC connector will be 3.3V LVCMOS.
d) The RP1CLK is supplied from AMC connecter with DC-blocking by default and connections from additional routes from the local oscillator are not connected by default.

4.2 HyperLink timing synchronization:

a) The SYNC pin on CDCE62005 of CLK#2 connects to 80-pin expansion header to synchronize the MCMCLK outputs between two EVM boards for common timing;
b) The TCLKB LVDS clock from the AMC edge connector is driven into the CLK#2 PRIREF input to provide the common reference timing for the MCMCLK clocks between two EVM boards.

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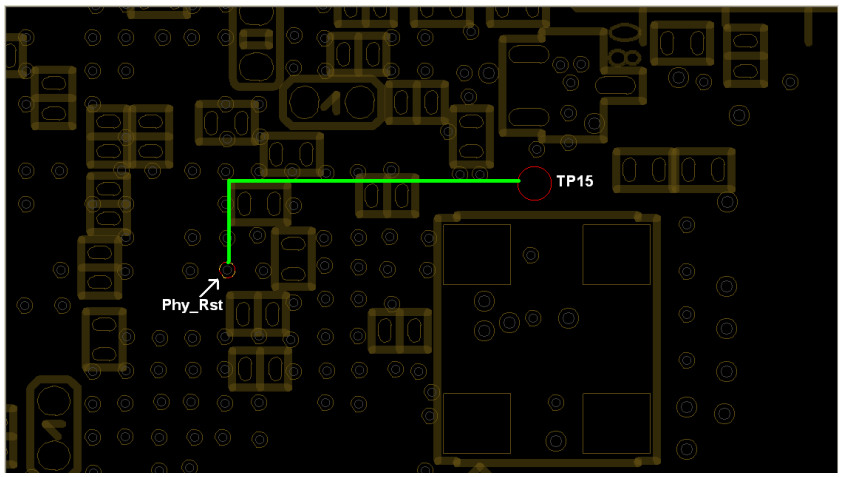
5. TMDXEVM6670 Beta EVM Design Changes

Preliminary versions of the EVM design were released during the EVM debug process and during EVM software integration. Therefore, the following section lists the design changes implemented after the first draft schematics were released so that users of these early schematics can see all of the changes implemented. All of these changes are contained in the latest design releases.

5.1 RESET# pin of the Gigabit Ethernet PHY of Marvel 88E1111 on the EVM

The Beta1 and Beta2 EVMs of C6670 were corrected before shipment. The RESET# (PHY_RST#) signal of 88E1111, the PHY of Gigabit Ethernet, was driven by an input pin K11 of FPGA instead output, it makes the PHY stay in reset state. The workaround is connecting the PHY_RST# to the TP15 pad of FPGA to fix the problem. The below figure shows the rework done on the PCB backside of Beta1 and Beta2 EVMs.



5.2 Unexpected EVM Reset Event

All Beta1 and Beta2 EVMs have a design erratum that may need to be corrected. Beta2 EVMs received this ECN before they were shipped from the factory. The TDI input to the FPGA is floating. This has been observed to allow unexpected FPGA behavior on a small percentage of the boards. Often the SYSPG_D1 LED goes out and CCS unexpectedly disconnects. A pull-up resistor needs to be added to prevent this from happening. This can be added on the bottom of connector TAP_FPGA1 between pins 1 and 5. Any resistor value between 1K and 10K will suffice. The following figure shows this rework.

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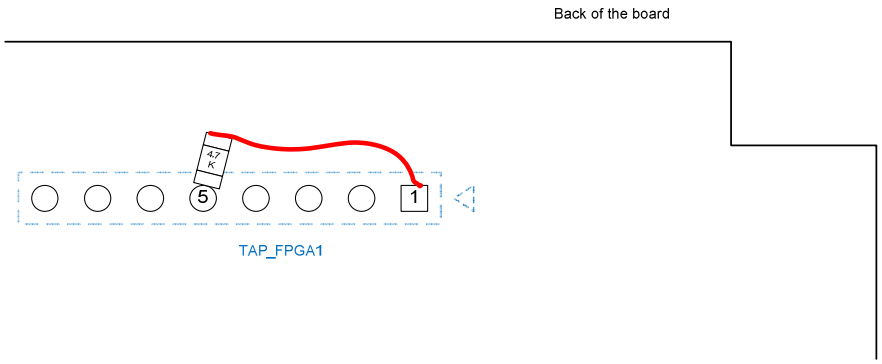
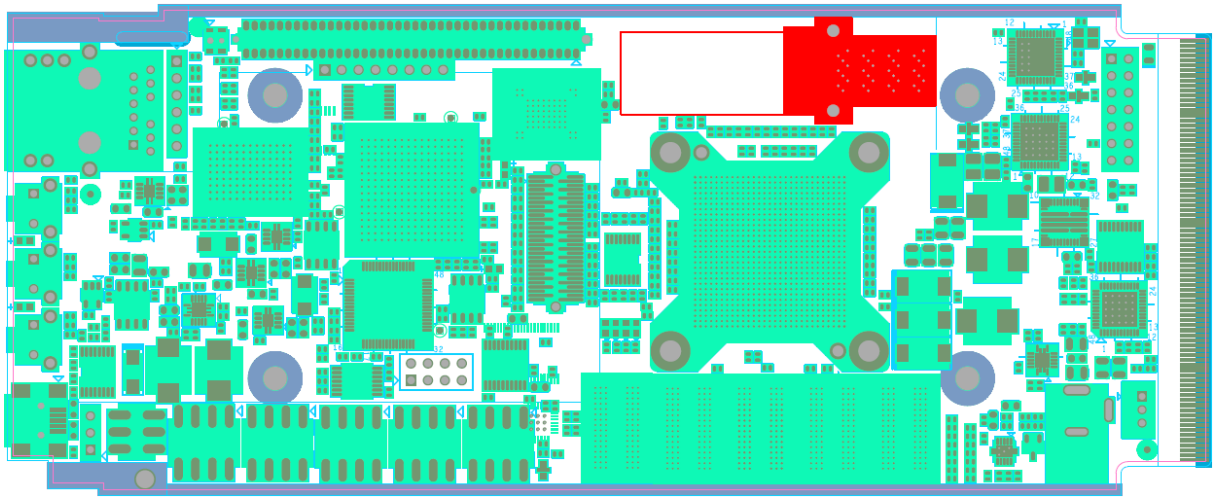


5.3 Incorrect pin out on the HyperLink1 connector on The EVMs

All Beta1 and Beta2 EVMs had populated the iPass+HD mini-SAS connector on the HyperLink1 for the HyperLink connection. The pin out on the HyperLink1 is incorrect. Many signals will be shorted if connecting the HyperLink interface by the cable. The HyperLink1 can NOT be used and should be removed on Beta1 EVMs. The HyperLink connectors were removed from Beta2 EVMs before they were shipped from the factory.



5.4 No HCSL support of the PCIE-CLK from the AMC FCLK on the EVMs

The PCIe clock circuitry does not support HCSL clock from AMC FCLK on Beta1 and Beta2 EVMs. Do NOT try to install the DC-blocking to provide a PCIe clock from the AMC edge connector.

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5.5 FPGA code update issue on the EVMs

The FPGA cannot be reprogrammed while the UCD9222 contains a configuration and it is operating. One solution requires erasing the configuration from the UCD9222 before programming the FPGA. The alternate and preferred solution is reprogramming the FPGA from the DSP with CCS connected. A utility to perform this is available.

5.6 Other minor design changes implemented on all Beta1 and Beta2 EVMs

The following minor design changes were implemented in Beta1 of the TMDXEVM6670 EVM design since the preliminary schematic released on April, 2011. All design revisions shipped contain these enhancements.

a) MMC (MSP430) always enabled when power is applied: remove R11, populate R16.
b) DDR3 slew rate setting set to FAST: remove R72, populate R70.
c) VCC5_AUX held in off state until enabled by FPGA: remove R237.
d) I2C SEEPROM changed to STMicro_M24M01-HRMN6TP so that it responded at addresses 50h and 51h as needed.
e) 3-pin header for RS-232 changed to contain locking clip.
f) NAND FLASH changed to 64MB part (Numonyx NAND512R3A2DZA6E).
g) DDR3 SDRAM chips changed to 1GB size (SAMSUNG_K4B1G1646G-BCH9).
h) Change DSP input clock rates to simplify development:
   SRIOSGMIICLK = MCMCLK =250MHz;
   CORECLK = PASSCLK = SYSCLK = 122.88MHz;
   PCIECLK = 100MHz

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6. TMDXEVM6670 Future Correction

The DDRSLRATE[1:0] pins of the C6670 DSP are 1.8V LVCMOS inputs. The EVM design incorrectly pulls then to 1.5V (DVDD15). This is a non-critical issue that should be fixed in a future release. The 1.5V input will always be above the Vih(min) of the 1.8V LVCMOS input. This issue will not cause a design problem but it does cause confusion. All customer designs should pull the DDRSLRATE[1:0] pins to either 1.8V or Ground.