

TMS320C6670 EVM Board for TI

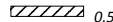











Product name : DSPM-8302E

Rev. A101-1

PCB PN : 19C2830200

Project Code :

PCB Thickness : 62 mils(1.6mm)
12 Layers

TOP		0.5 oz	3mils	p,p
L2_GND		0.5 oz	4mils	core
L3		0.5 oz	7mils	p,p
L4_PWR		0.5 oz	6mils	core
L5		0.5 oz	4.5mils	p,p
L6_GND		0.5 oz	4mils	core
L7_GND		0.5 oz	4.5mils	p,p
L8		0.5 oz	6mils	core
L9_PWR		0.5 oz	7mils	p,p
L10		0.5 oz	4mils	core
L11_GND		0.5 oz	3mils	p,p
BOT		0.5 oz		

DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS.

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TI Information - Selective Disclosure
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20450 Century Blvd
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USA

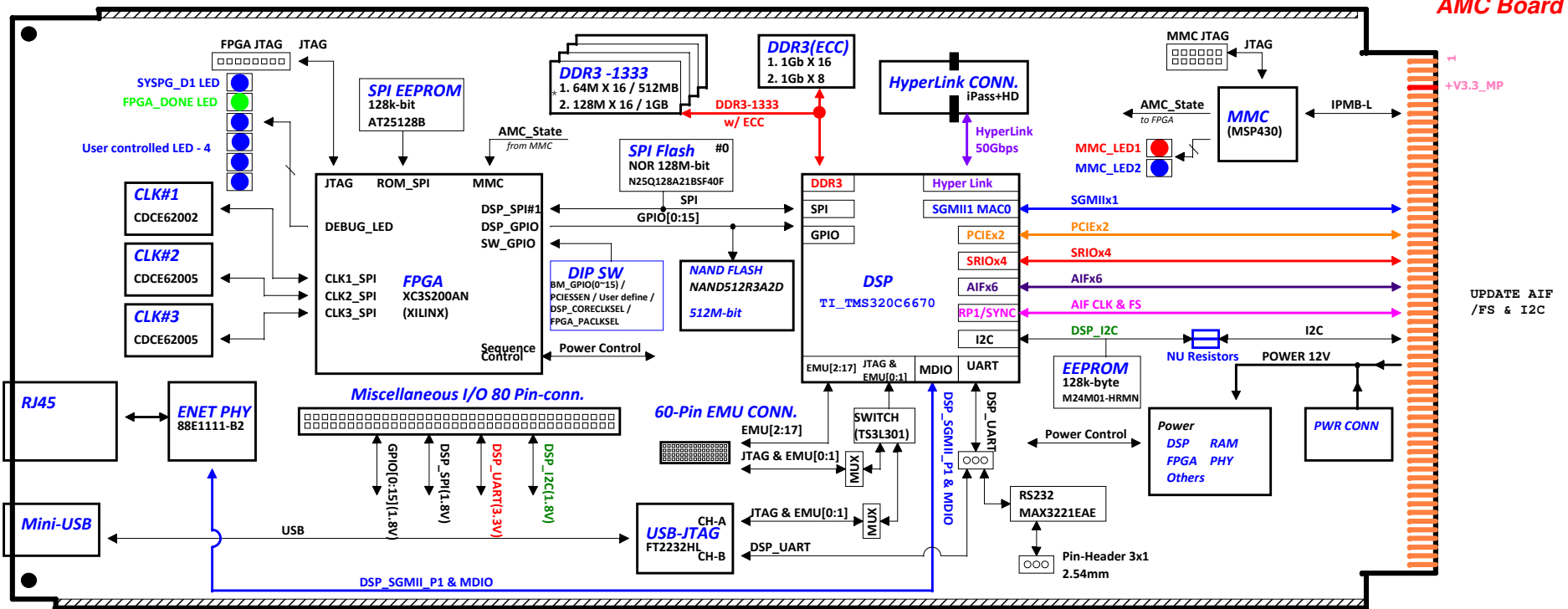
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TMS320C6670 EVM BLOCK DIAGRAM

AMC Board



Miscellaneous I/O 80 Pin conn. Signal

PIN	Port mapping	PIN	Port mapping	PIN	Port mapping
02		42		01	Gnd
04		44		03	SDA
06		46		05	SCL
08		48		07	
10		50	GPIO00	09	
12		52	GPIO01	11	
14		54	GPIO02	13	
16		56	GPIO03	15	
18		58	GPIO04	17	
20		60	GPIO05	19	
22		62	GPIO06	21	
24		64	GPIO07	23	
26		66	GPIO08	25	
28		68	GPIO09	27	
30		70	GPIO10	29	
32		72	GPIO11	31	
34		74	GPIO12	33	
36		76	GPIO13	35	
38		78	GPIO14	37	
40		80	GPIO15	39	

AMC Port mapping

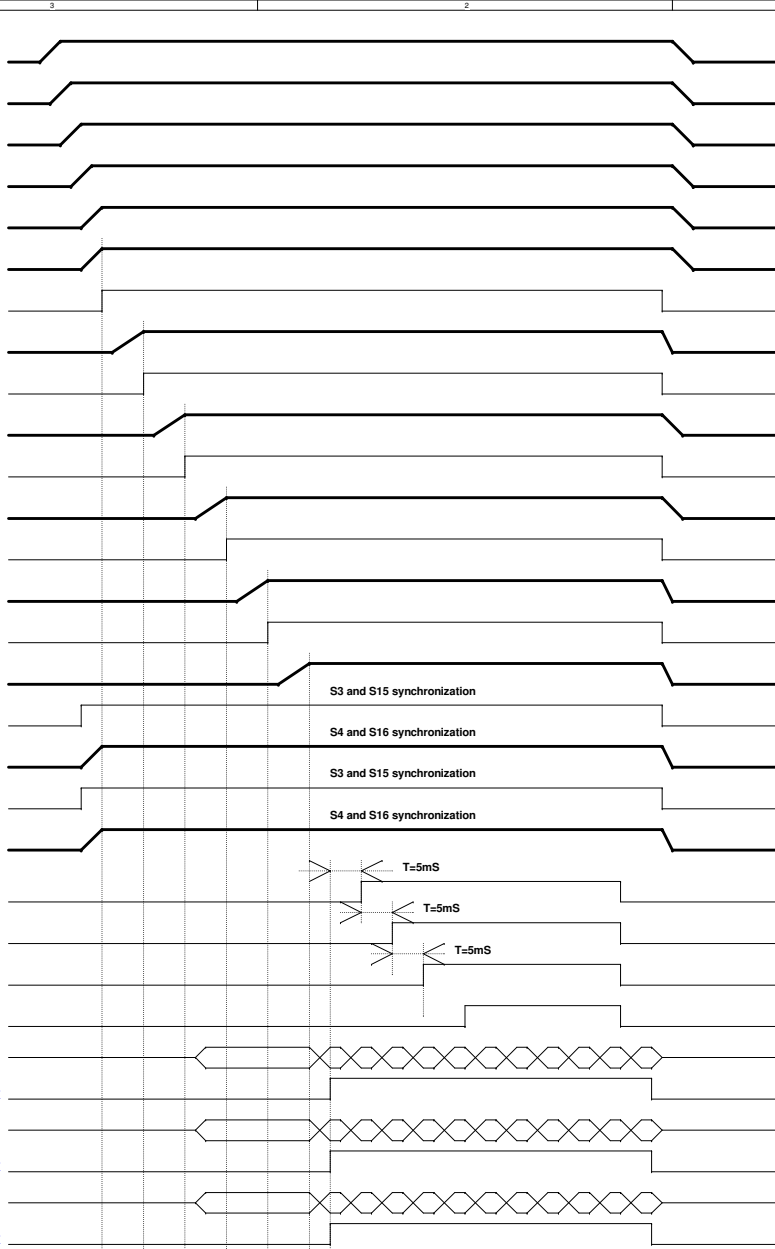
PIN	Port mapping	PIN	Port mapping
41		11	SRIO_4
43		12	AIF_0
45		13	AIF_1
47		14	AIF_2
49		15	AIF_3
51		16	TCLKC TCLKD
53		17	AIF_4
55	TIMIO	18	AIF_5
57	TIM00	19	AIF_CLK & FS
59	TIM11	20	Expansion I2C
61	TIM01		
63	SSPMISO		
65	SSPMOSI		
67	SSPCS1		
69	SSPCK		
71	UARTTXD		
73	UARTRXD		
75	UARTRTS		
77	UARTCTS		
79	Gnd		

Power Sequence

Label	Time	Description
T0	1ms	S2 plane power stable to S3 enable signal assertion

Signal	Device	Power Plane
S0	MMC	VCC3V3_MP_AMC
S1		VCC12
S2	Other FT2232H XC3S200AN	VCC3V3_AUX
S3	XC3S200AN	VCC1V8_AUX
S4	88E1111 XC3S200AN	VCC1V2
S5		PMBUS & UCD9222_ENA1
S6	DSP TMS320C6670	CVDD
S7		UCD9222_VID2 & UCD9222_ENA2
S8	DSP TMS320C6670	VCC1V0
S9		VCC1V8_EN
S10	DSP TMS320C6670	VCC1V8
S11		VCC1V5_EN
S12	DDR3 DSP TMS320C6670	DDR3 SDRAM VCC1V5
S13		VCC0V75_EN
S14	DDR3 DSP TMS320C6670	DDR3 Vref VCC0V75
S15		VCC2V5_EN
S16	88E1111	VCC2V5
S17		VCC5_EN
S18	XDS560V2 Mazzenine Board	VCC5

RESET#	
POR#	
RESETFULL#	
RESETSTAT#	
REFCLKP&N by REFCLK1_PD#	
CLOCK1_PLL_LOCK	
REFCLKP&N by REFCLK2_PD#	
CLOCK2_PLL_LOCK	
DDRCLKP&N by REFCLK3_PD#	
CLOCK3_PLL_LOCK	



Power Sequence

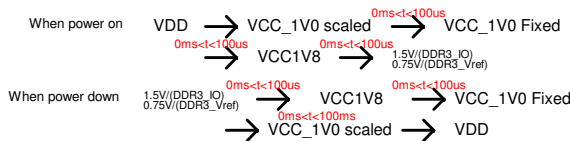
Reset Sequence

CLK Sequence

There is no specific power-up nor power-down sequence.

XILINX_XC3S200AN
1.2V_AUX (VCCINT)
1.8V_AUX (VCC1V8_AUX)
3.3V_AUX (VCCAUX)

XILINX_XC3S200AN

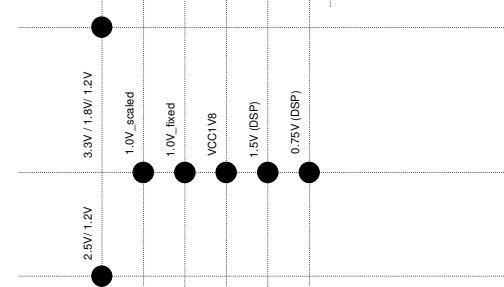


DSP TMS320C6670
VCC1V0 Scaled/(CVDD)
VCC1V8 Fixed/(CVDD1)
VCC1V8/(DVD18)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

DSP TMS320C6670

88E1111 (PHY)

88E1111



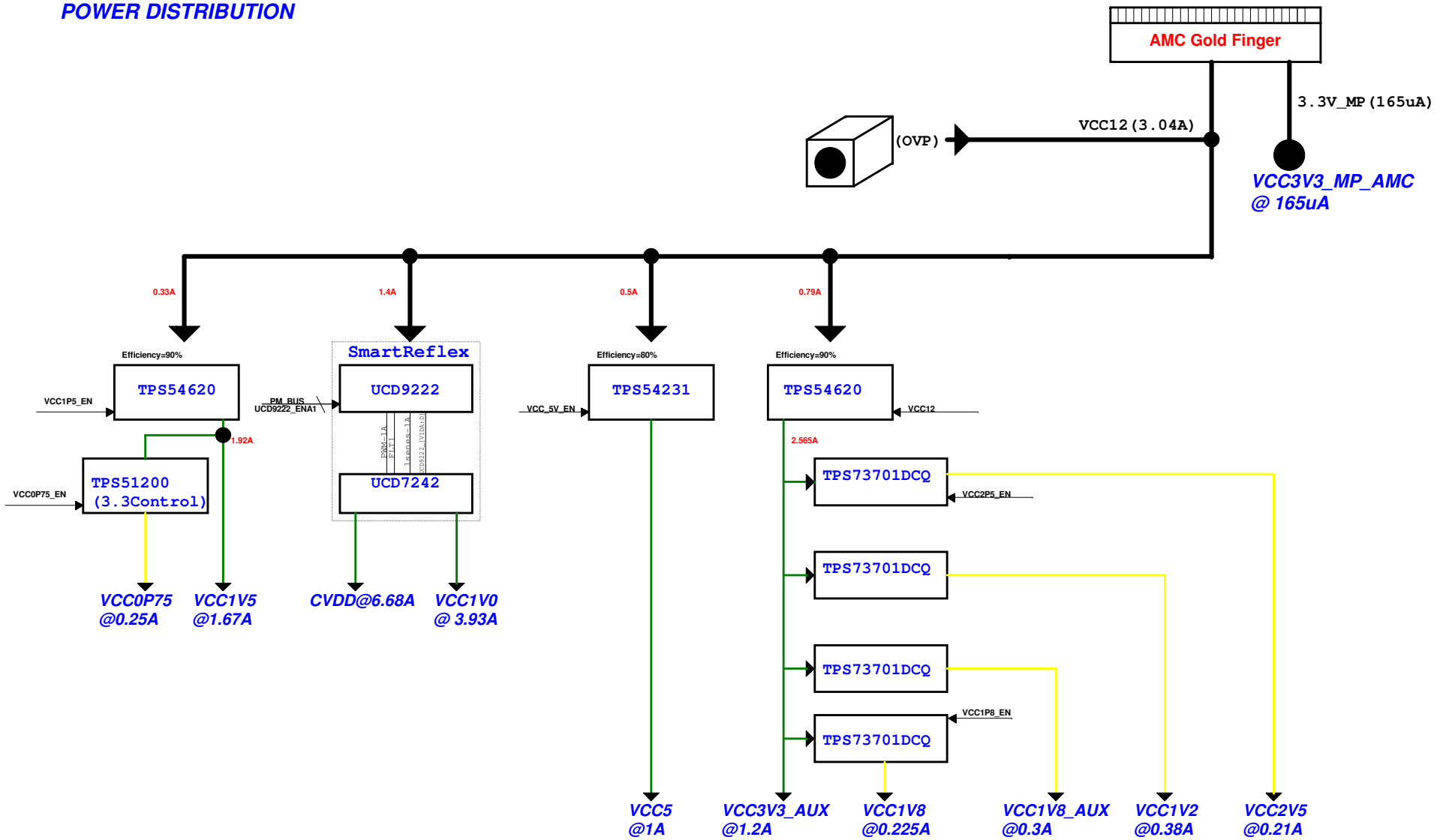
POWER CONSUMPTION

TMS320C6670 At application the total power near consumption 11.6W

$$\begin{aligned}
 11.6W * 57.64\% &= 6.68W = 1.0V @ 6.68A \\
 11.6W * 33.87\% &= 3.93W = 1.0V @ 3.93A \\
 11.6W * 6.13\% &= 0.71W = 1.5V @ 0.47A \\
 11.6W * 2.36\% &= 0.27W = 1.8V @ 0.15A
 \end{aligned}$$

	V	I	Qty	Isub.	Efficiency	Max. Power Design			Operating (for Thermal)		Note
						Pd (W)	I12V	I3vsb	Utilization	Pd (W)	
1.0V Adjustable core (12V-->1.0V)				6.680			0.696				UCD9222 + UCD7242
TMS320C6670	1.00	6.680	1	6.680	80%	8.350	0.696	x	70%	5.845	
1.0V Fixed core (12V-->1.0V)				3.930			0.364				TP554620
TMS320C6670	1.00	3.930	1	3.930	90%	4.367	0.364	x	70%	3.057	
1.5V (12V-->1.5V)				1.920			0.267				TP554620
TMS320C6670	1.50	0.470	1	0.470	90%	0.783	0.065	x	70%	0.548	
DDR3	1.50	0.240	5	1.200	90%	2.000	0.167	x	100%	2.000	
0.75V(VTT for DDR3) 1.5V-->0.75V							x				TP551200
DDR3	0.75	0.050	5	0.250	45%	0.417	0.035	x	70%	0.292	
3.3V_AUX (12V-->3.3V_AUX)				1.000			0.690				TP554620
FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
XDS560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
1.2V_AUX (3.3V_AUX-->1.2V_AUX)							x				TP573701DCQ
FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
1.8V (3.3V_AUX-->1.8V_AUX)							x				TP573701DCQ
FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
1.8V (1.8V_AUX-->1.8V)							x				TP573701DCQ
TMS320C6670	1.80	0.150	1	0.150	46%	0.587	0.049	x	70%	0.411	
FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
2.5V (3.3V-->2.5V)							x				TP573701DCQ
88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
5V (12V-->5V)				1.000			0.490				TP554231
XDS560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
3.3V_MP (150mA)				0.048			x	0.048			
MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
Total power consumption						Pmax.	I12V	I3VSB		Pop.	
						30.233	2.506	0.096		21.763	

POWER DISTRIBUTION



DDR3
 1.5V / 0.24A (VDD)*5 Total:1.2A
 0.75V / 0.25A (Vref)

Quad Core DSP
 TI_TMS320C6670
 VCC1V0 / 6.68A Scaled/(CVDD)
 VCC1V0 / 3.93A Fixed/(CVDD1)
 VCC1V8 / 0.15A (VDD18)
 1.5V / 0.47A (DDR3_IO)
 0.75V/(DDR3_Vref)

RS232
 3.3V

XDS560V2
Mazzenine Board
 5.0V / 1A
 3.3V / 0.3A

EEPROM
 3.3V

FT2232H(USB-JTAG)
 3.3V / 0.21A
 1.8V / 0.075A

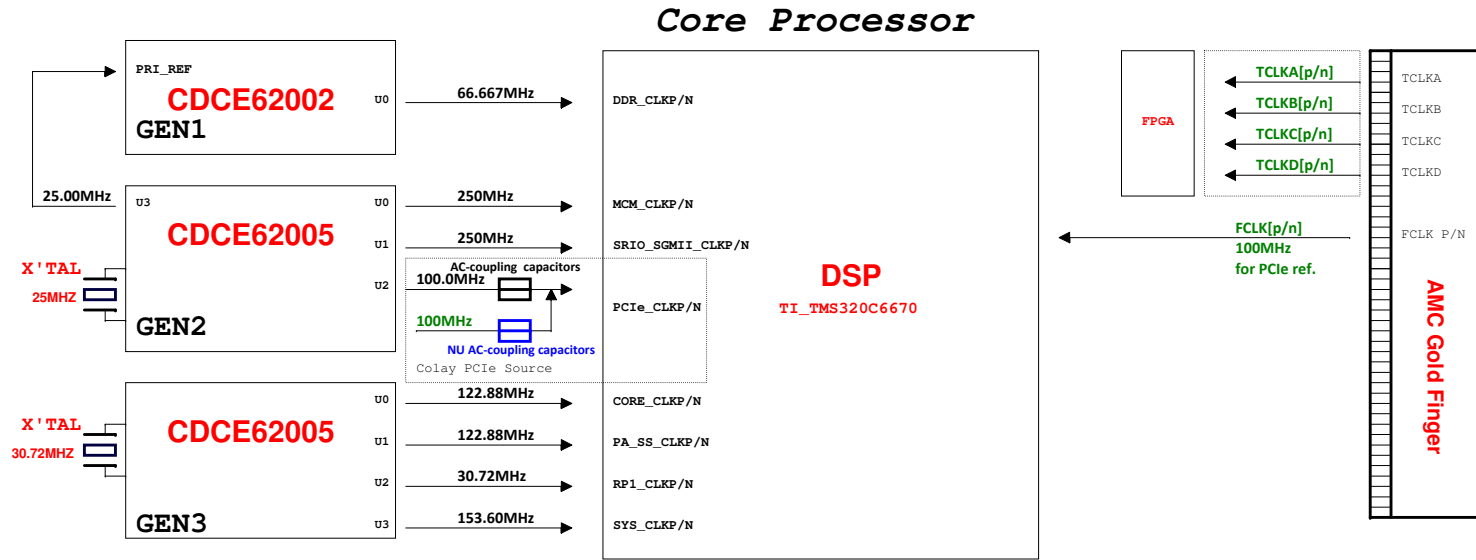
MicronNAND FLASH
 1.8V / 0.02A

NOR FLASH
 Standby mode 1.8V/80uA

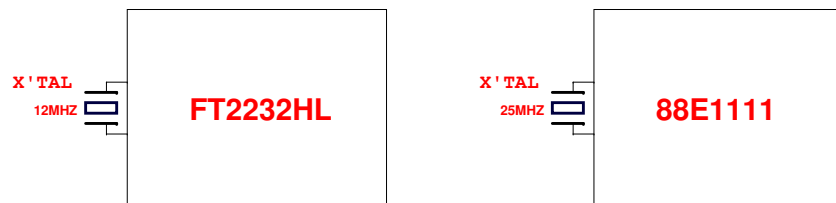
XILINX_XC3S200AN
 1.2V_AUX/ 0.125A (VCCINT)
 3.3V_AUX/ 0.024A (VCCAUX)

88E1111 (PHY)
 2.5V / 0.21A
 1.2V / 0.25A

CLOCK DIAGRAM

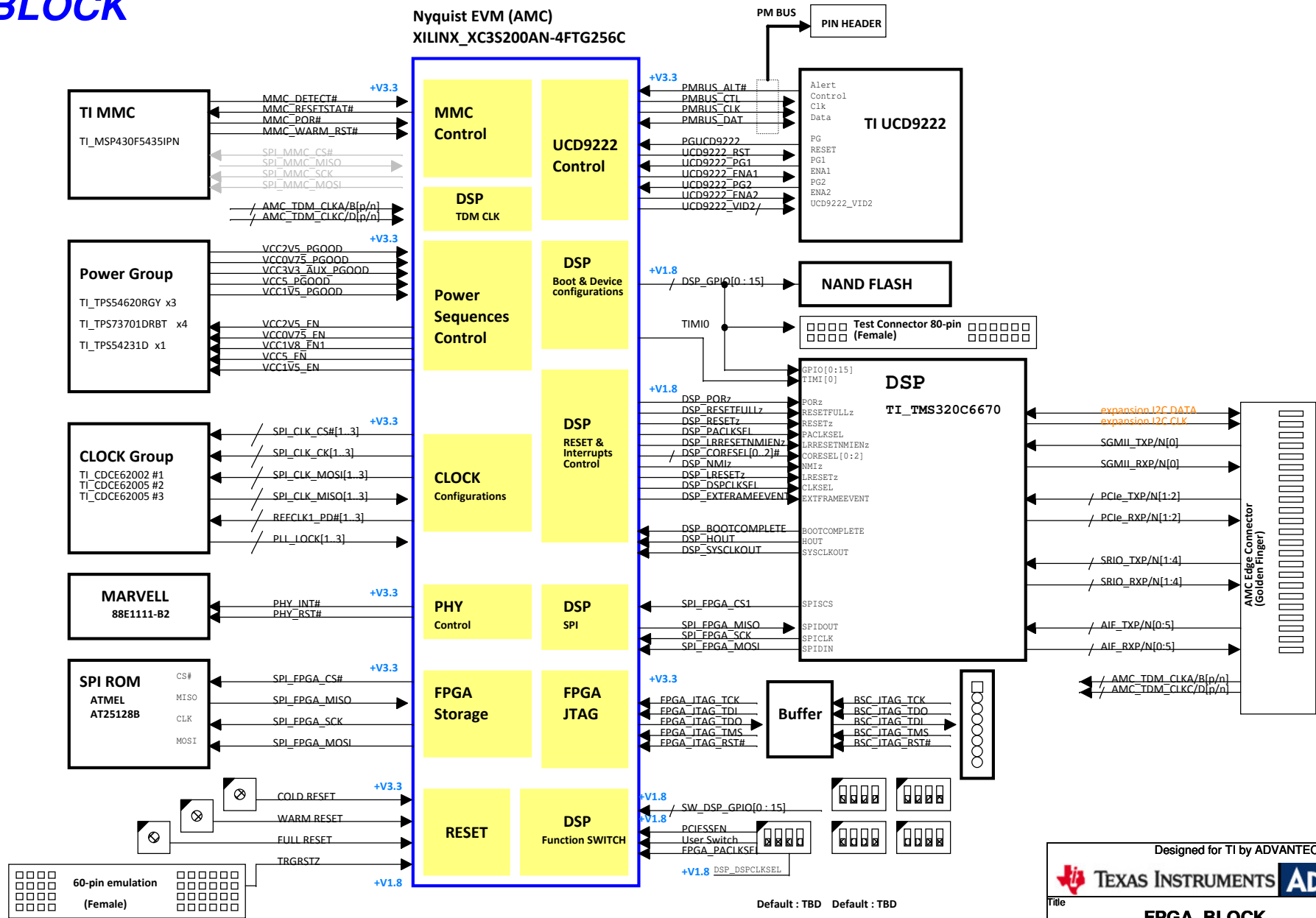


Decive Control



FPGA_BLOCK

Nyquist EVM (AMC)
XILINX_XC3S200AN-4FTG256C



Default : TBD Default : TBD

GPIO[0:3] GPIO[8:11]
GPIO[4:7] GPIO[12:15]

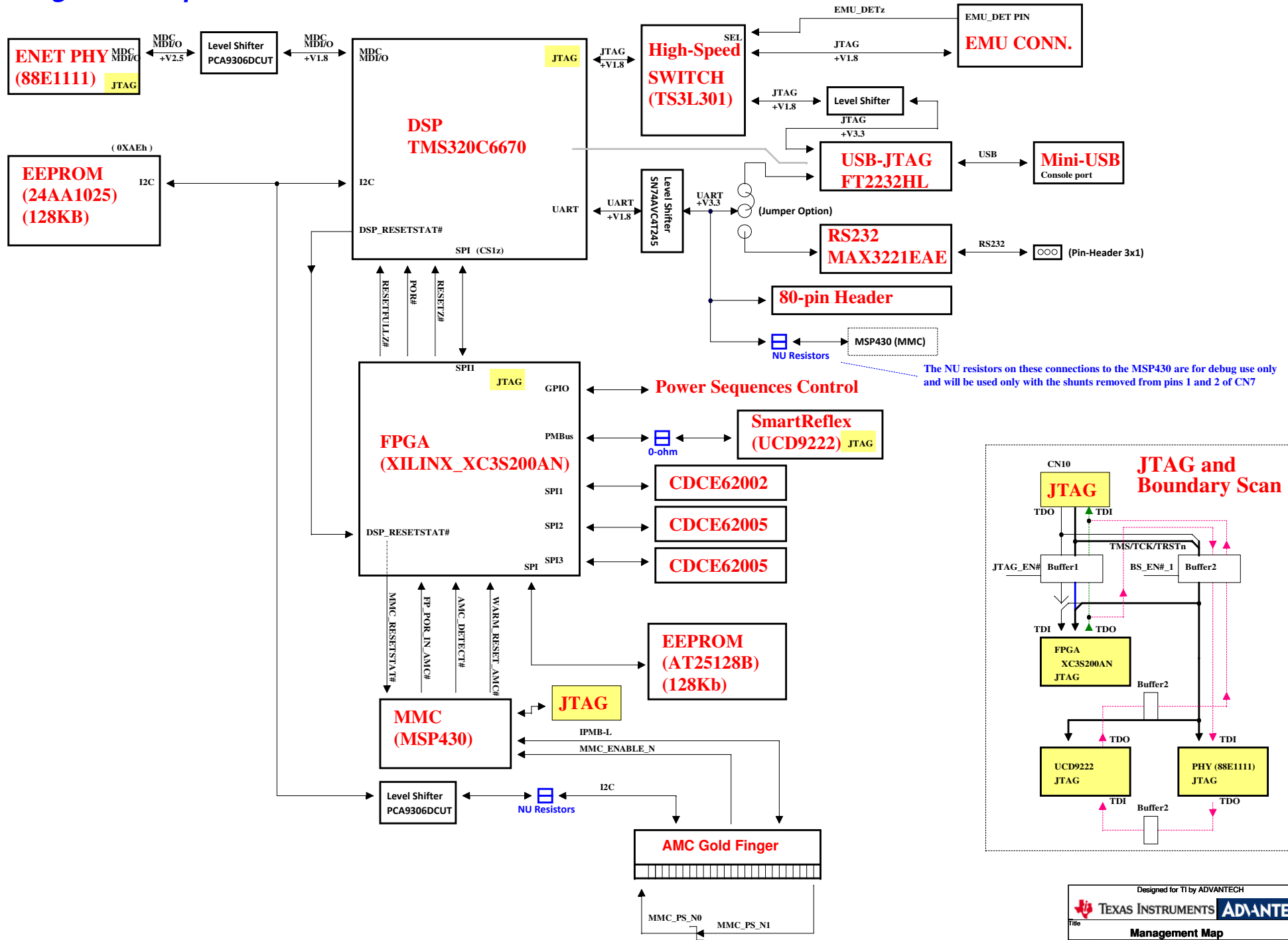
Designed for TI by ADVANTECH

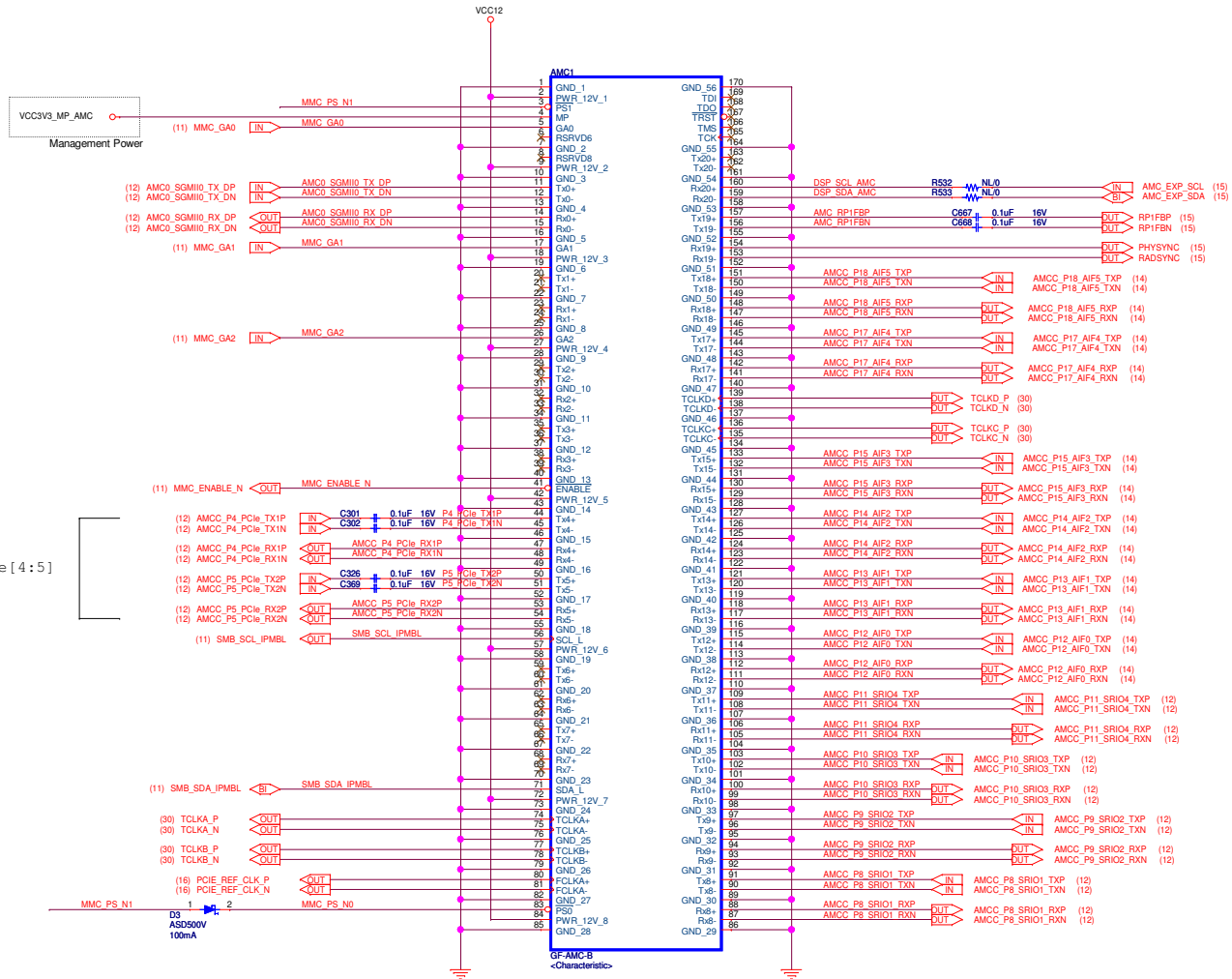
Title: **FPGA_BLOCK**

Size: **B** Document Number: **DSPM-8302E** Rev: **A101-1**

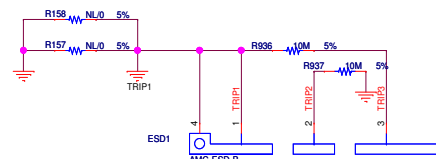
Date: Wednesday, March 16, 2011 Sheet 8 of 36

Management Map

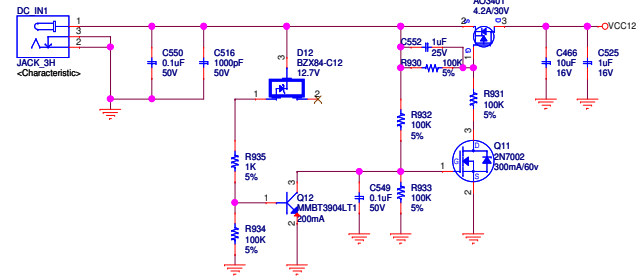




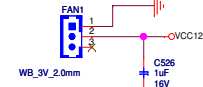
Front panel and ESD Strip



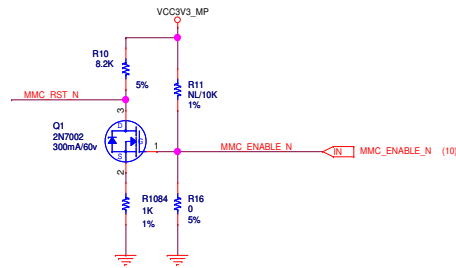
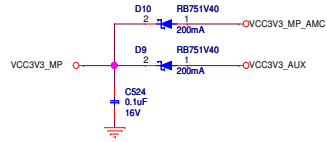
OVP: ~12.7V+0.6V = ~13.3V



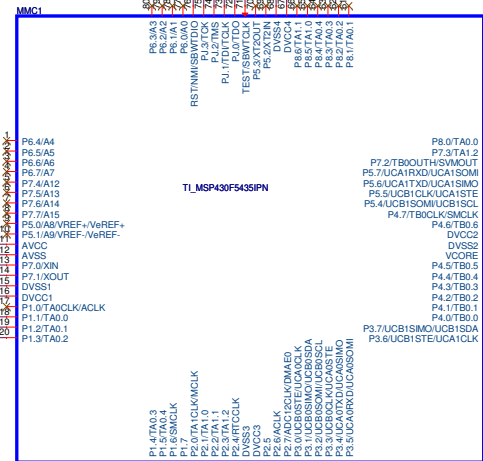
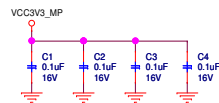
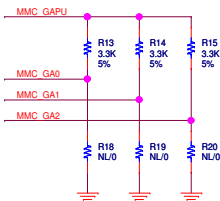
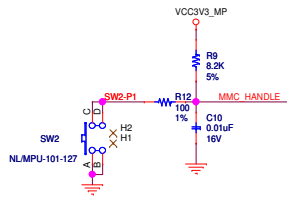
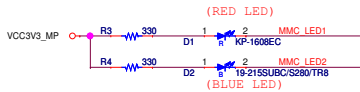
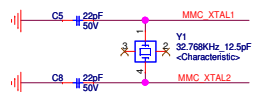
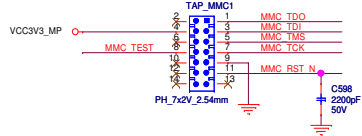
FAN DC Connet for DSP



Power for MSP430

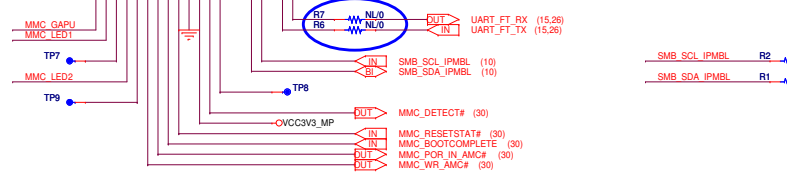


MMC JTAG

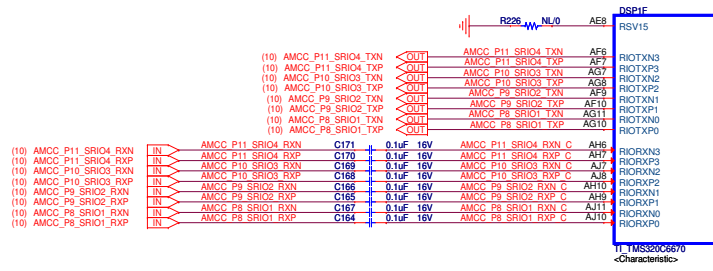


SPI I/F is for Advantech FPGA debugging.

The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7

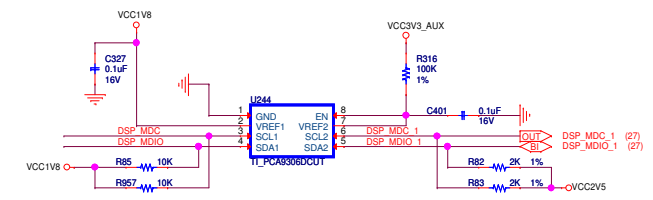
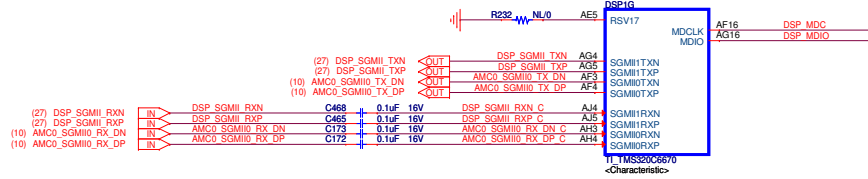


SRIO

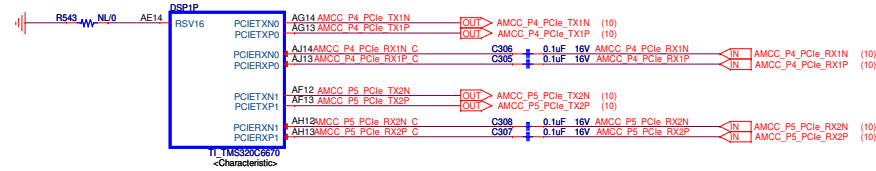


Caution!
 "Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

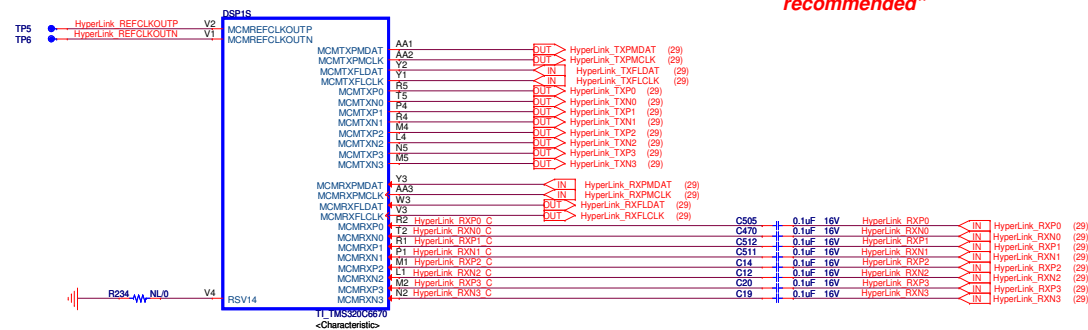
SGMII



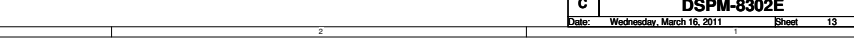
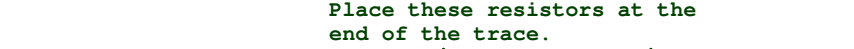
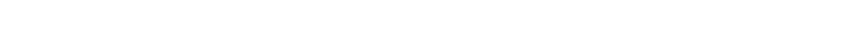
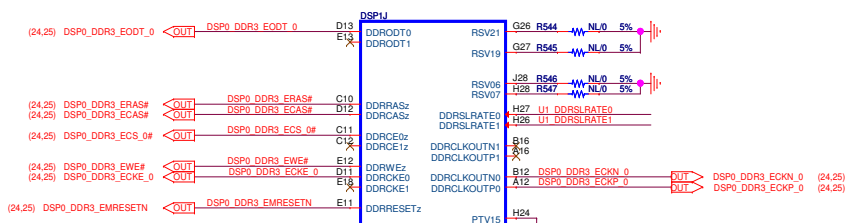
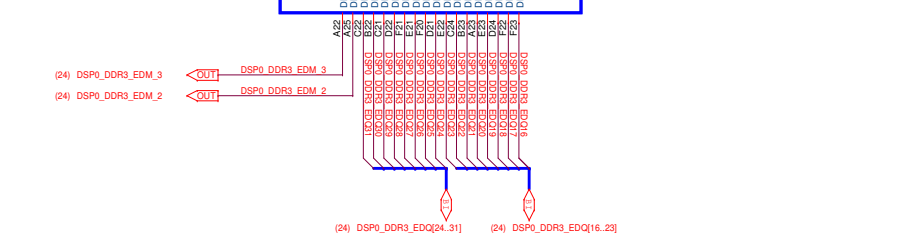
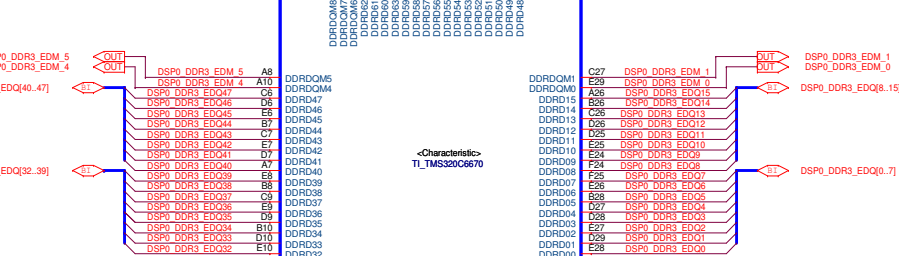
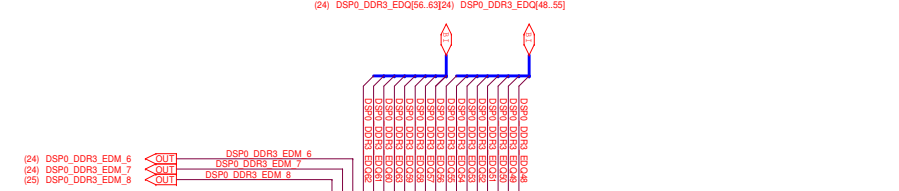
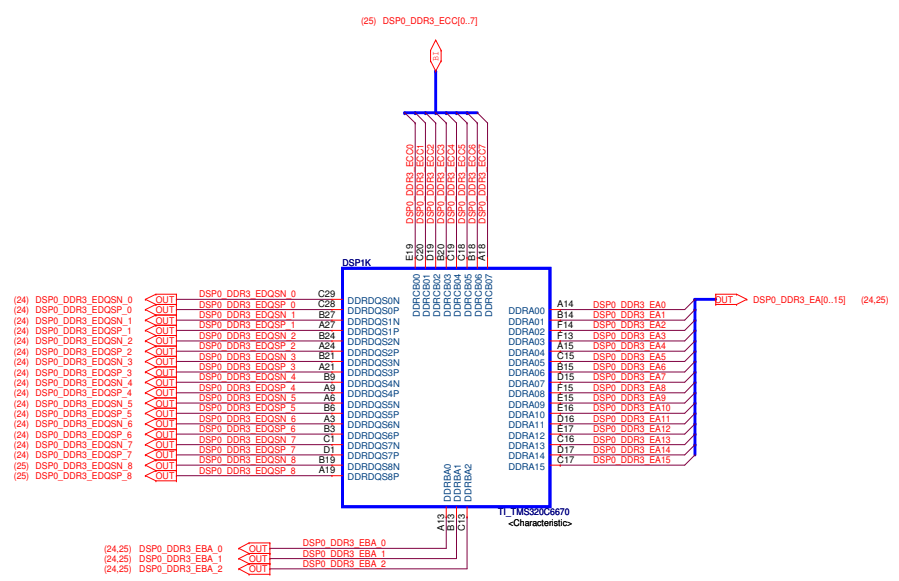
PCIE



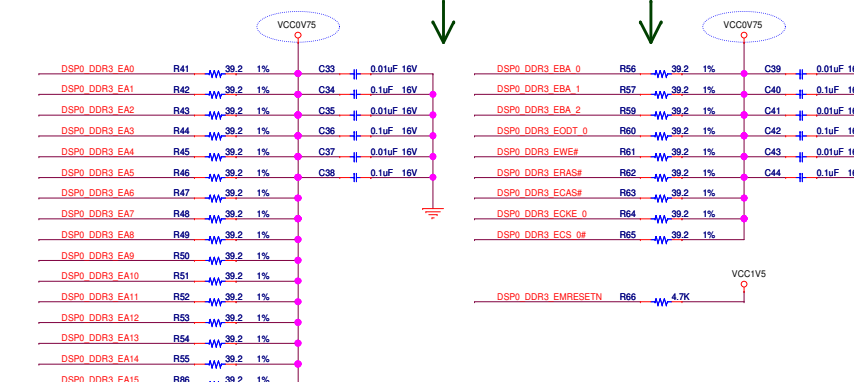
MCM



"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"

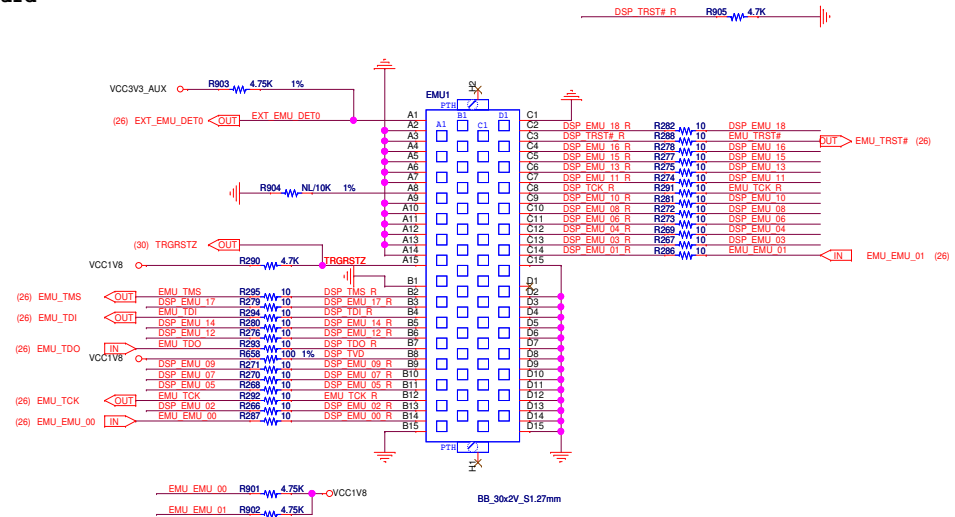
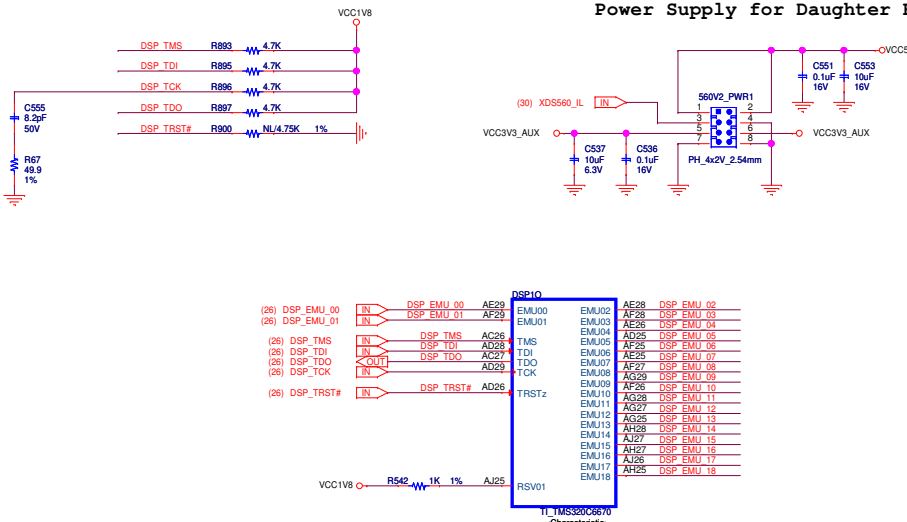


Place these resistors at the end of the trace.

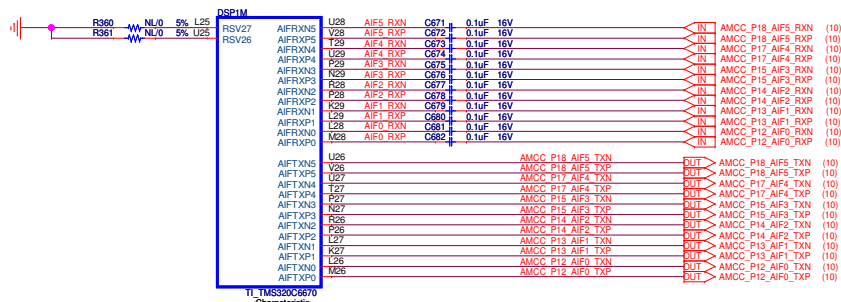


JTAG & EMU

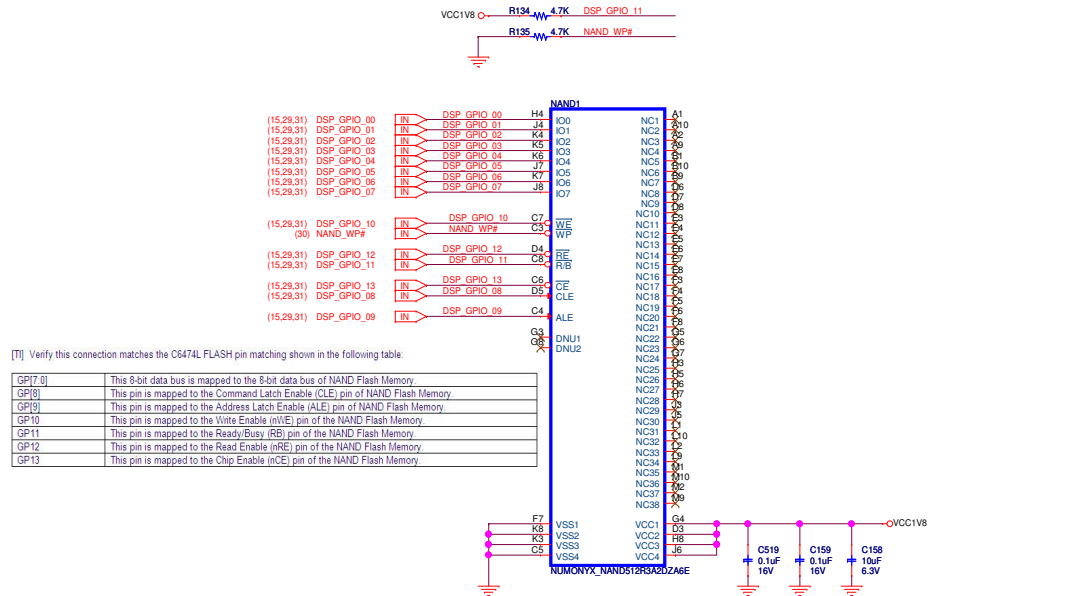
Power Supply for Daughter Board



DSP AIF



NAND FLASH

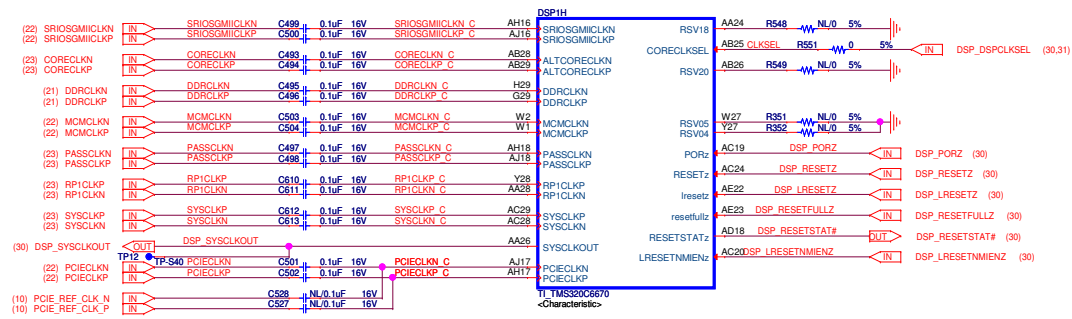


[T] Verify this connection matches the C6474L FLASH pin matching shown in the following table:

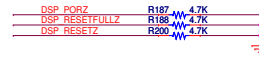
Pin	Signal	Value
GP[7:0]	This 8-bit data bus is mapped to the 8-bit data bus of NAND Flash Memory.	
GP[8]	This pin is mapped to the Command Latch Enable (CLE) pin of NAND Flash Memory.	
GP[9]	This pin is mapped to the Address Latch Enable (ALE) pin of NAND Flash Memory.	
GP[10]	This pin is mapped to the Write Enable (WE) pin of the NAND Flash Memory.	
GP[11]	This pin is mapped to the Ready/Busy (RB) pin of the NAND Flash Memory.	
GP[12]	This pin is mapped to the Read Enable (RE) pin of the NAND Flash Memory.	
GP[13]	This pin is mapped to the Chip Enable (CE) pin of the NAND Flash Memory.	

DSP CLOCK / RESET

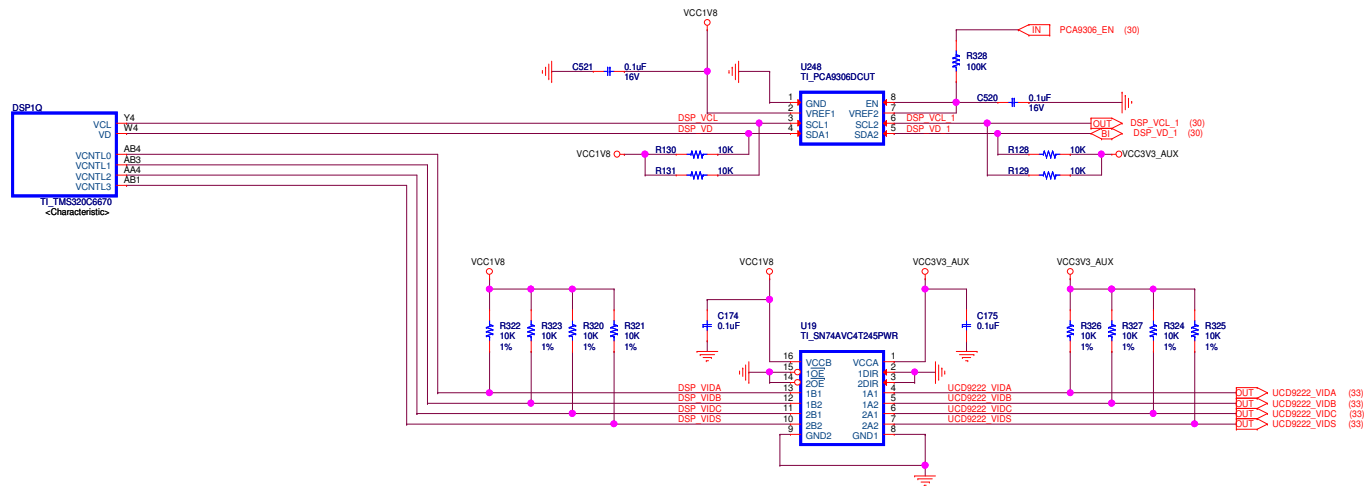
- 312.50MHz Input
- 122.88MHz Input
- 66.67MHz Input
- 312.50MHz Input
- 122.88MHz Input
- 30.72MHz Input
- 153.60MHz Input
- 156.25MHz Input



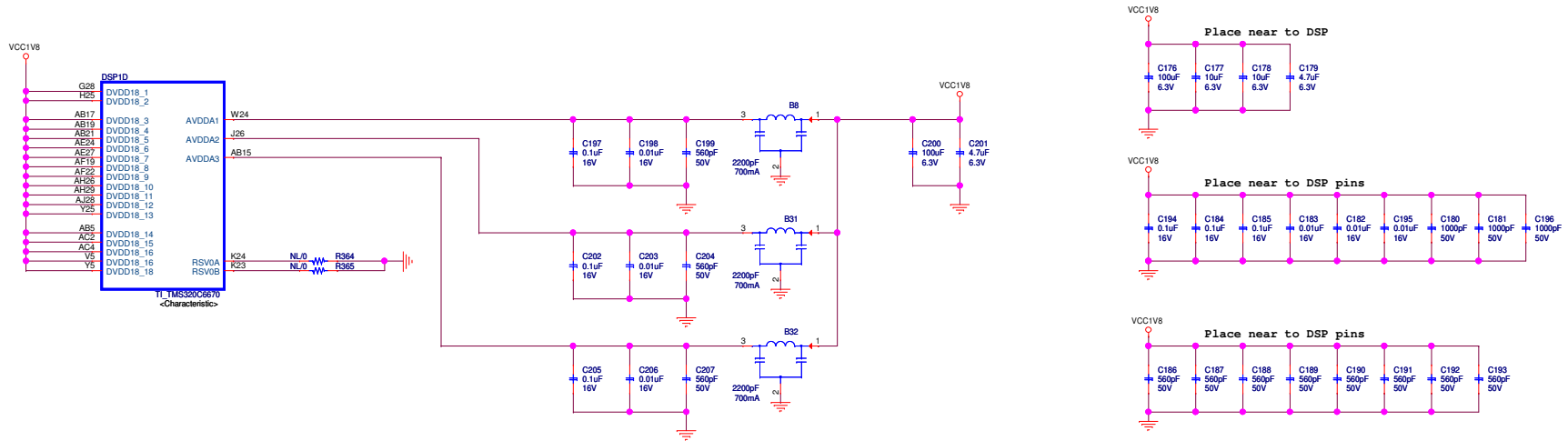
All blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias



Smart Reflex



1.8V

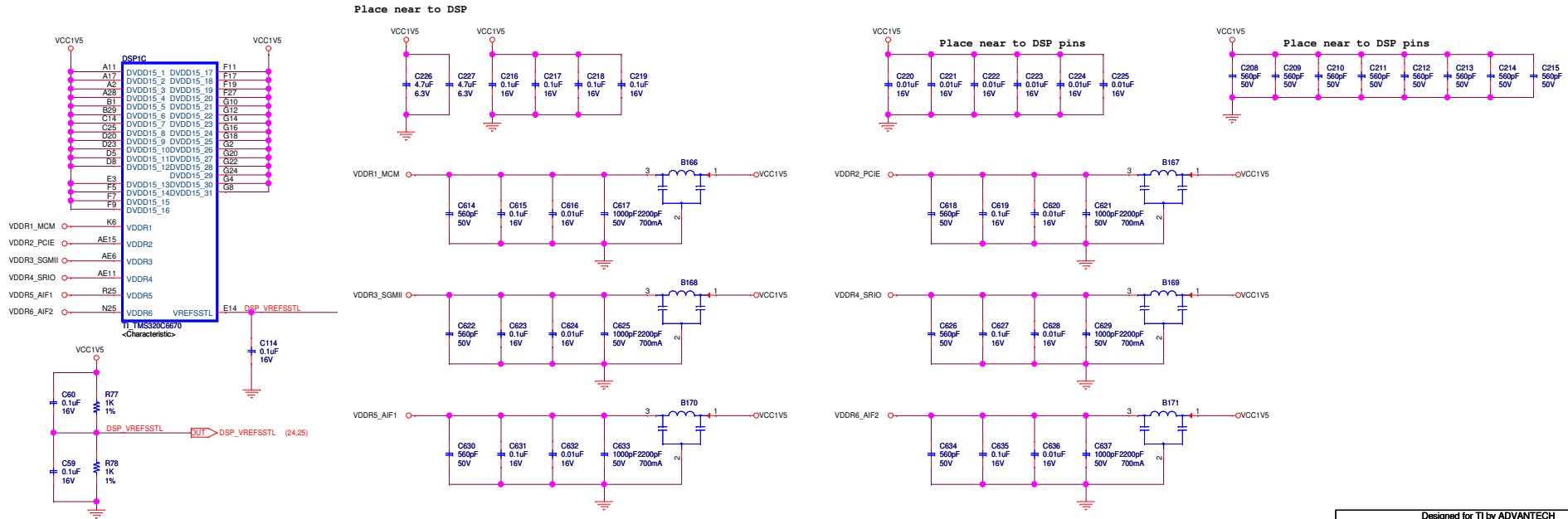


Place near to DSP

Place near to DSP pins

Place near to DSP pins

1.5V



Place near to DSP

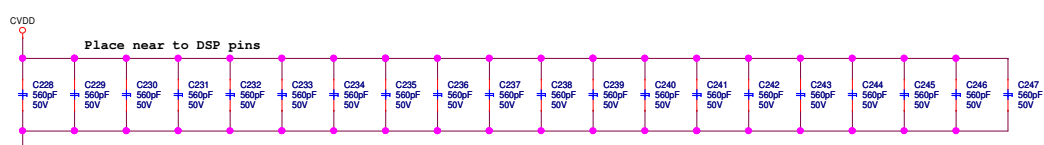
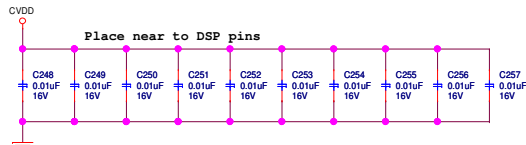
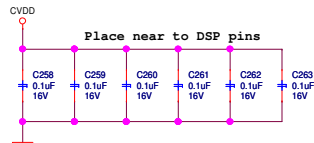
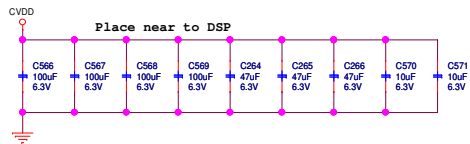
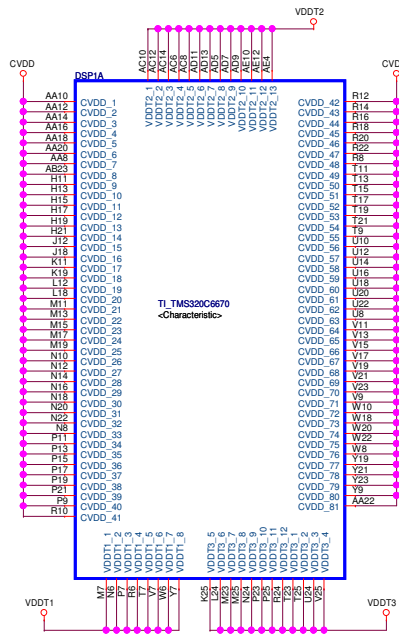
Place near to DSP pins

Place near to DSP pins

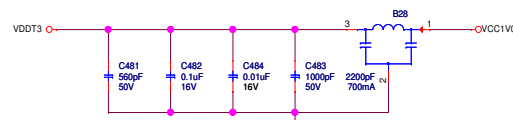
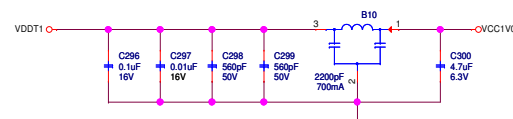
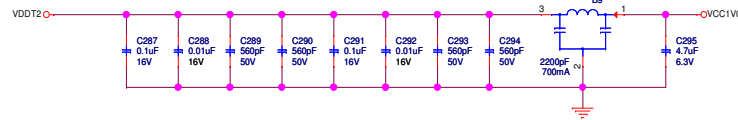
Trace need 20 mil.

0.9V - 1.1V (CVDD) (Smart Reflex)

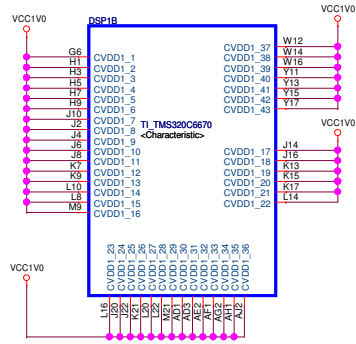
Fix_1.0V(VCC1P0)



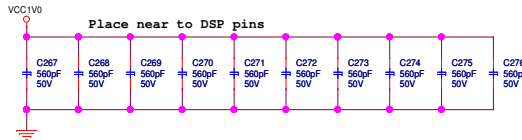
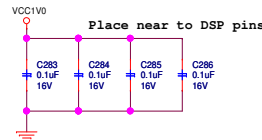
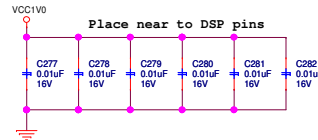
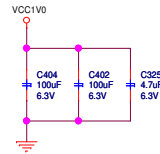
Place near to DSP pins

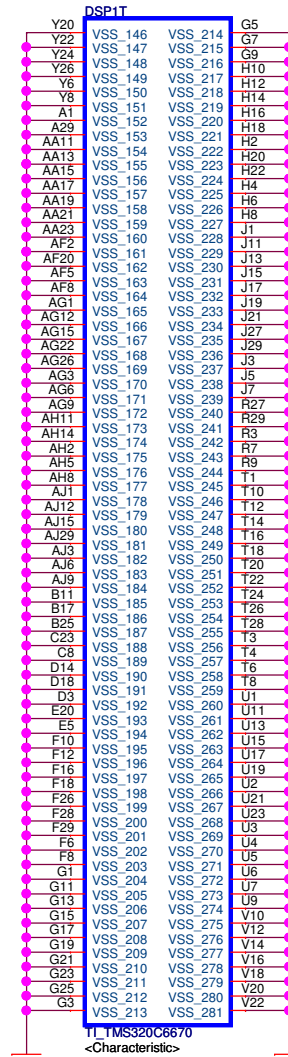
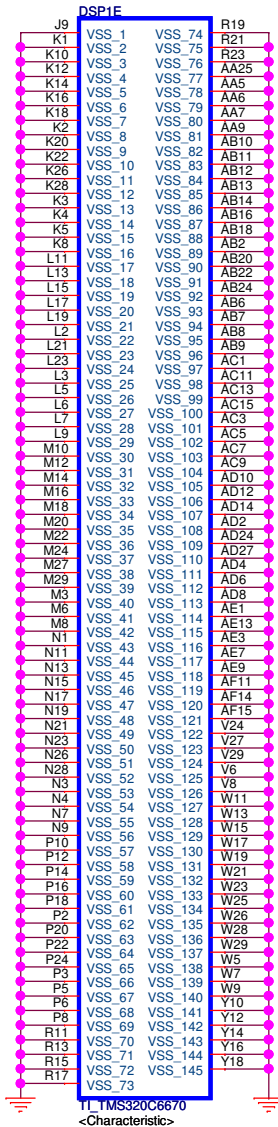


1.0V Serdes



Place near to DSP





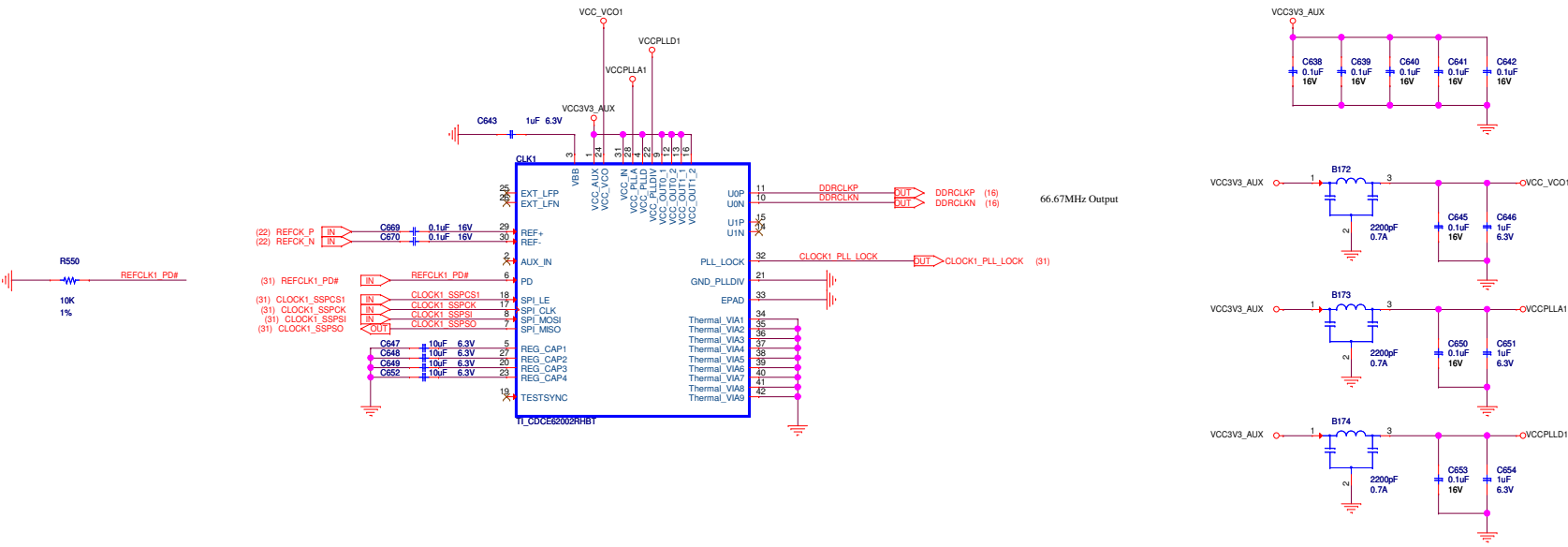
Designed for TI by ADVANTECH

TEXAS INSTRUMENTS ADVANTECH

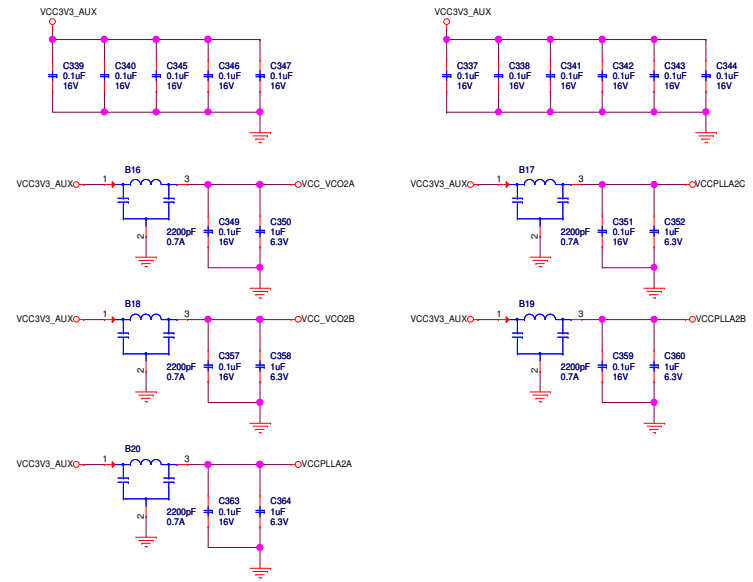
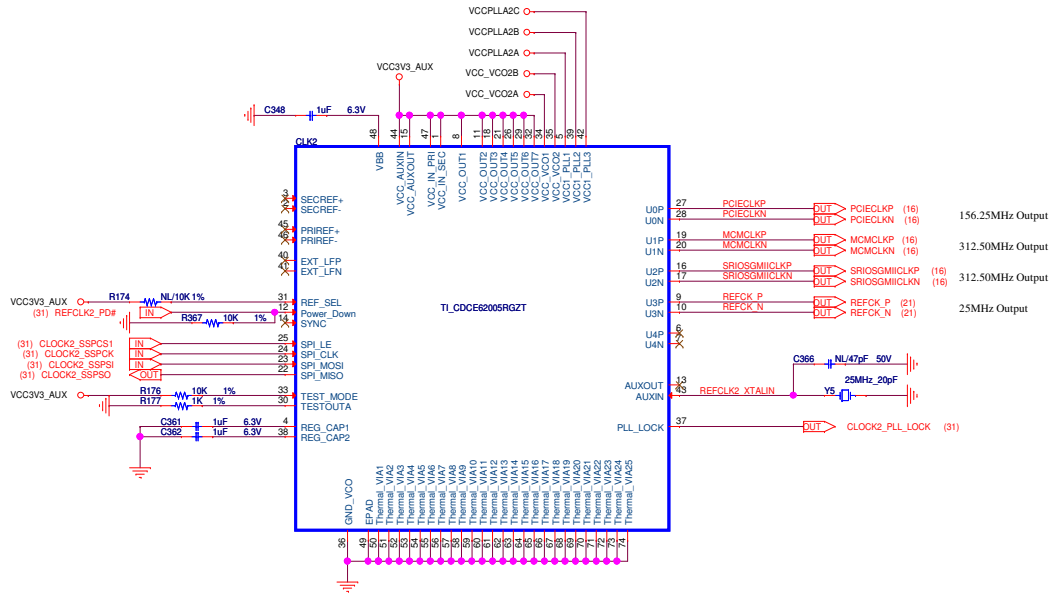
Title: **DSP_GND**

Size B	Document Number DSPM-8302E	Rev A101-1
Date: Wednesday, March 16, 2011	Sheet 20	of 36

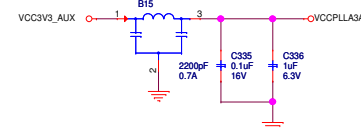
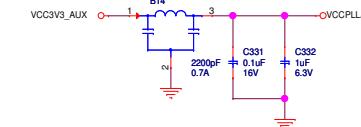
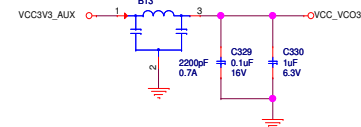
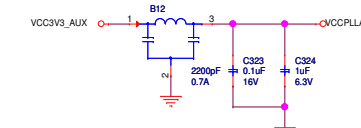
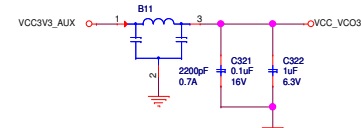
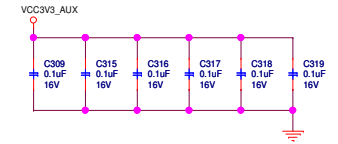
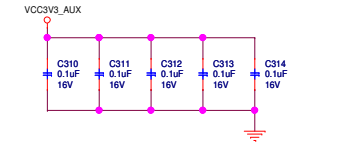
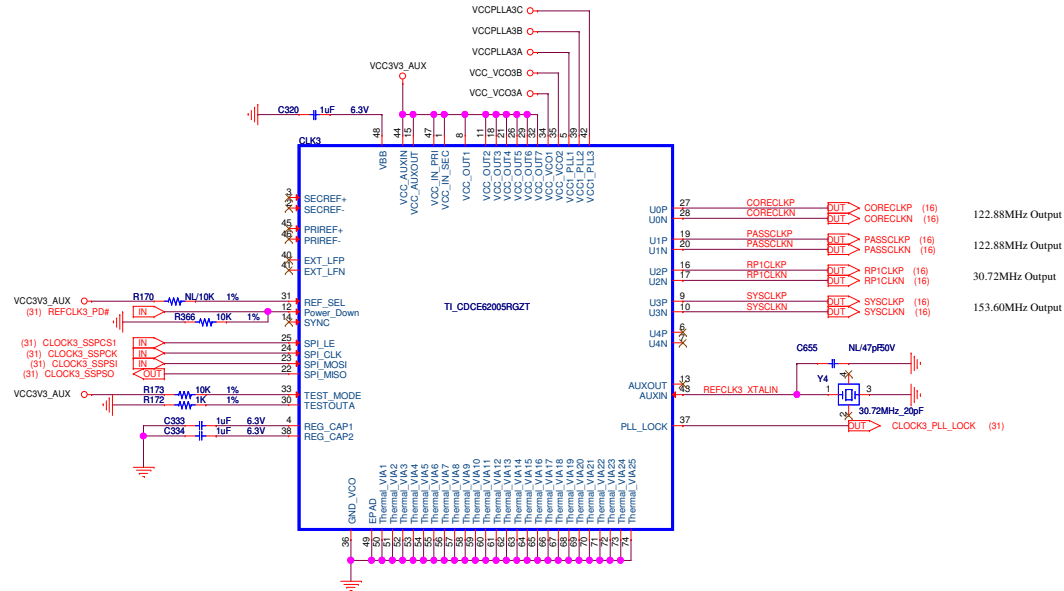
CLOCK GEN1 (DDR3)

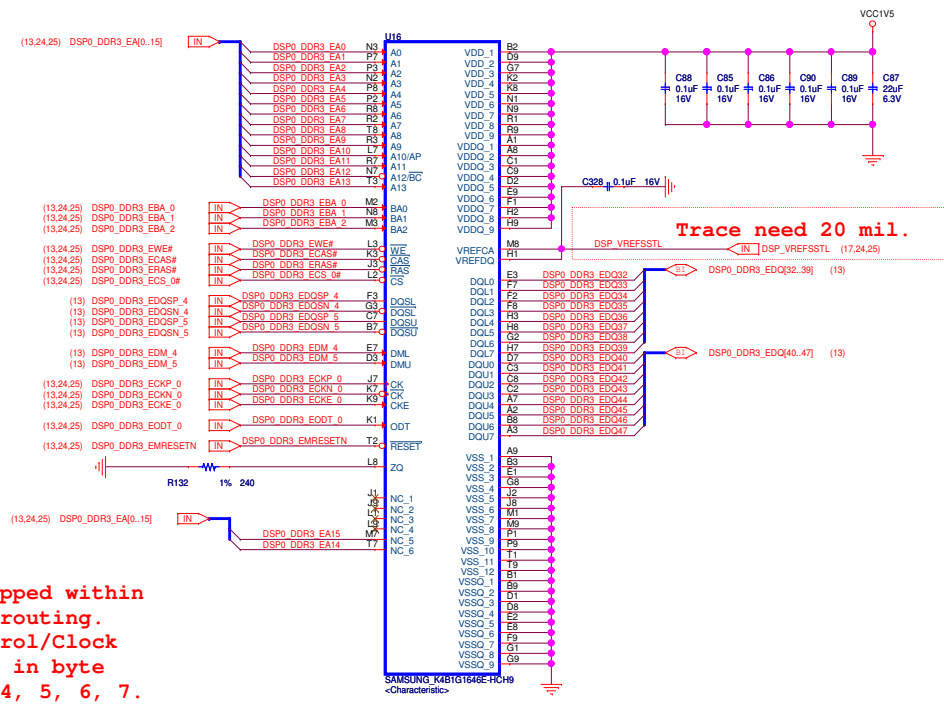
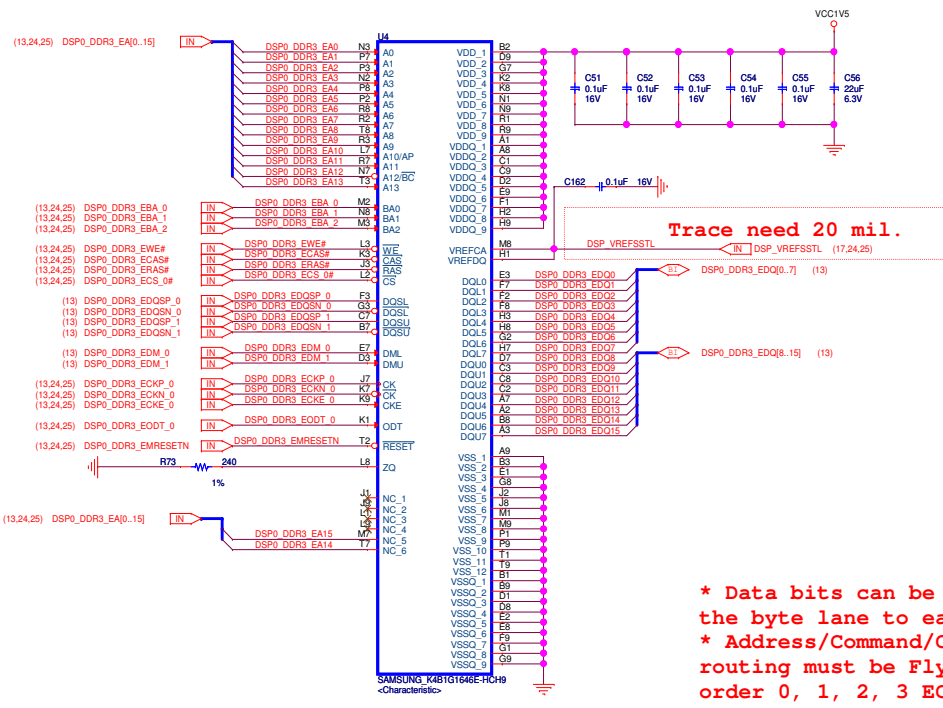


CLOCK GEN2

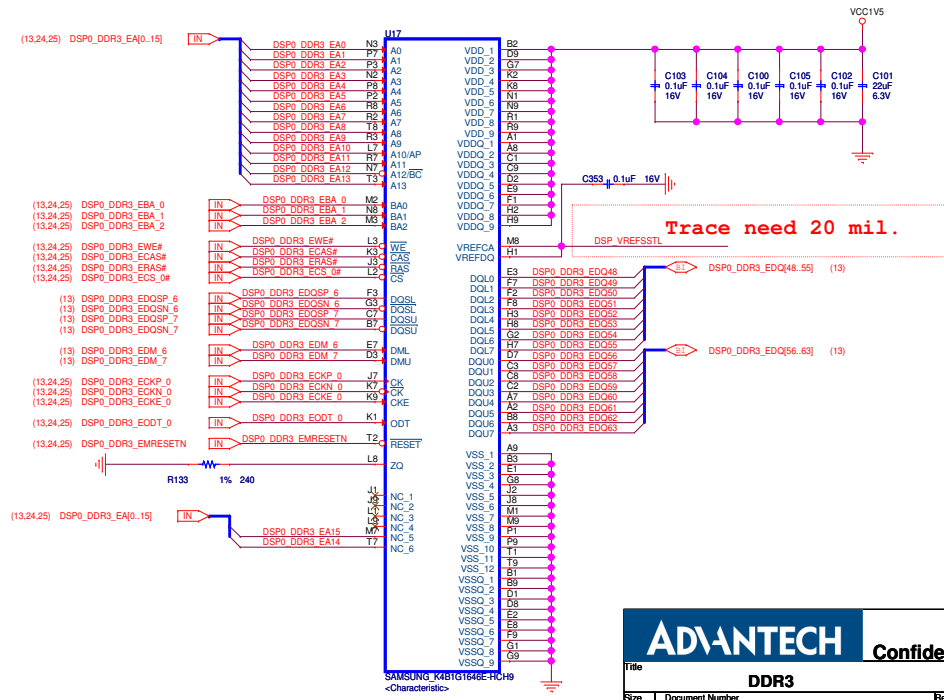
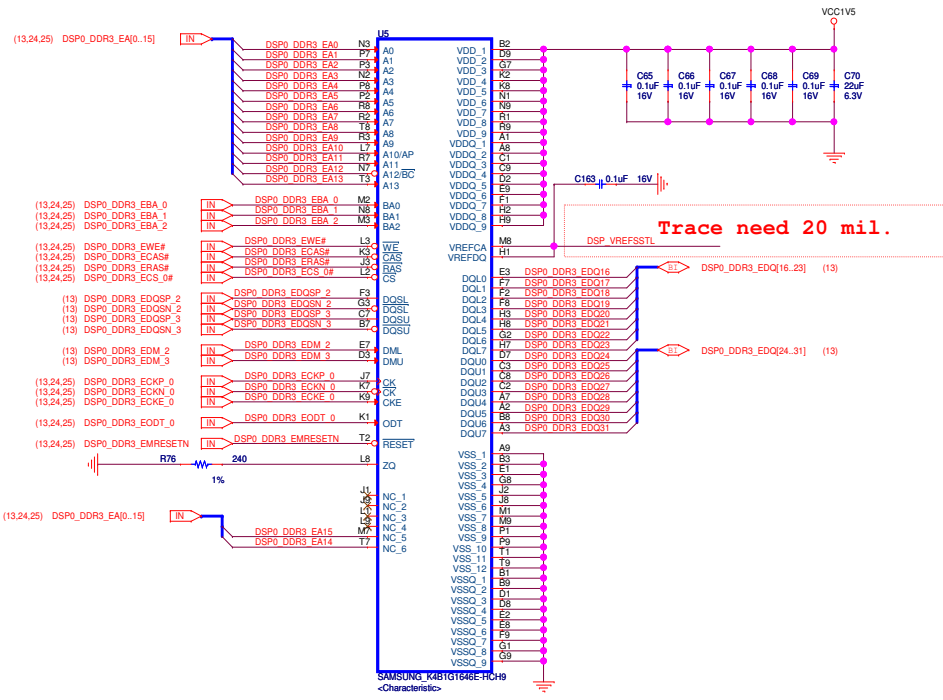


CLOCK GEN3

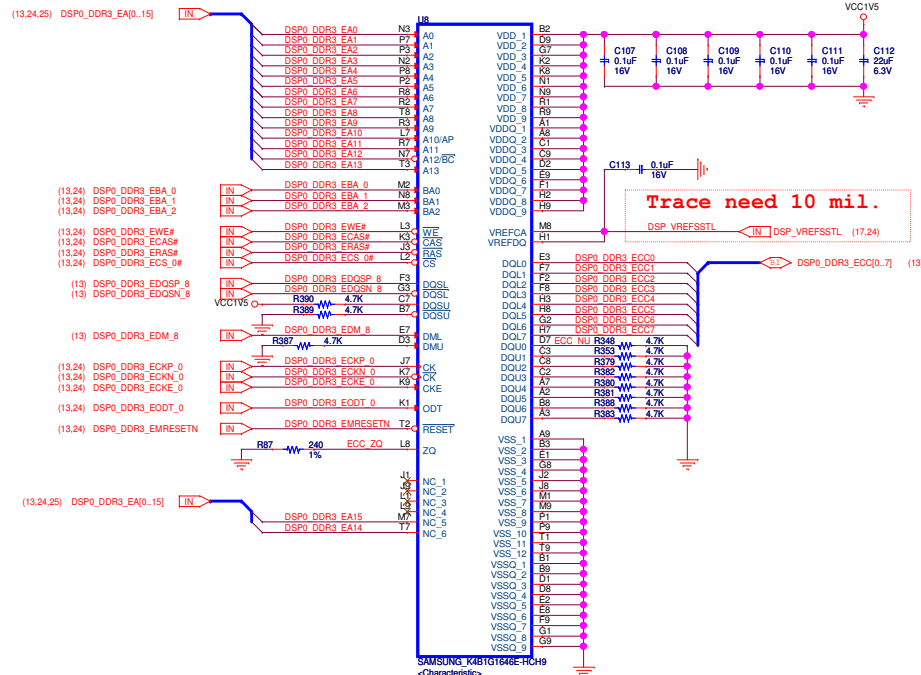
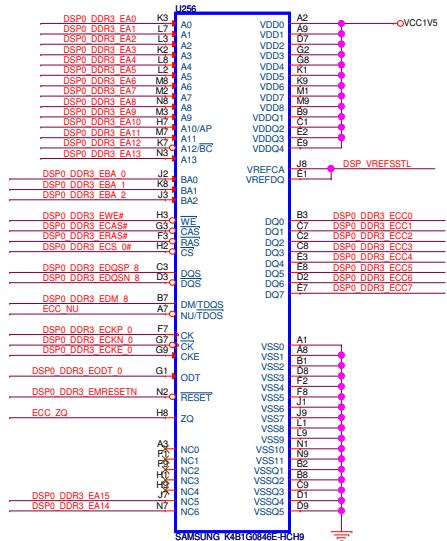


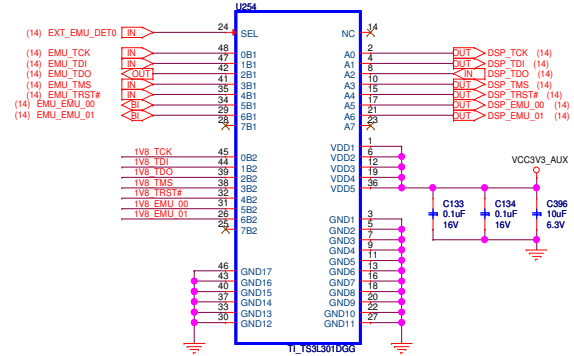
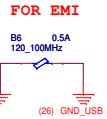
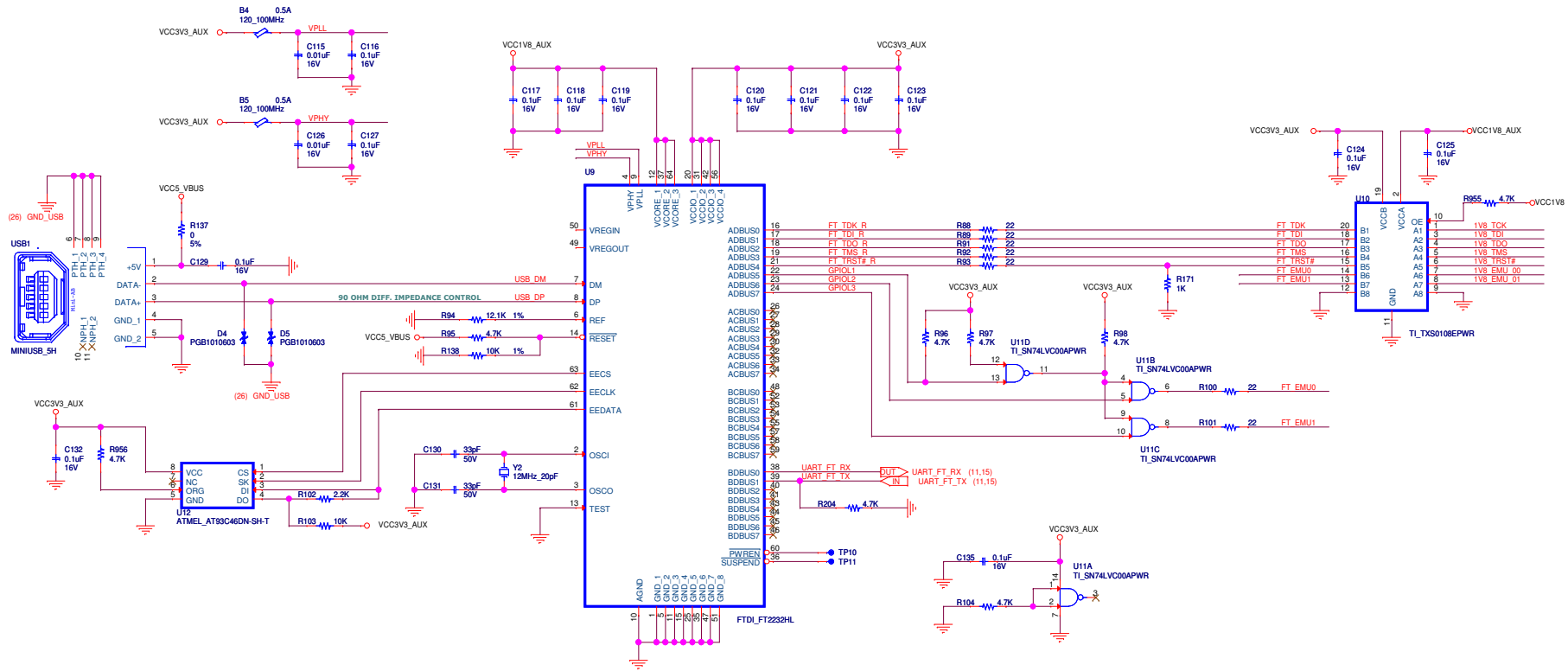


* Data bits can be swapped within the byte lane to ease routing.
 * Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.

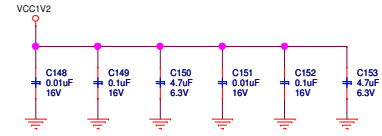
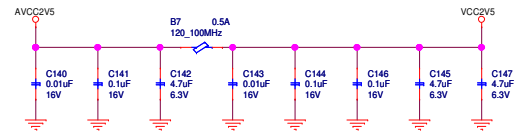
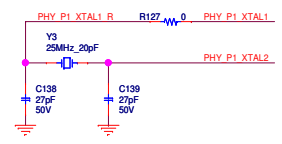
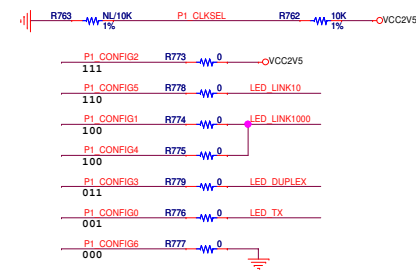
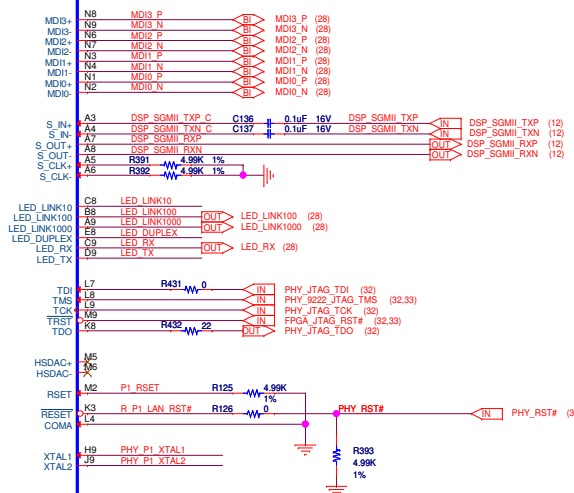
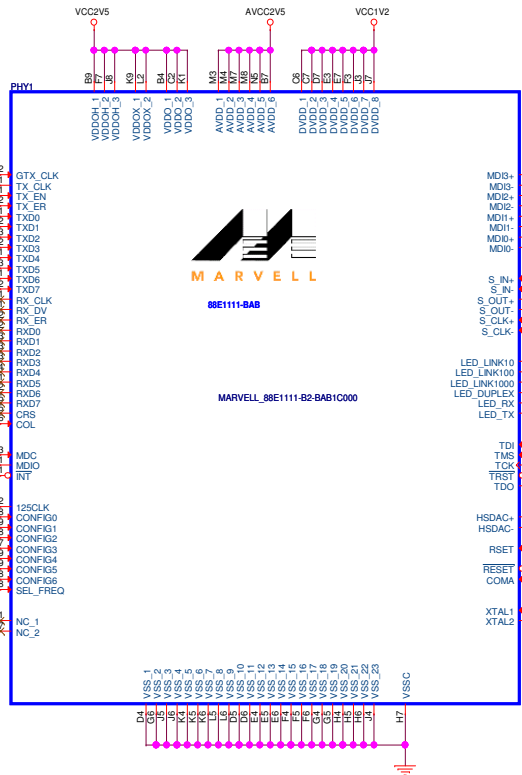


CO-LAYOUT





Switch for JTAG emulation
 EXT_EMU_DET = 0 --> External / Mezzanine Emulator
 EXT_EMU_DET = 1 --> On board emulation



88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

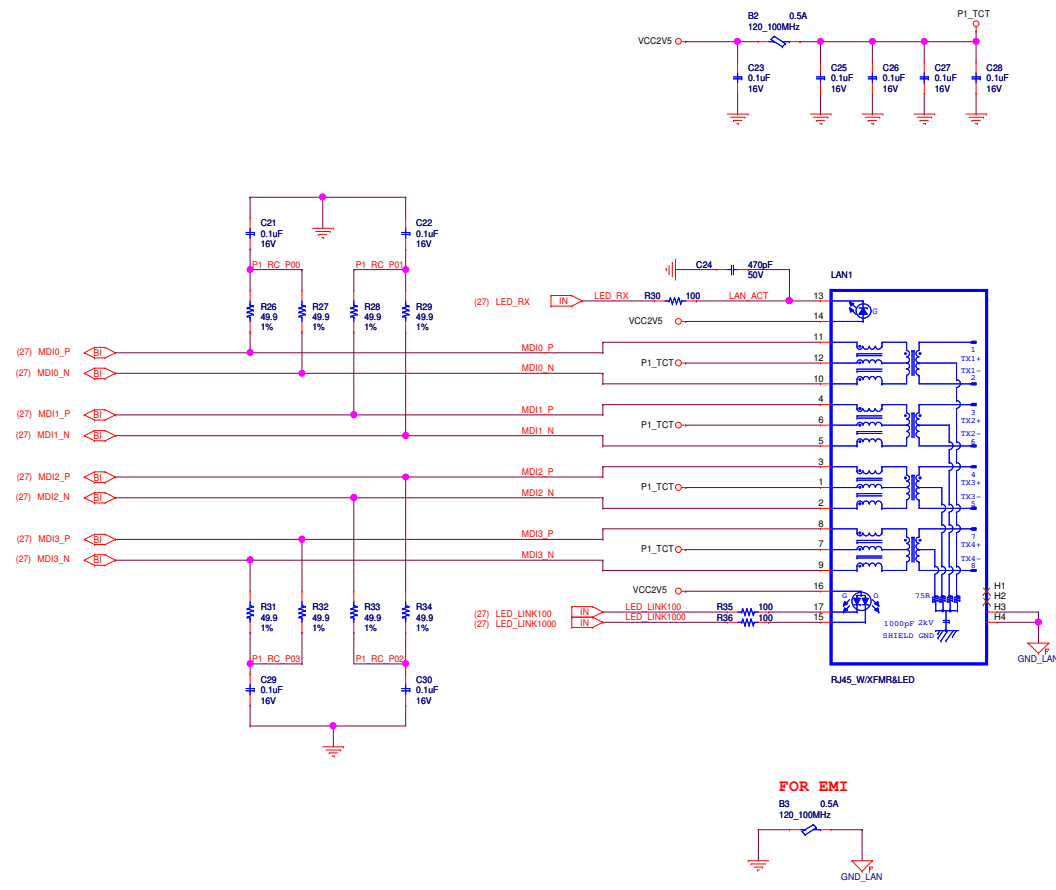
Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

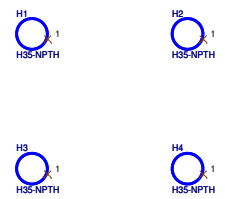
Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

PHY Address = 0x01

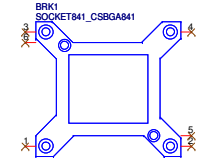
RJ45



Heatsink Holes

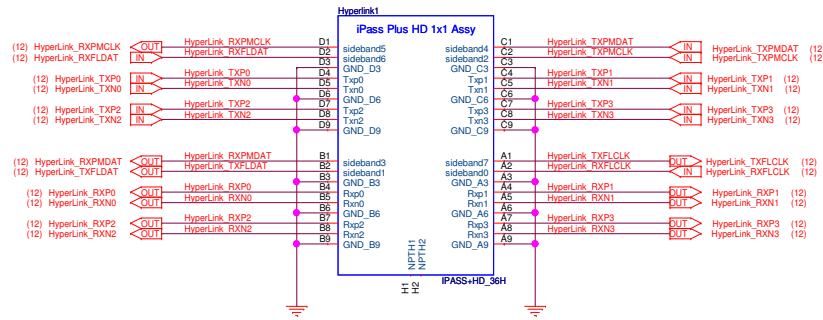


On board



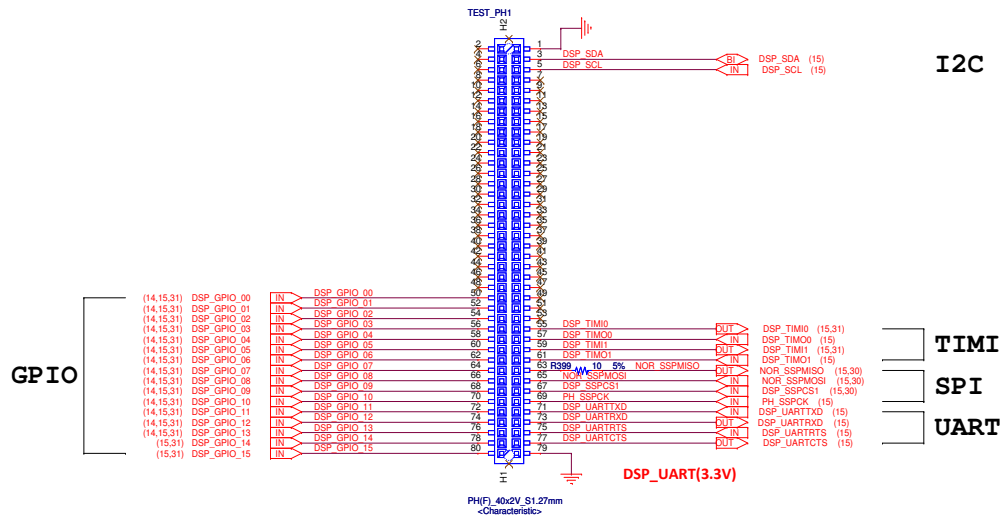
(Bottom Side 3mm) Placed Capacitors

IPASS+HD for HyperLink Bus connection



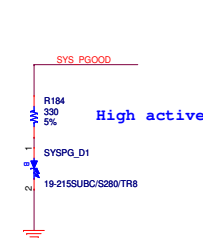
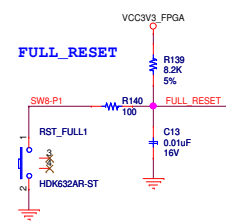
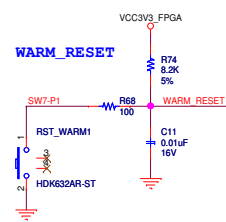
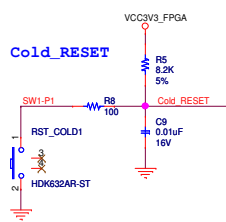
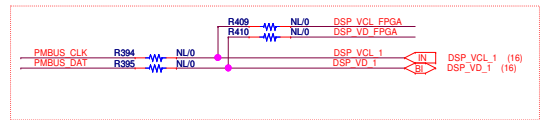
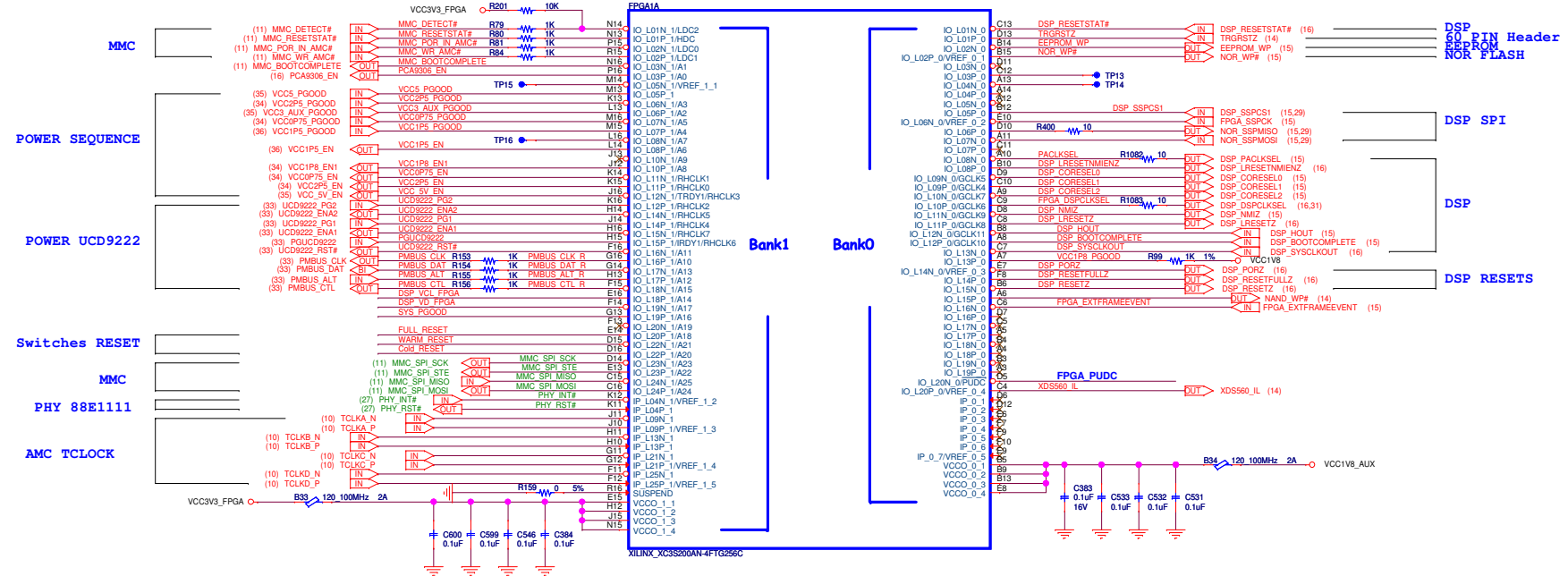
Pin Header for debug

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

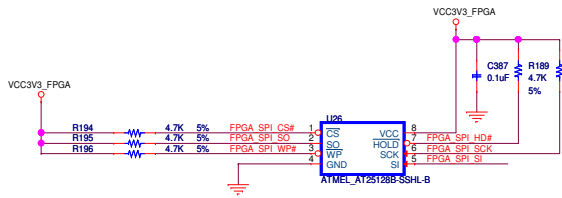


TCLKA_P	R228	100	TCLKA_N
TCLKB_P	R237	100	TCLKB_N
TCLKC_P	R318	100	TCLKC_N
TCLKD_P	R319	100	TCLKD_N

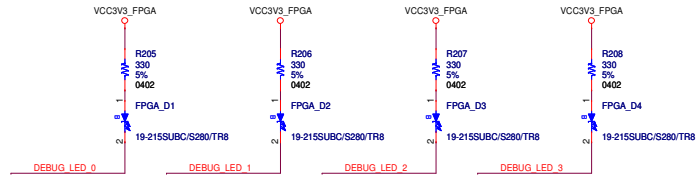
Place near to FPGA



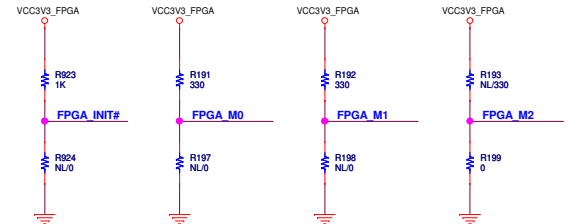
PUDC:
User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCCO input.
0: Pull-ups during configuration
1: No pull-ups



SPI EEPROM

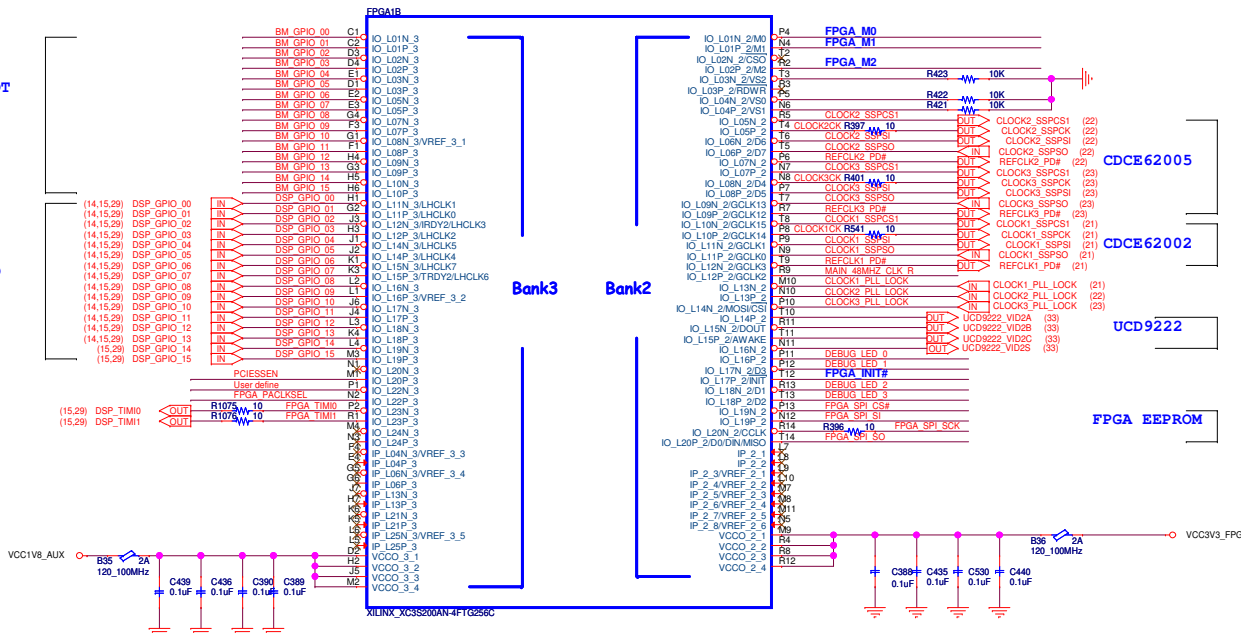


DEBUG_LED



For BOOT MODE SWITCH

DSP GPIO TO FPGA



Boot Device

BM_GPIO	BOOT Device	NOTE
3 2 1	Device	
0 0 0	NA	
0 0 1	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCIe	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

Device Configuration

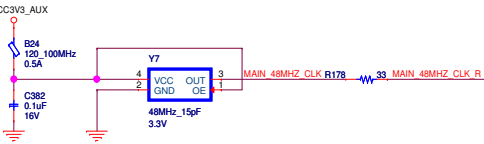
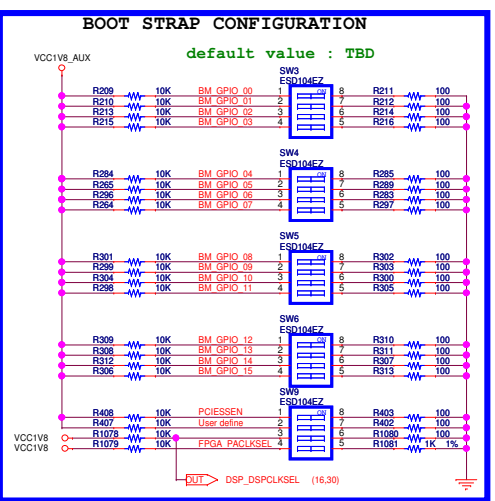
BM_GPIO [10:4]	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.

PLL Settings

BM_GPIO	INPUT	CorePac System PLL Configuration
13 12 11	CLK (MHz)	
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function
			Pull Up Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex



PCIENSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIe subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIe subsystem is enabled

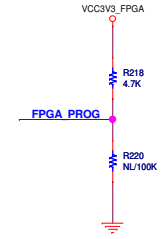
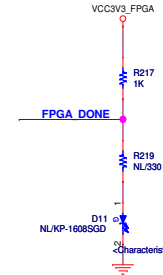
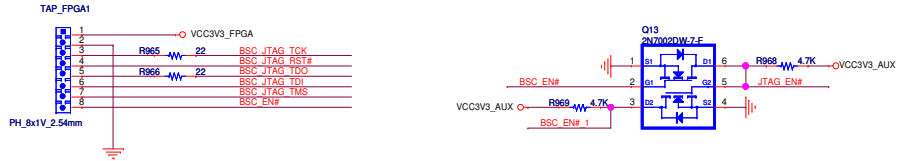
PCIe Mode selection (PCIESSMODE[1:0])

BM_GPIO[15:14] INPUT	Description
00b	PCIe in End-point mode
01b	PCIe in Legacy End-point mode(no support for MSI)
10b	PCIe in Legacy Root complex mode

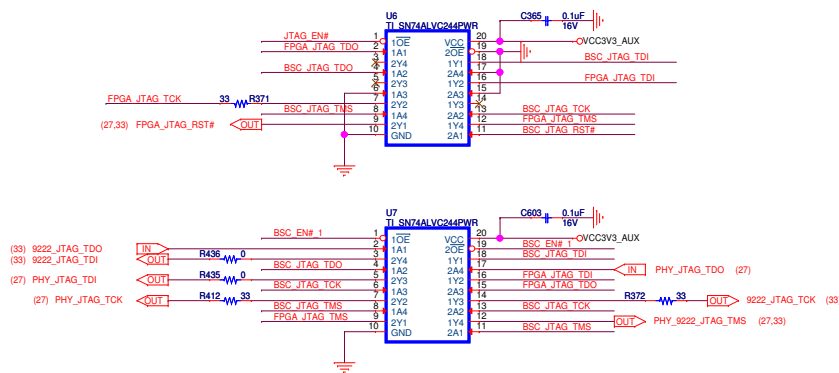
CLK Mode

Clock	Input	Description
Default_Down	DSP_DSPCLKSEL = 0	SYSClk used to clock the core PLL.
Default_Down	DSP_DSPCLKSEL = 1	ALTCORECLK is used to clock the core PLL
	FPGA_PACKKSEL = 0	PASSCLK is not used and should be tied to a static state.
	FPGA_PACKKSEL = 1	PASSCLK is used as a source for the PA_SS PLL. It must be present before the PA_SS PLL is removed from reset and programmed

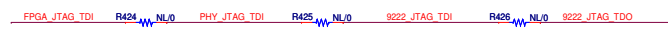
FPGA JTAG



During Configuration :
Must be High to allow
configuration to start.



For boundary scan by pass test



Always enabling :

BSC_JTAG_RST# --> FPGA_JTAG_RST#.
BSC_JTAG_TCK --> FPGA_JTAG_TCK

When BSC_EN# = 1:

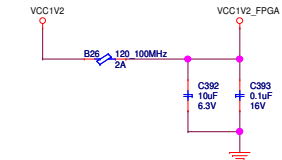
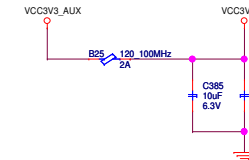
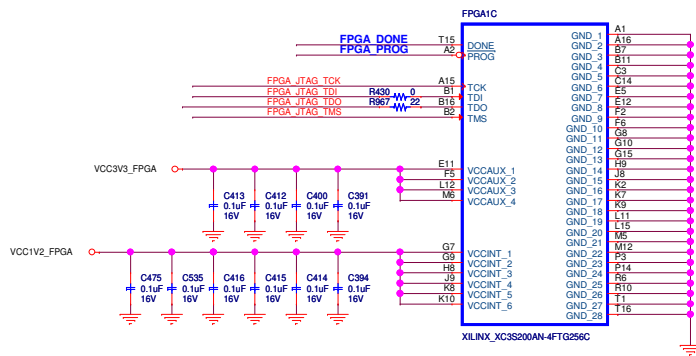
JTAG port (CN10) is only for FPGA debug
and programming.

BSC_JTAG_TDO --> FPGA_JTAG_TDI
BSC_JTAG_TDI <-- FPGA_JTAG_TDO
BSC_JTAG_TMS --> FPGA_JTAG_TMS

When BSC_EN# = 0:

JTAG port (CN10) is a boundary scan feature.
The sequence is FPGA, 88E1111, then UCD9222.

BSC_JTAG_TCK --> FPGA_JTAG_TCK
BSC_JTAG_TCK --> 9222_JTAG_TCK
BSC_JTAG_TMS --> PHY_9222_JTAG_TMS
BSC_JTAG_TCK --> PHY_JTAG_TCK
BSC_JTAG_TDO --> FPGA_JTAG_TDI
PHY_JTAG_TDO --> 9222_JTAG_TDI
9222_JTAG_TDO --> BSC_JTAG_TDI

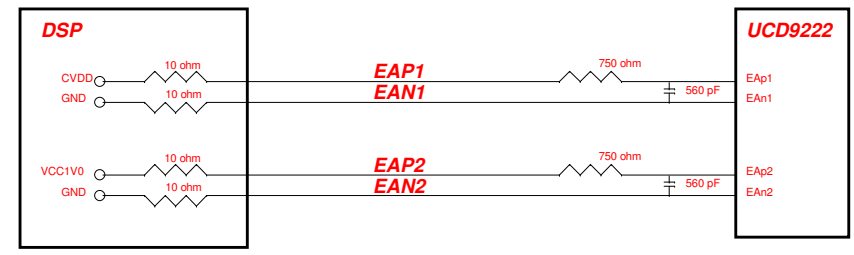
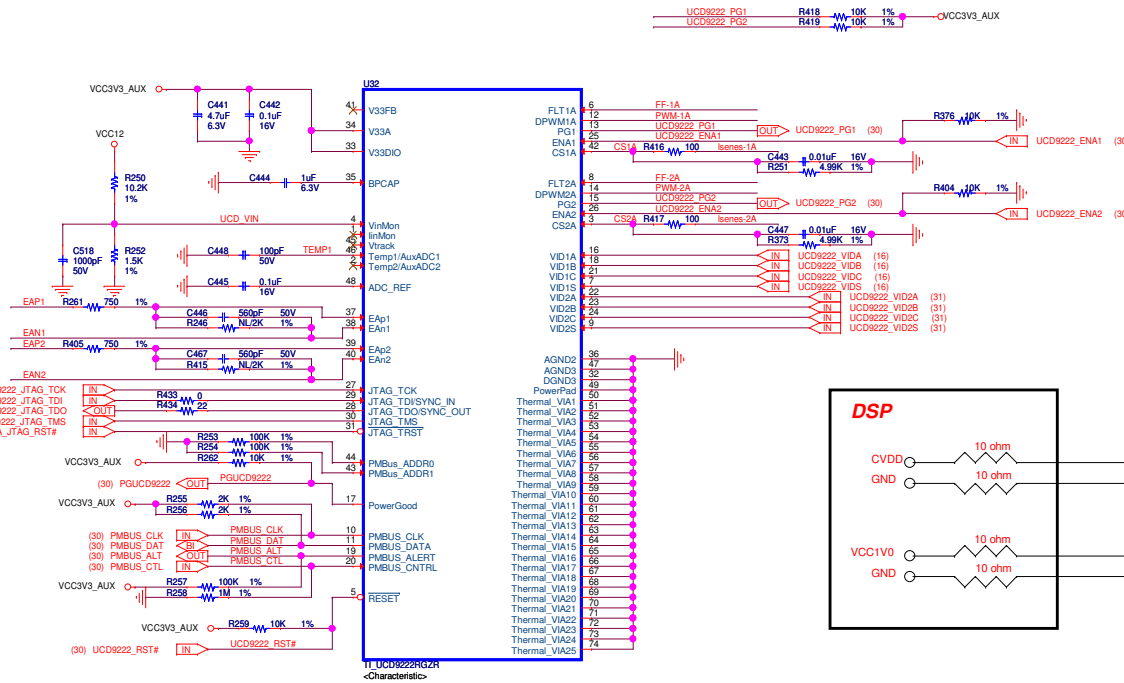
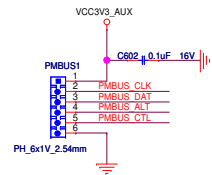


CVDD

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

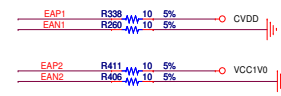
PMBUS Address
=>78 (6*12+6)
=> 0x4Eh



The design contains two 22uF input capacitors for the UCD7242 (one for each half bridge driver).
The placement of these capacitors is the most critical aspect of the layout.
Each cap needs to be tightly coupled to Vin and PGND of the UCD7242.

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.



+++output capacitor Calculation for VCC1V0+++

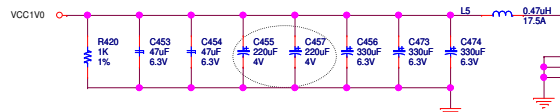
$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

$$C = 3.93 / (10m \times 8 \times 750k)$$

$$C = 65.5 \mu F$$

1.0V@ 3.93A



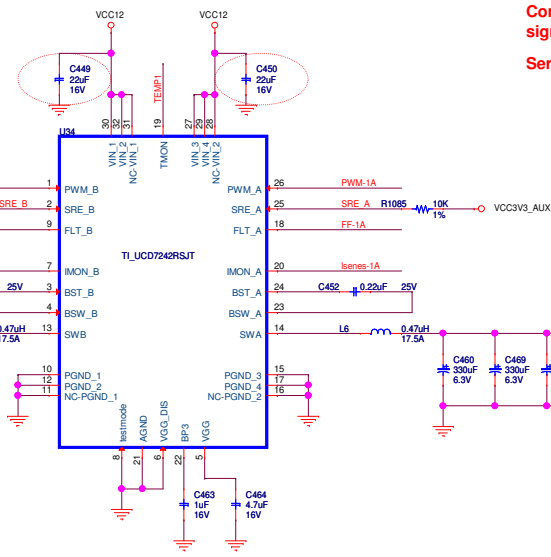
+++Inductor Calculation for VCC1V0+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f_s}$$

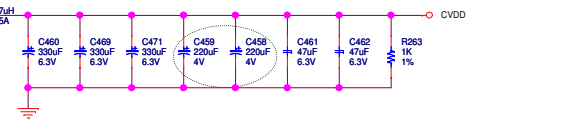
$$L = (12 - 1) / 3.93 \times (1/12) / 750K$$

$$L = (11 / 3.93) \times (0.083 / 750K)$$

$$L = 0.308 \mu H$$



DSP Vcore @6.68A



+++Inductor Calculation for CVDD+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f_s}$$

$$L = (12 - 1) / (6.68) \times (1/12) / 750K$$

$$L = (11 / 6.68) \times (0.083 / 750K)$$

$$L = 0.182 \mu H$$

+++output capacitor Calculation for VCC1V0+++

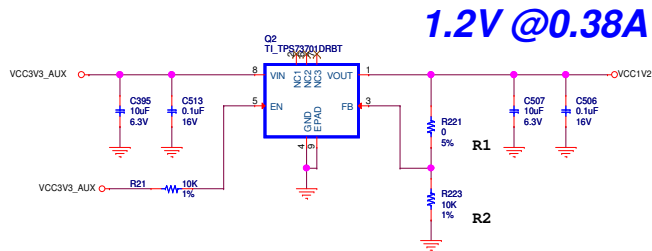
$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

$$C = 6.68 / (10m \times 8 \times 750k)$$

$$C = 111.3 \mu F$$

VCC1V2

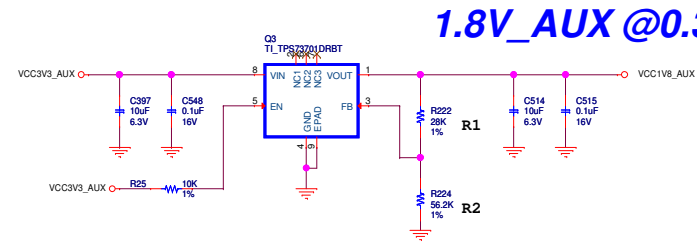


1.2V @0.38A

$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.204V = (0+10k) / 10k * 1.204$$

VCC1V8_AUX

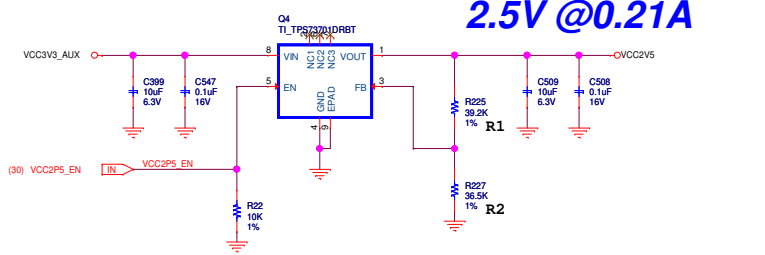


1.8V_AUX @0.3A

$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.805V = (28k+56.2k) / 56.2k * 1.205$$

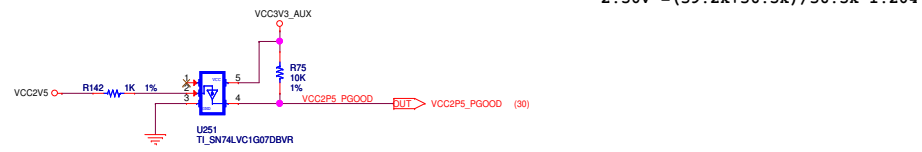
VCC2V5



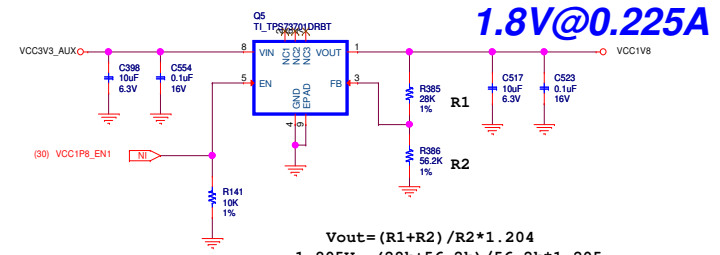
2.5V @0.21A

$$V_{out} = (R1+R2) / R2 * 1.204$$

$$2.50V = (39.2k+36.5k) / 36.5k * 1.204$$



VCC1V8

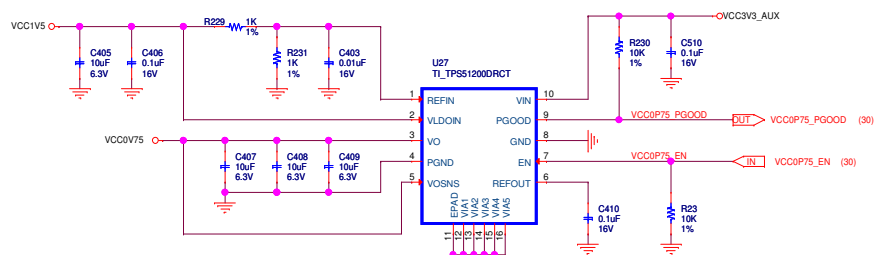


1.8V@0.225A

$$V_{out} = (R1+R2) / R2 * 1.204$$

$$1.805V = (28k+56.2k) / 56.2k * 1.205$$

VCC0V75



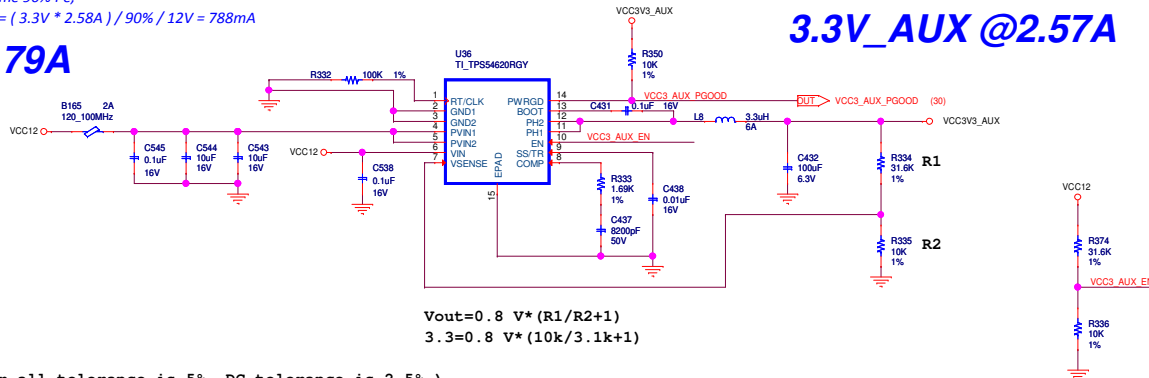
0.75V @0.25A

VCC3V3_AUX

Assume 90% Pe,
 $I_{in} = (3.3V * 2.58A) / 90\% / 12V = 788mA$

12V@0.79A

3.3V_AUX @2.57A



$$V_{out} = 0.8 V * (R1/R2+1)$$

$$3.3 = 0.8 V * (10k/3.1k+1)$$

(Over all tolerance is 5% ,DC tolerance is 2.5%)

+++output capacitor Calculation+++

$$C_{out} = (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$$

$$C_{out} = (2 * 2.57) / (1MHz * 0.0825)$$

$$C_{out} = (5.16) / (82500)$$

$$C_{out} = 62\mu F$$

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)

$$L = ((V_{in(max)} - V_{out}) / I_{out} * Kind) * (V_{out} / (V_{in(max)} * F_{sw}))$$

$$L = ((12.6 - 3.3) / 2.57 * Kind) * (3.3 / (12.7 * 1MHz))$$

$$L = (9.3 / 2.57 * 0.3) * (3.3 / (12.7M))$$

$$L = (9.3 / 0.771) * (0.26M)$$

$$L = 3.13\mu H$$

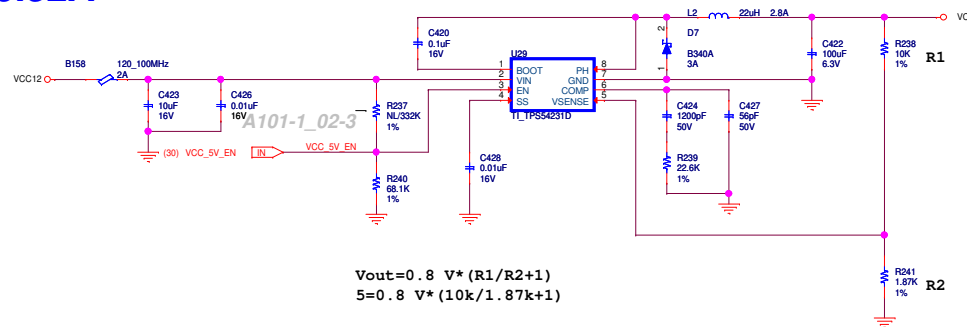
Reference Inductor 3.3uH

VCC5

Assume 80% Pe,
 $I_{in} = (5V * 1A) / 80\% / 12V = 520mA$

12V@0.52A

5V @1A



$$V_{out} = 0.8 V * (R1/R2+1)$$

$$5 = 0.8 V * (10k/1.87k+1)$$

+++output capacitor Calculation+++

$$C_{o_min} = 1 / (2 * \pi * R_o * F_{CO_max})$$

$$C_{out} = 1 / (2 * 3.14 * 5 * 25K)$$

$$C_{out} = 1.3 \mu F$$

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)

$$L = ((V_{in(max)} - V_{out}) / I_{out} * Kind) * (V_{out} / (V_{in(max)} * F_{sw}))$$

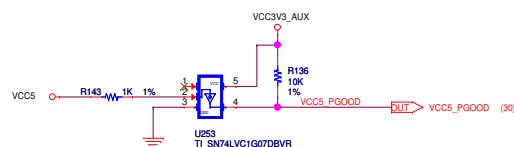
$$L = ((12.6 - 5) / 1 * Kind) * (5 / (12.7 * 570K))$$

$$L = ((7.6 / 0.3) * 0.3) * (5 / (7239K))$$

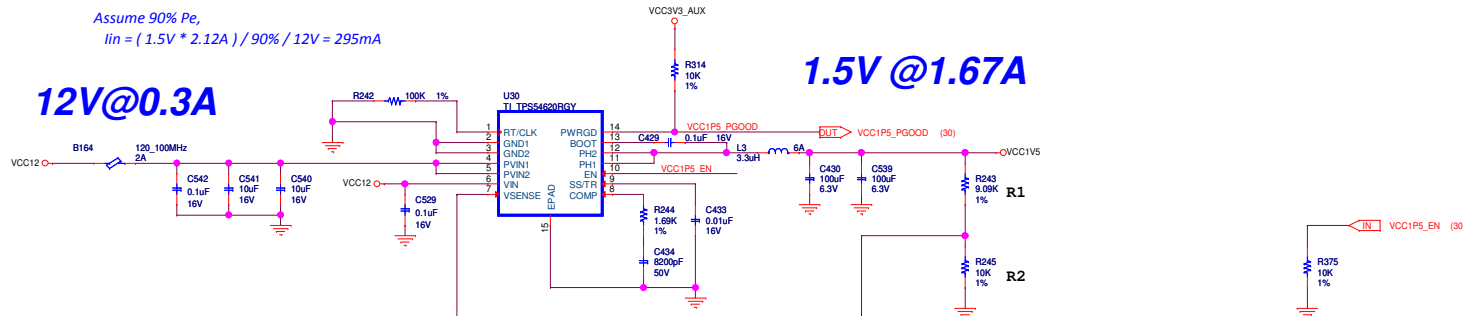
$$L = (25.3) * (0.69M)$$

$$L = 17.5\mu H$$

Reference Inductor 22uH



VCC1V5



$$V_{out} = 0.8 V * (R1/R2 + 1)$$

$$1.52 = 0.8 V * (9.09k/10k + 1)$$

(Over all tolerance is 5% ,DC tolerance is 2.5%)

+++output capacitor Calculation+++
 $C_{out} = (2 * \Delta I_{out}) / (F_{sw} * \Delta V_{out})$
 $C_{out} = (2 * 1.67) / (1MHz * 0.0375)$
 $C_{out} = (3.34) / (37500)$
 $C_{out} = 89uF$
Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
 $L = ((V_{in(max)} - V_{out}) / I_{out} * Kind) * (V_{out} / (V_{in(max)} * F_{sw}))$
 $L = ((12.6 - 1.5) / 1.67 * 0.3) * (1.5 / (12.7M))$
 $L = (11.1 / 1.67 * 0.3) * (1.5 / (12.7M))$
 $L = (11.1 / 0.501) * (0.12M)$
 $L = 2.65uH$
Reference Inductor 3.3uH