A Keystone 2 EVM Board for TI

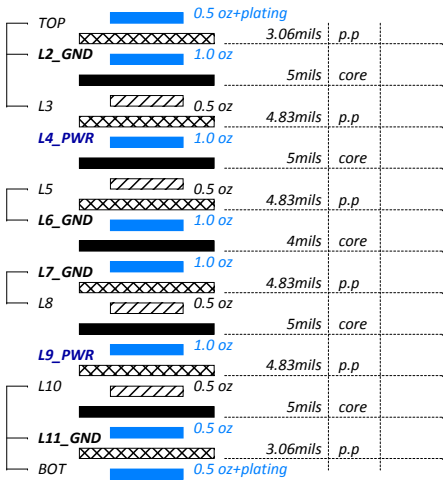
Product name : K2EVM-HK

Rev. 2.0

PCB PN :

Project Code :

PCB Thickness : 63 mils(1.6mm)
12 Layers



DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY , PLEASE REFER TO THE DEVICE DATA MANUAL.

Copyright (C) 2013 Texas Instruments Incorporated.
All rights reserved.

NOTE: TI Information – Selective Disclosure

NOTE: EVM design supports multiple devices. Check your device datasheet to determine if a given functionality is supported.

K2EVM-HK Revision Table

K2EVM-HK (Rev 103-1 / PCB- 19C2830502-01)

Item	Description	Page
1	Update Sequency for combining CVDD and CVDDT	Page. 6
2	Update POWER DISTRIBUTION for combining CVDD and CVDDT	Page. 7
3	R117, R468, R116 Change 10ohm to 0 ohm for version 1.2	Page.40,41
4	UU1 and U28 combining	Page.18
5	Add U62 and R802 for combining CVDD and CVDDT	Page.40
6	Change plane CVDDT to CVDD	Page.23
7	EXP_SCL2_3V3/EXP_SDA2_3V3 SWAP from U54	Page.18
8	EEPROM 512Kb change to 1Mb for Text correction Add NAND memory size 4Gb for Text correction Modify DDR3B 128*16 to 128/256*16 & 1GB to 1-2GB	Page.5
9	change R399/R400 from 4.7kohm to 220 ohm	Page.14
10	change R438/R439 from 4.7kohm to 220 ohm	Page.15
11	Change EMIF termination resistor to buffer for ESD/EMI Issue Change link NAND Flash Interface net name	Page.19
12	Add EMIF_DIR for EMIF Data control through buffer	Page.13
13	1.Remove Choke from B26 , Add AC CAP 0.1uf from C839/C840 for USB3.0 Superspeed Error 2.Connect the EN pin of the U59 to the USBDRVVBUS pin of the Kepler SoC through a R809 (10ohm) resistor (oThis USBDRVVBUS pin is used by the USB state-machine to control the VBUS supplied to the TypeA connector)	Page.15
14	1.Power rail net name change from VDDAHV to AVDDAHV 2.Power rail net name change from VDD0V85 to AVDDALV 3.Replace B46 and B43 with the Murata BLM18SG121TN	Page.23
15	Remove D13/D15 ESD Diode for avoid the snaking at the end of the routing as well.	Page.15
16	Add U67 Buffer for SOC_EMIFWAIT1	Page.19
17	Correction directional for SOC_EMIFWAIT1	Page.39
18	Add EMIF_OEz net from U50.21 for control Data R/W	Page.13
19	Add R811/R810 for select read/write control reserve	Page.19
20	Modify the stack-up changes from 4.34mils to 4.83 mils between L7 and L8	Page.1
21	Change the Values of 11 capacitors. The C617 , C600 , C675 , C697, C639 change to 1uf. The C649,C645,C575,C660,C651,C667 change to 47nf.	Page.23

Item	Description	Page

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title

K2EVM-HK Revision Table II

Size	Document Number	Rev
C	K2EVM-HK	A103

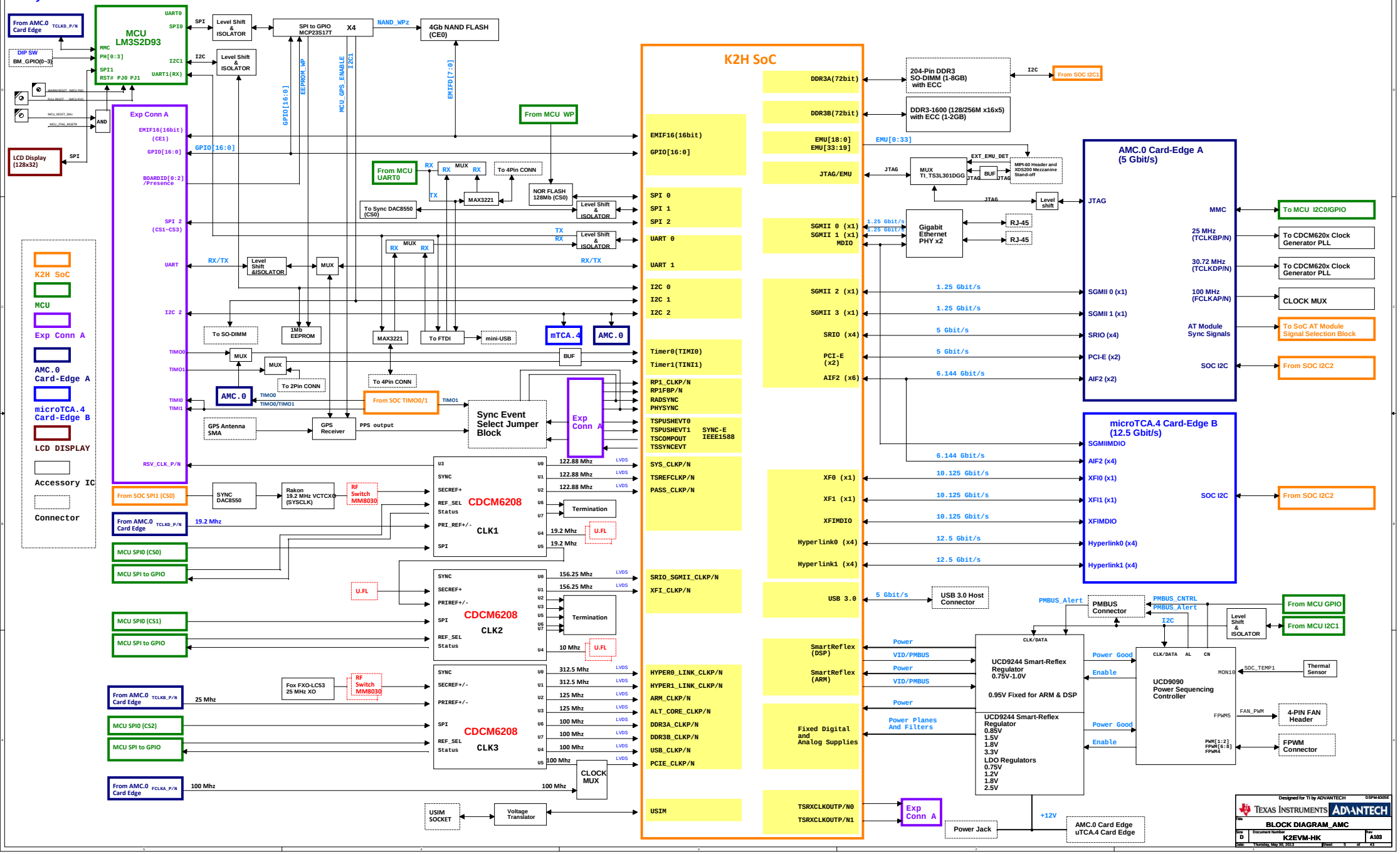
Date: Thursday, May 30, 2013 Sheet 3 of 43

TITLE & TABLE OF CONTENTS

Page	Description
01	COVER PAGE
02	K2EVM-HK Revision Table I
03	K2EVM-HK Revision Table II
04	TITLE & TABLE OF CONTENTS
05	BLOCK DIAGRAM_AMC
06	POWER SEQUENCE
07	POWER DISTRIBUTION
08	CLOCK & TIMER DIAGRAM
09	MCU_BLOCK_ Diagram
10	Intentionally Left Blank
11	K2EVM-HK EVM Placement
12	AMC GF
13	SPI to GPIO Converter
14	SOC_SRIO_SGMII_PCIE_MCM
15	SOC_XFI_USB
16	SOC_DDR3A
17	SOC_DDR3B
18	SOC_MISC
19	SOC_JTAG_EMU
20	SOC_AIF
21	SOC CLOCKs & Smart-Reflex VID
22	SOC_POWERA
23	SOC_POWERB
24	SOC_GND
25	CLOCK_GEN1
26	CLOCK_GEN2
27	CLOCK_GEN3
28	DDR3
29	DDR3_ECC
30	DDR3_SODIMM

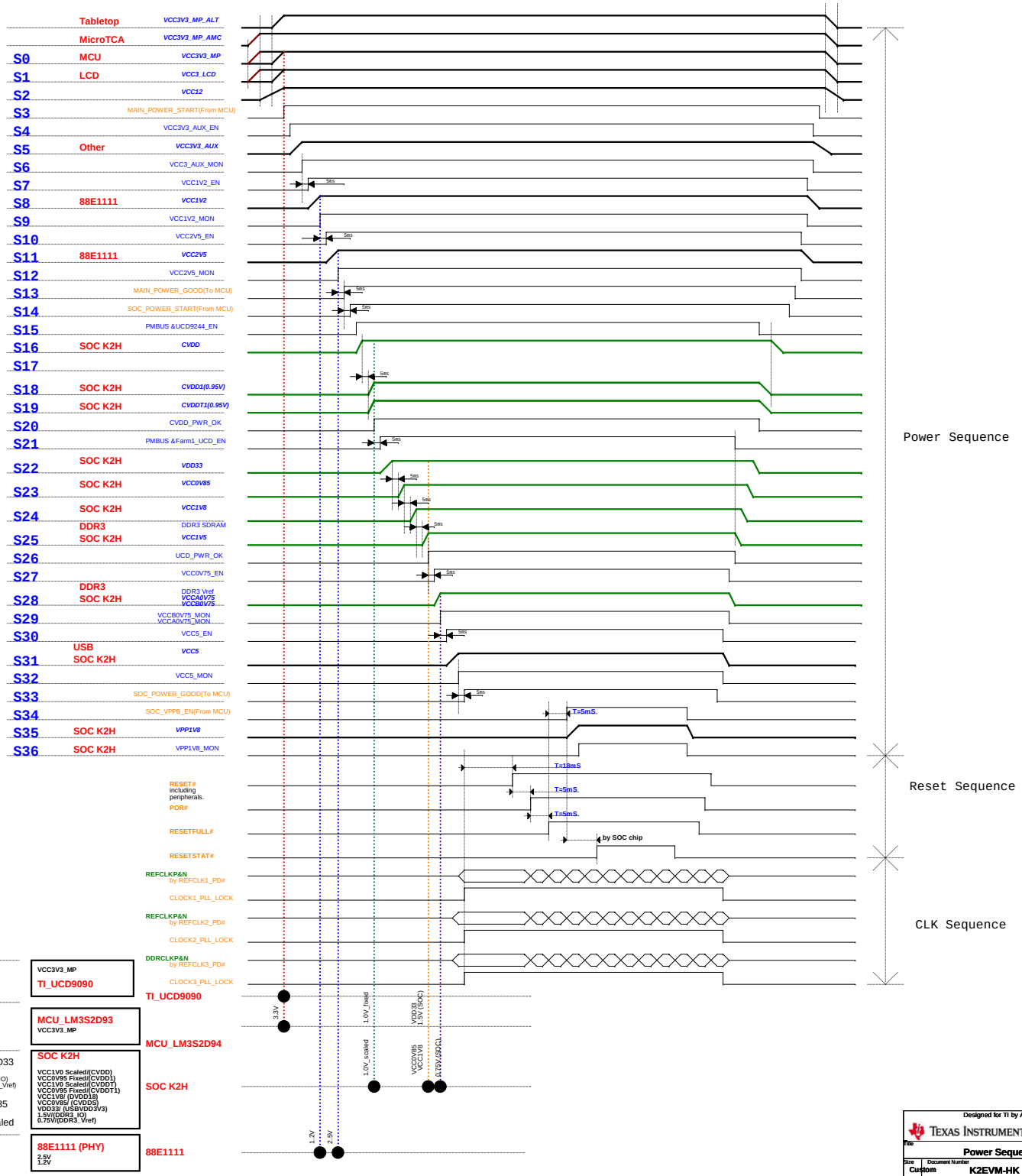
Page	Description
31	Connectors for Debug
32	GBE Ethernet PHY1
33	GBE Ethernet PHY2
34	88E1111 (RJ45)
35	GPS & SIM CARD
36	MCU_LM3S2D93
37	MCU_MISC
38	MCU LCD
39	mTCA_ZD3/120-pin Expansion
40	Smart-Reflex AVS
41	Smart_Reflex 1.8V/1.5V/0.85V
42	Power_1.2V/2.5V/0.75V/1.8V
43	Power_VCC5 / VCC3_AUX/MP_ALT

Keystone-2 EVM BLOCK DIAGRAM



Power Sequence

Has not been modify , wait TI provide document.

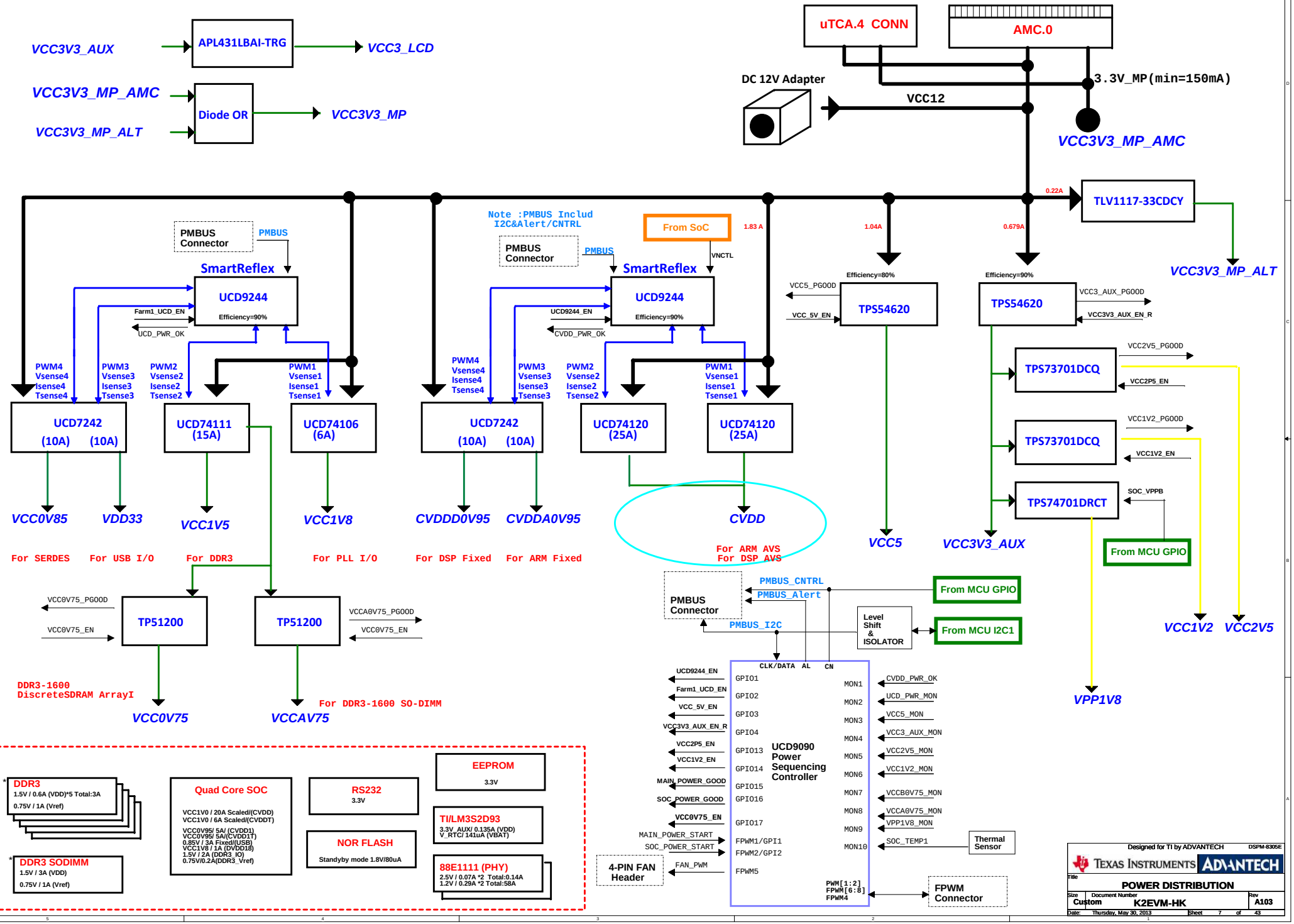


Designed for TI by ADVANTECH DSPM-8365E

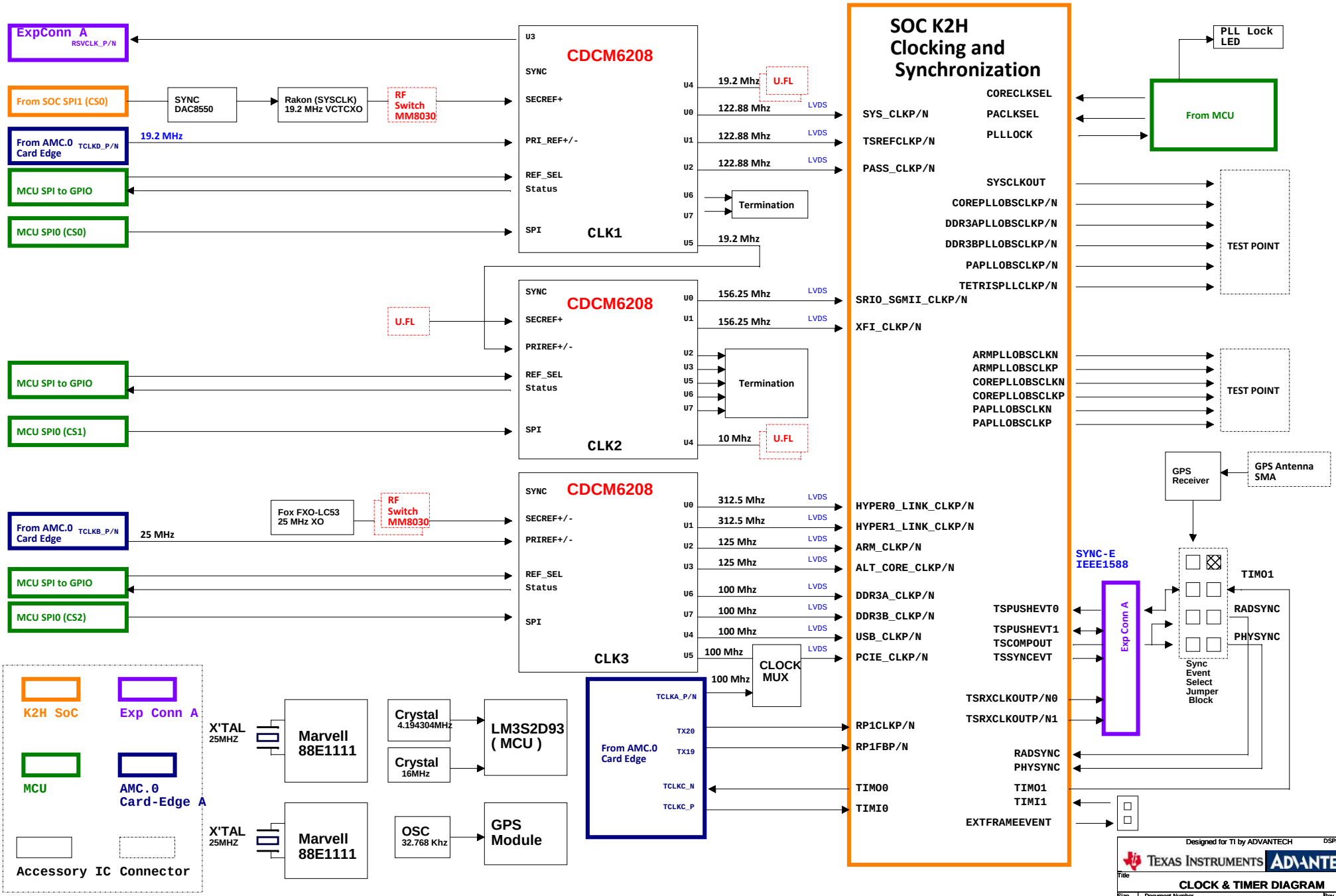
TEXAS INSTRUMENTS ADVANTECH

Title: Power Sequence		
Size: Custom	Document Number: K2EVM-HK	Rev: A103
Date: Thursday, May 30, 2013	Sheet 6 of 43	

POWER DISTRIBUTION



CLOCK & TIMER DIAGRAM



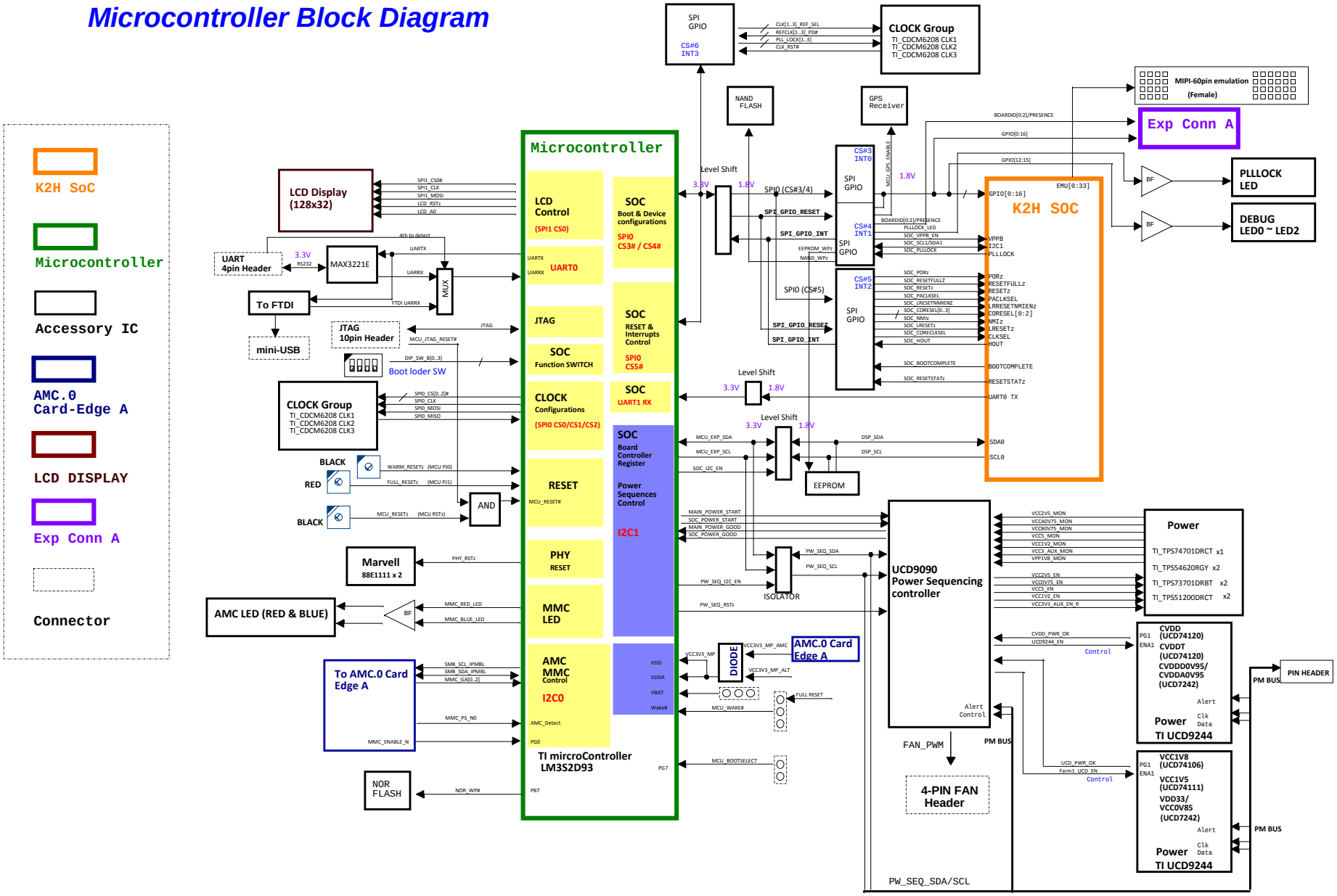
Designed for TI by ADVANTECH

DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title		
CLOCK & TIMER DIAGRAM		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 8 of 43	

Microcontroller Block Diagram



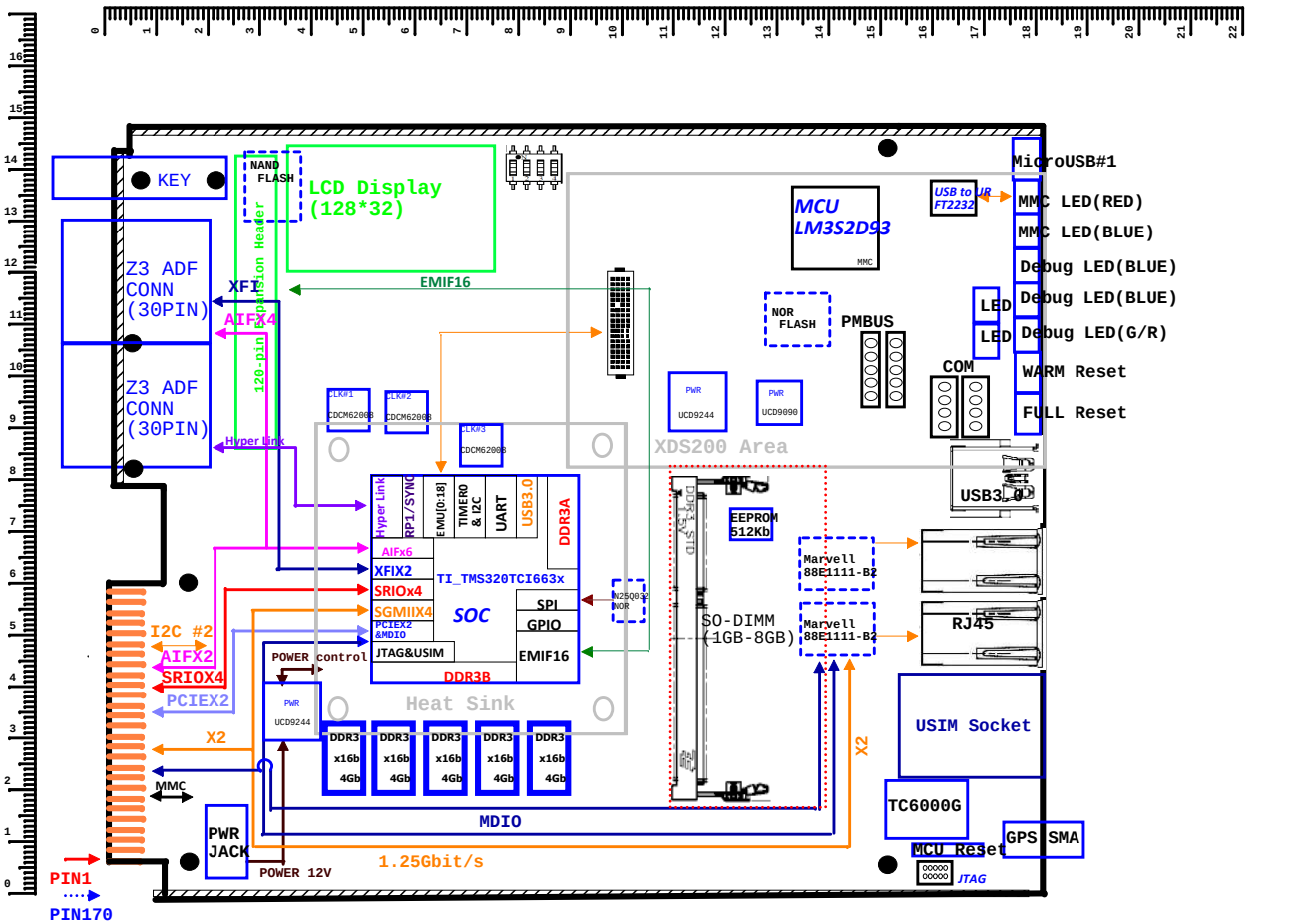
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title		
Microcontroller Block Diagram		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 9 of 43	

Intentionally Left Blank

K2EVM-HK EVM PLACEMENT (TOP SIDE)



PCB Half Length = 181.5x148.5mm

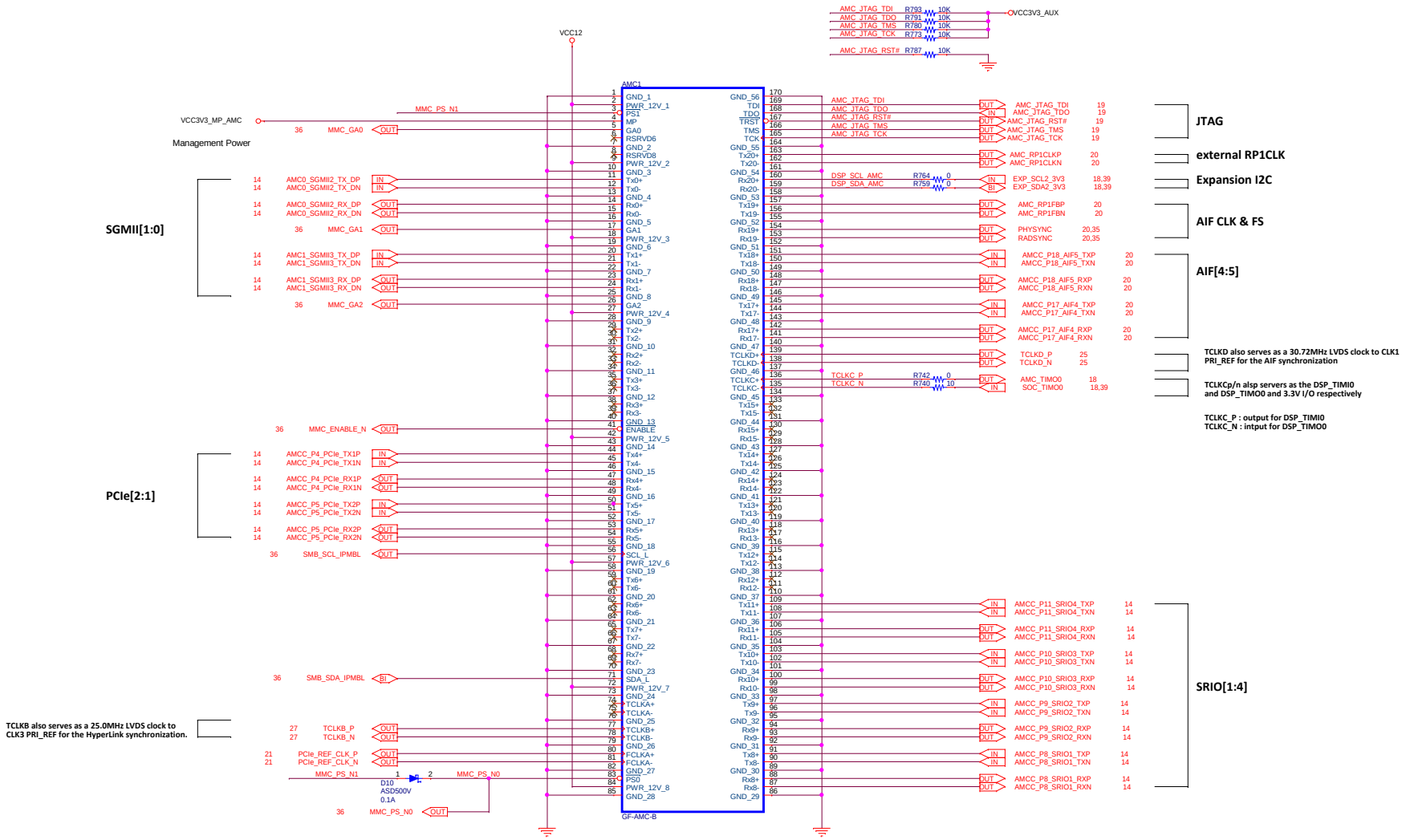
Note: Dotted line is Bottom SIDE Component

Note: EVM with K2H device does not support XGMII

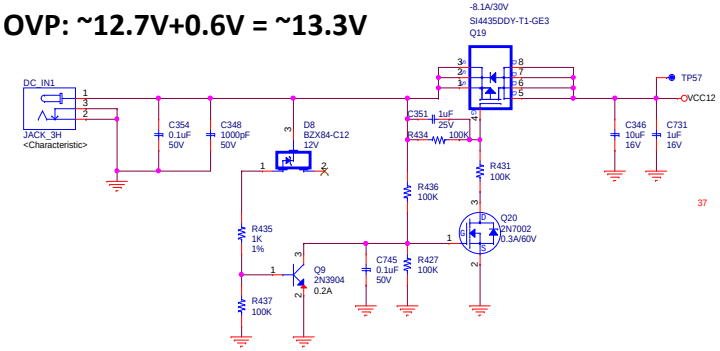
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

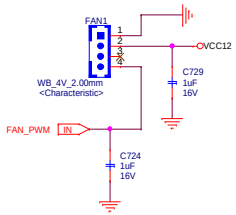
Title		
K2EVM-HK Placement		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 11 of 43	



OVP: ~12.7V+0.6V = ~13.3V



DC FAN Connector for SOC

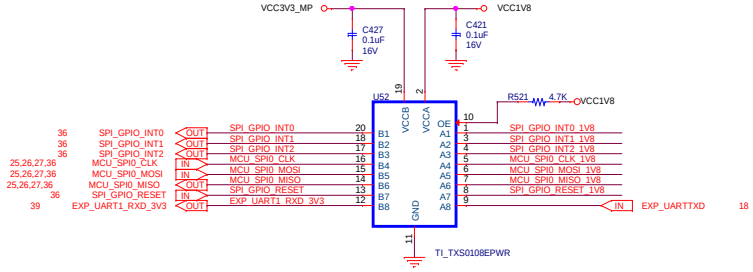


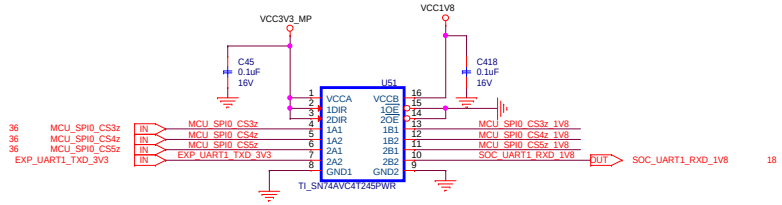
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

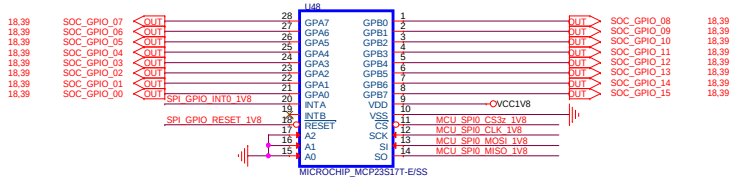
Title		
	AMC GF	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 12 of 43	

SPI level shift 3.3V <=> 1.8V



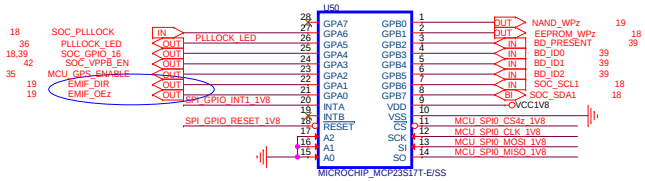


1.8V Level



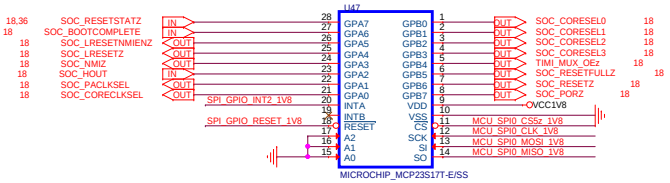
MicroChip SPI to GPIO

1.8V Level



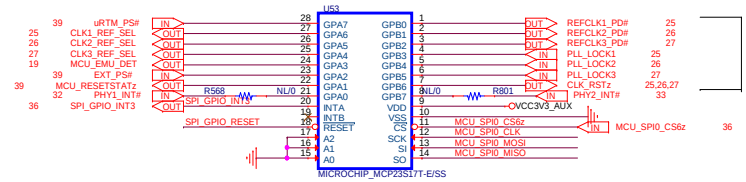
MicroChip SPI to GPIO

1.8V Level



MicroChip SPI to GPIO

3.3V Level



MicroChip SPI to GPIO

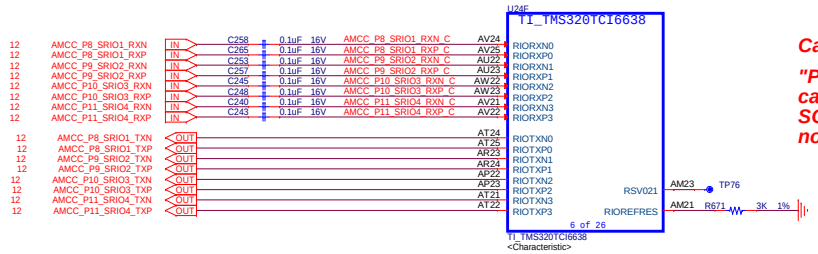
CDCM-620X Control

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title		
	SPI to GPIO Converter	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 13 of 43	

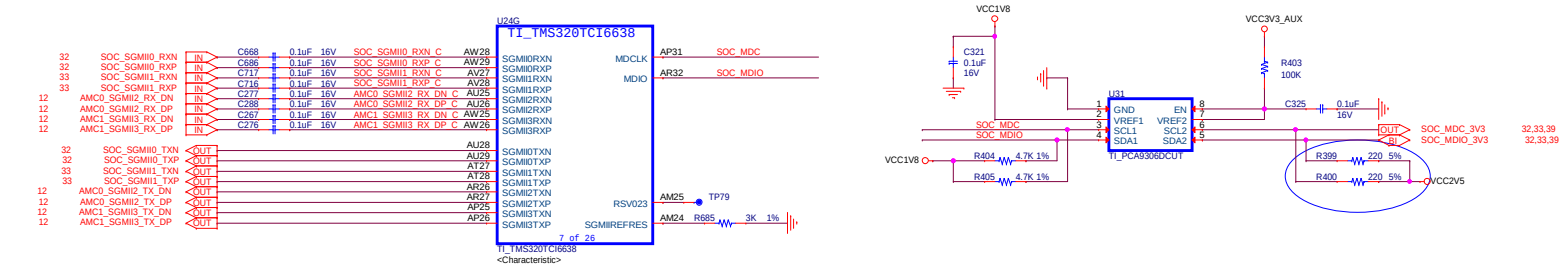
SRIO X4



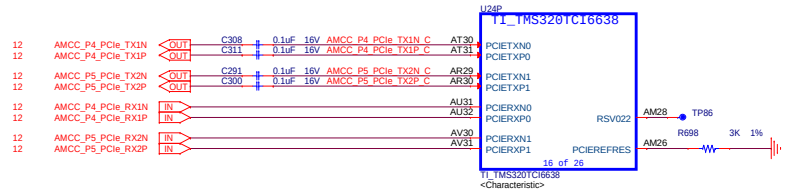
Caution!

"Place ALL SRIO DC-blocking caps on top layer adjacent to the SOC's RX pins so that there are no additional vias"

SGMII X4



PCIE X2



Caution!

"Place ALL PCIe DC-blocking caps close to the TX pins"

HyperLink X8

"The HyperLink routes should have a maximum of 2 vias and no via stubs – All routes should be on the outer layer of the board."

Designed for TI by ADVANTECH

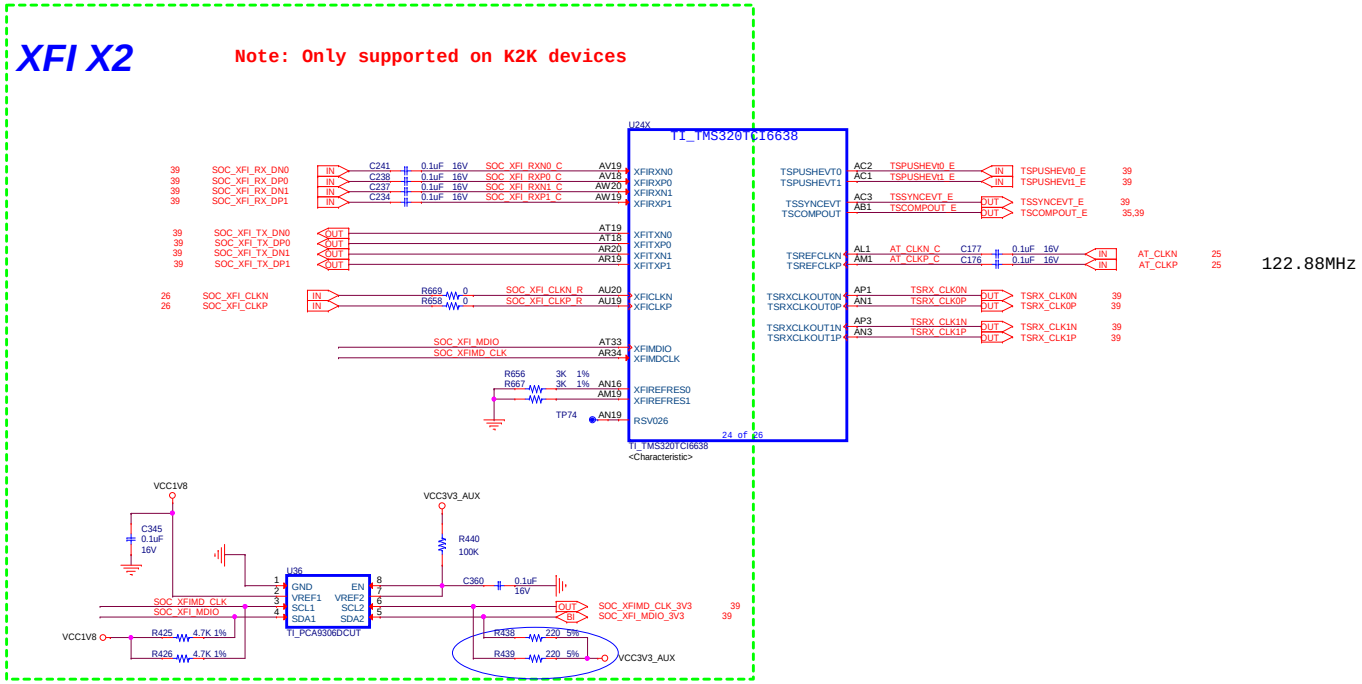
DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

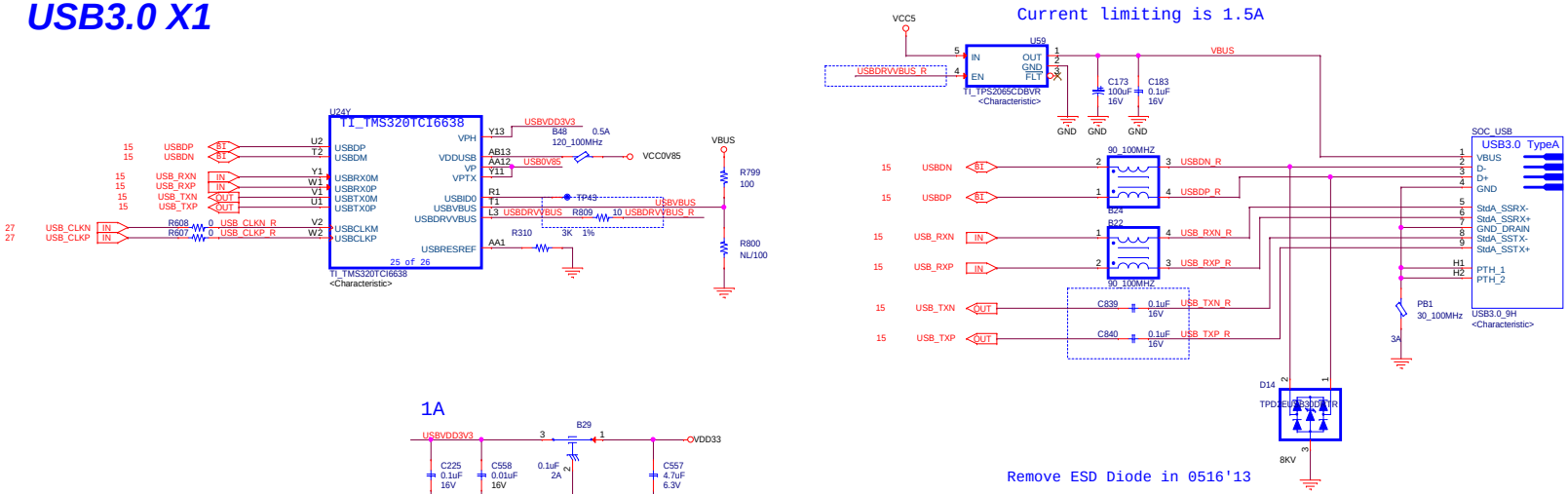
Title	SOC_SERDES_PORTS	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 14 of 43	

XFI X2

Note: Only supported on K2K devices



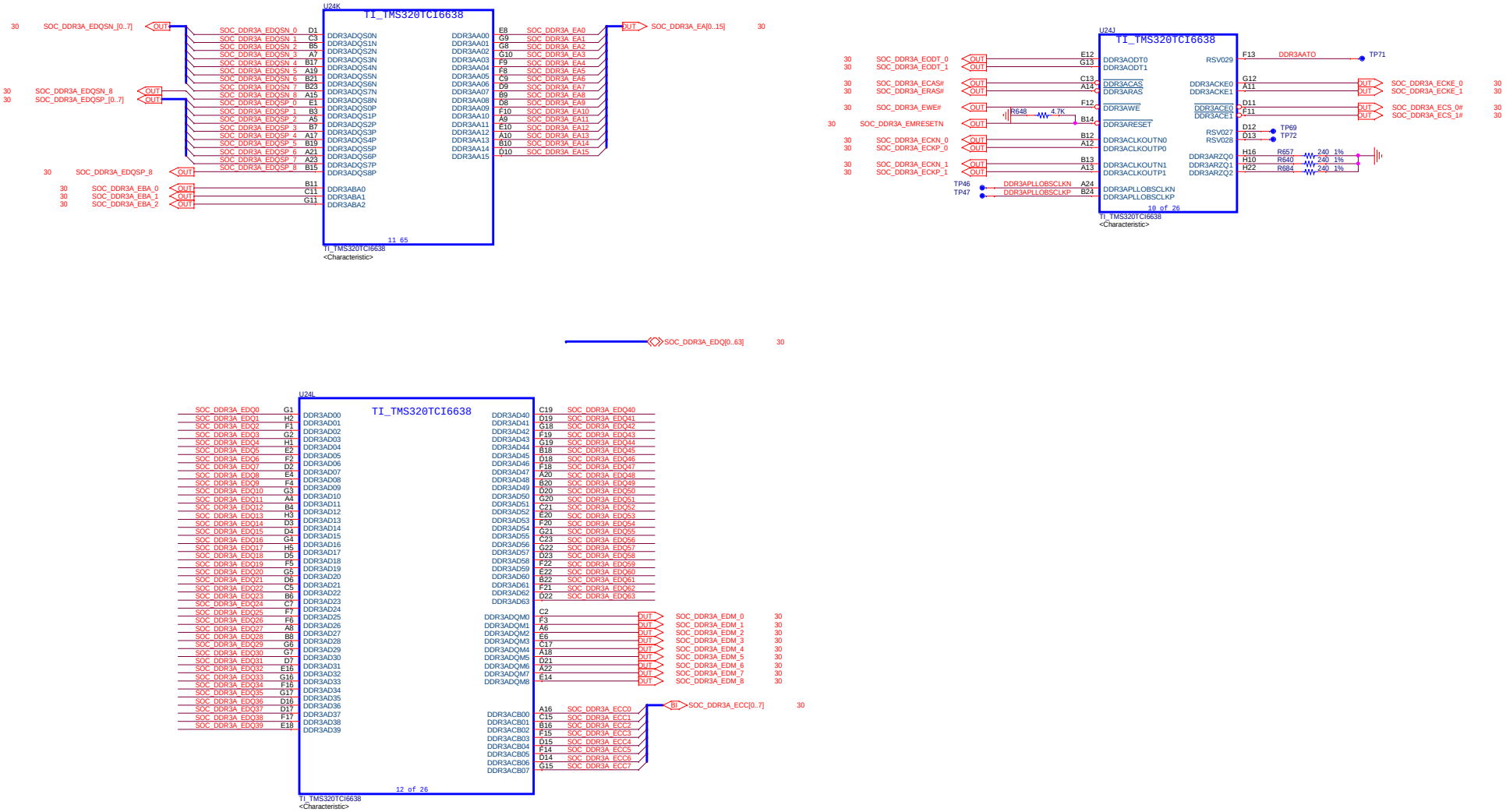
USB3.0 X1



Designed for TI by ADVANTECH

DSPM-8305E

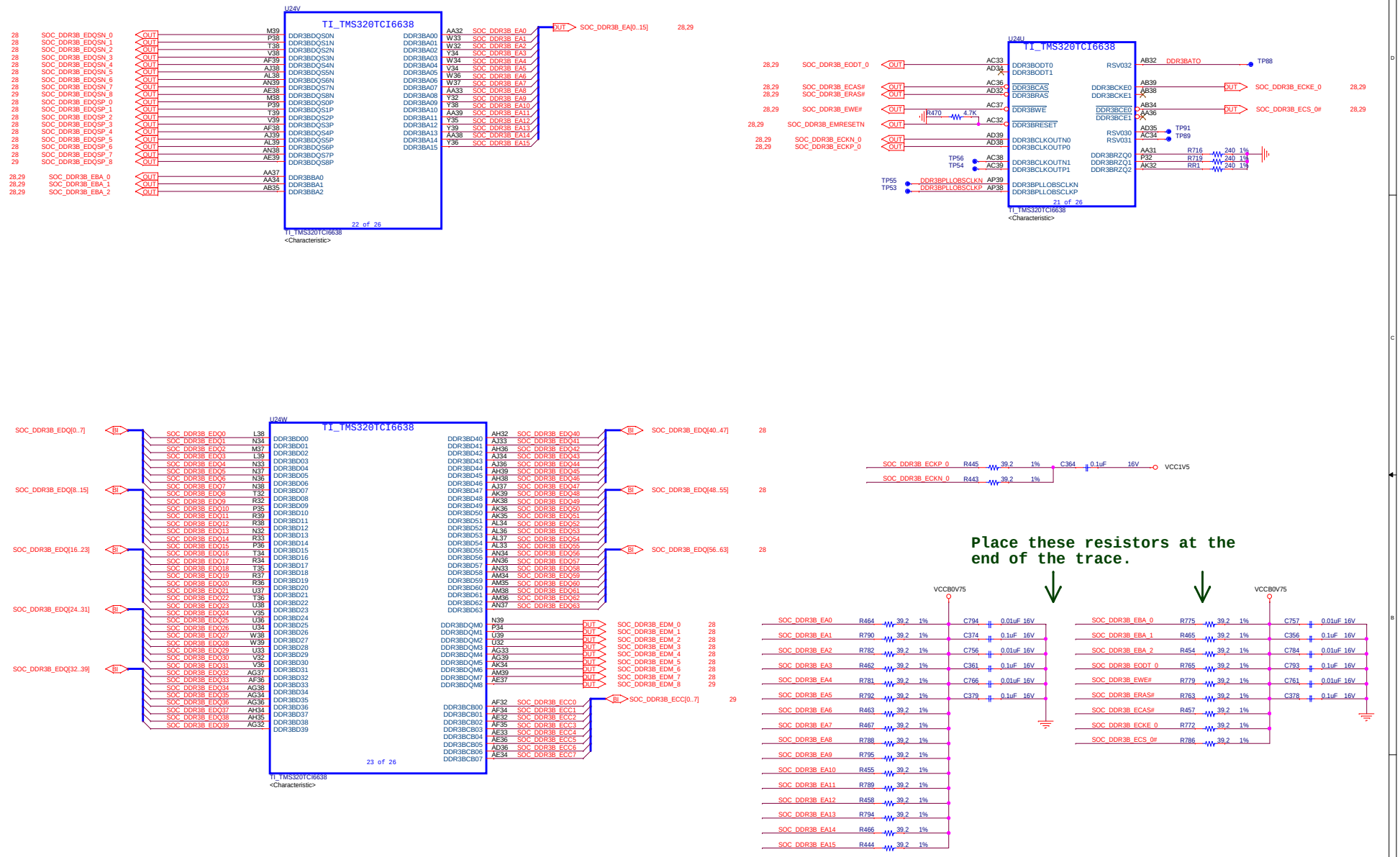
Title		
SOC_XFI_USB		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 15 of 43	



Designed for TI by ADVANTECH

DSPM-8305E

Title		
SOC_DDR3A		
Size: C	Document Number: K2EVM-HK	Rev: A103
Date: Thursday, May 30, 2013	Sheet 16 of 43	

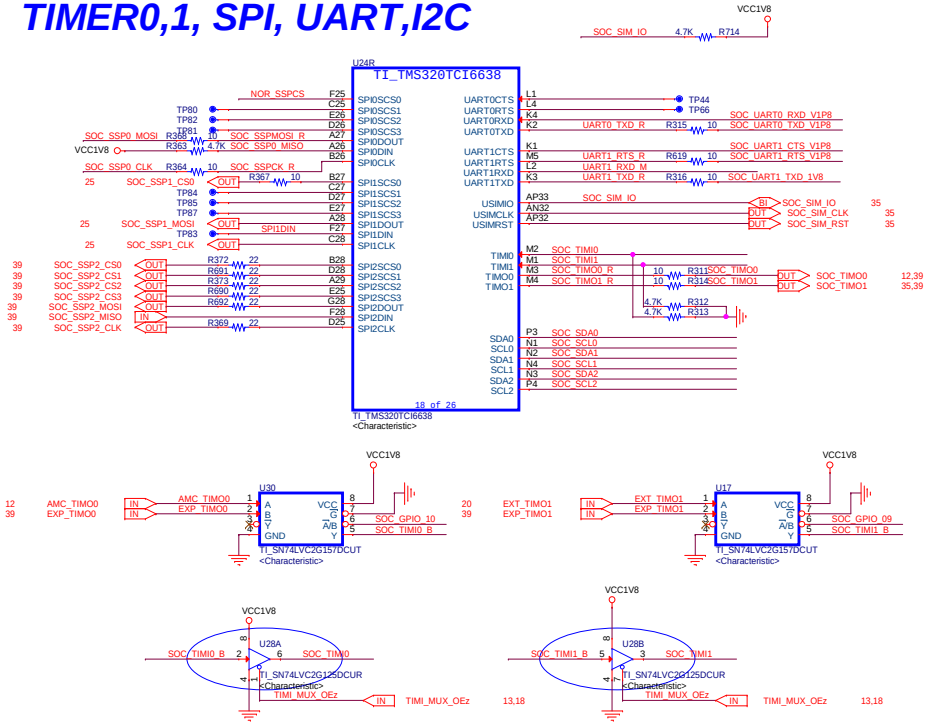


Designed for TI by ADVANTECH

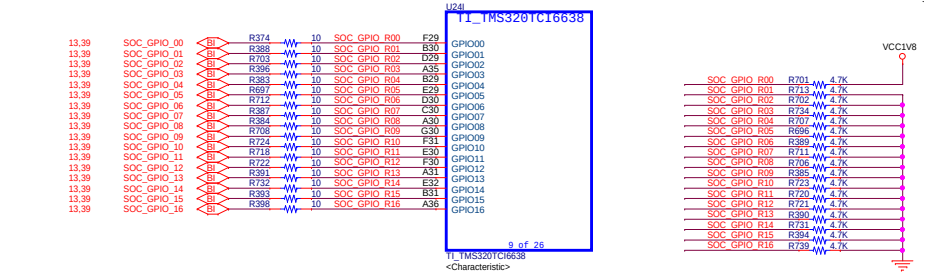
DSPM-8305E

Title		
	SOC_DDR3B	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 17 of 43	

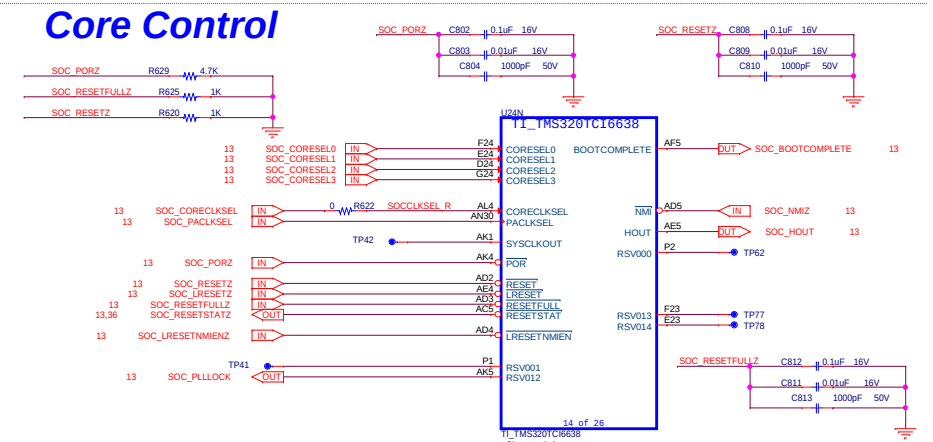
TIMER0,1, SPI, UART,I2C

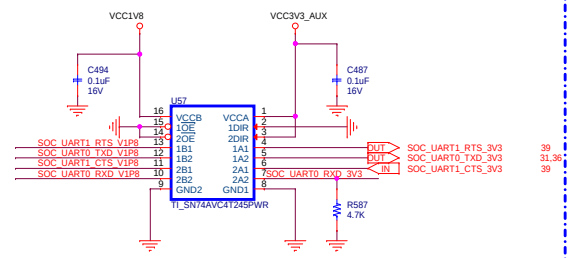


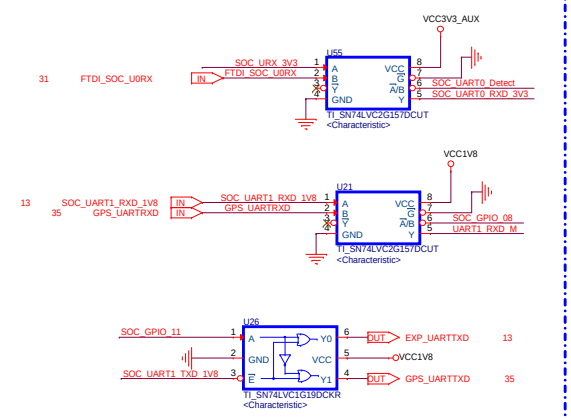
GPIO

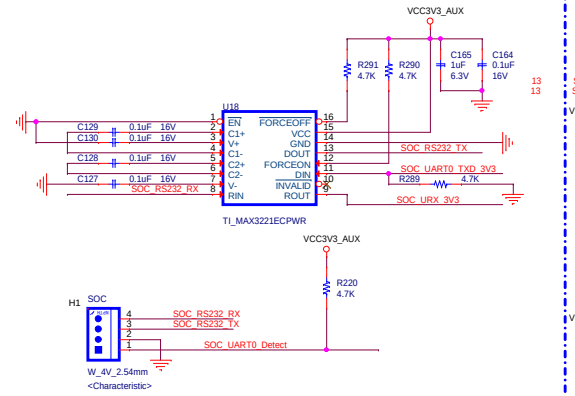


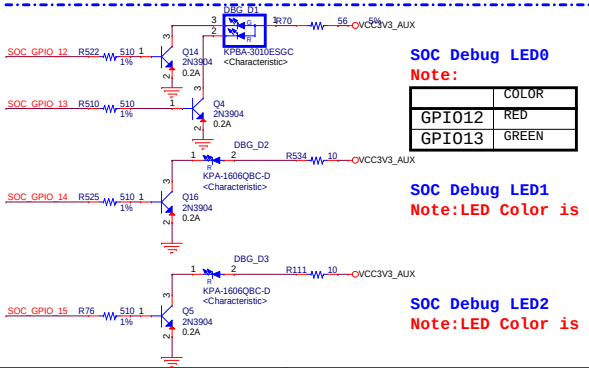
Core Control











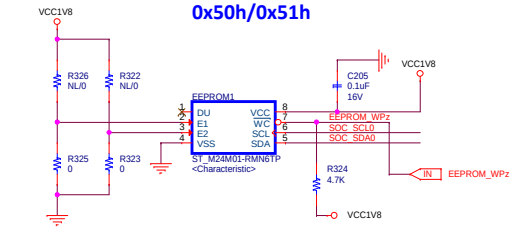
SOC Debug LED0
Note:

	COLOR
GPIO12	RED
GPIO13	GREEN

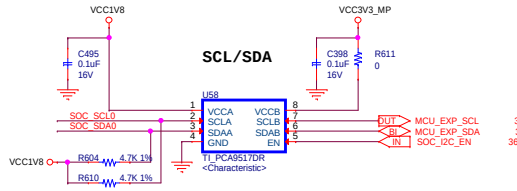
SOC Debug LED1
Note:LED Color is BLUE

SOC Debug LED2
Note:LED Color is BLUE

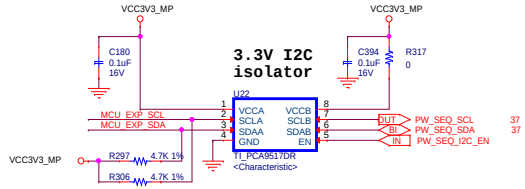
1M-bit I2C EEPROM 0x50h/0x51h



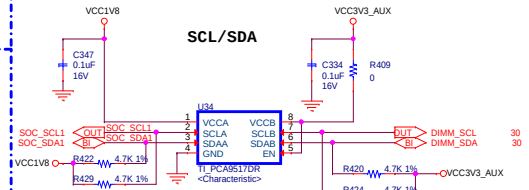
SCL/SDA



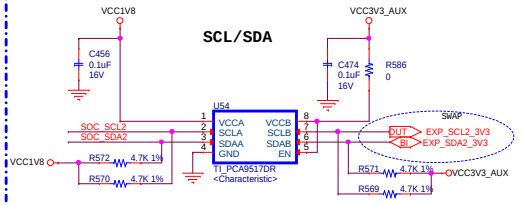
3.3V I2C isolator



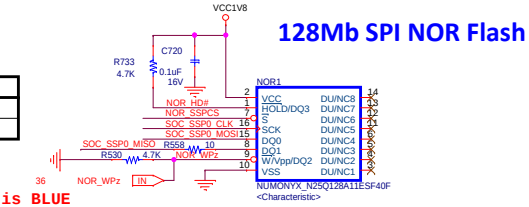
SCL/SDA



SCL/SDA



128Mb SPI NOR Flash

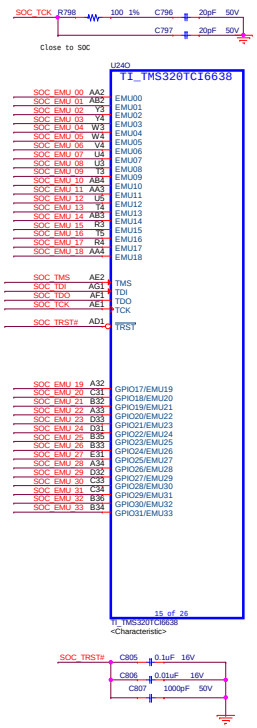


Designed for TI by ADVANTECH DSPM-8305E

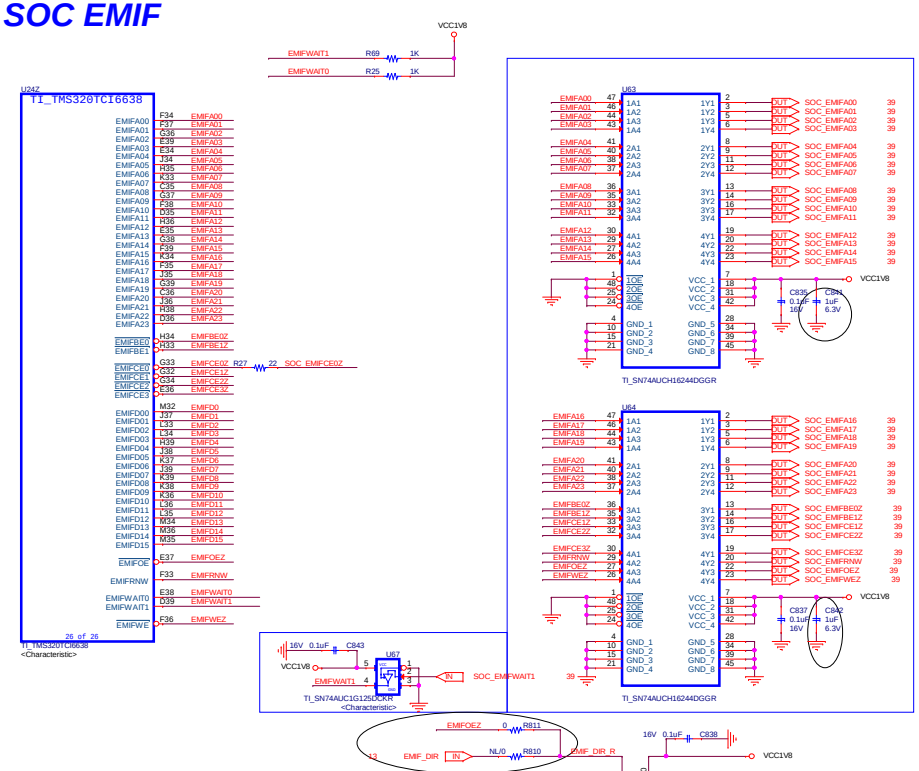
TEXAS INSTRUMENTS ADVANTECH

Title	SOC_MISC	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 18 of 43	

EMU & JTAG

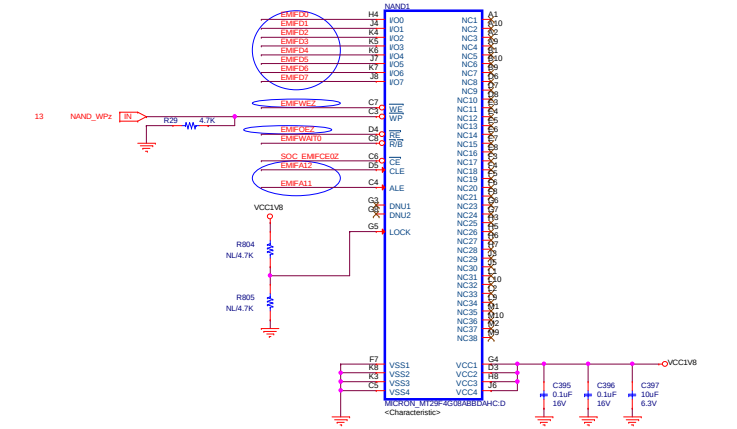


SOC EMIF

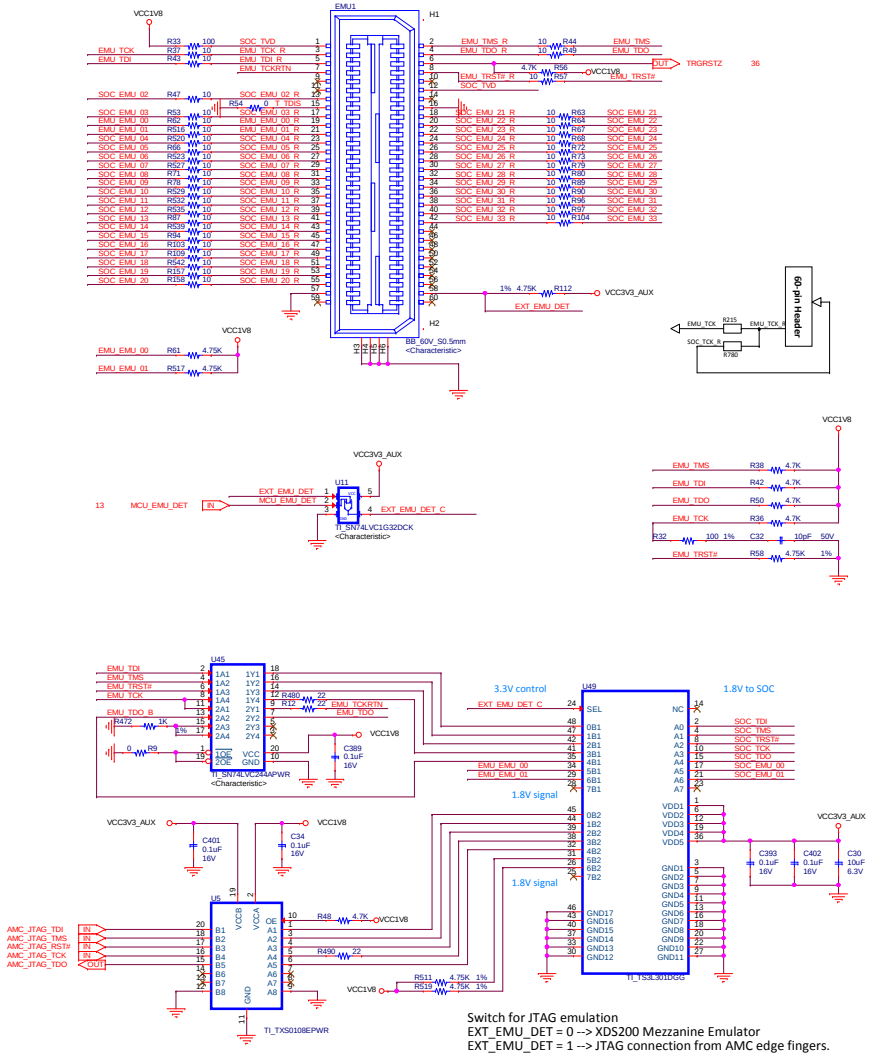


NAND FLASH

Note: NAND FLASH Device size is 4Gb.



EMU CONN.



Switch for JTAG emulation
EXT_EMU_DET = 0 --> XDS200 Mezzanine Emulator
EXT_EMU_DET = 1 --> JTAG connection from AMC edge fingers.

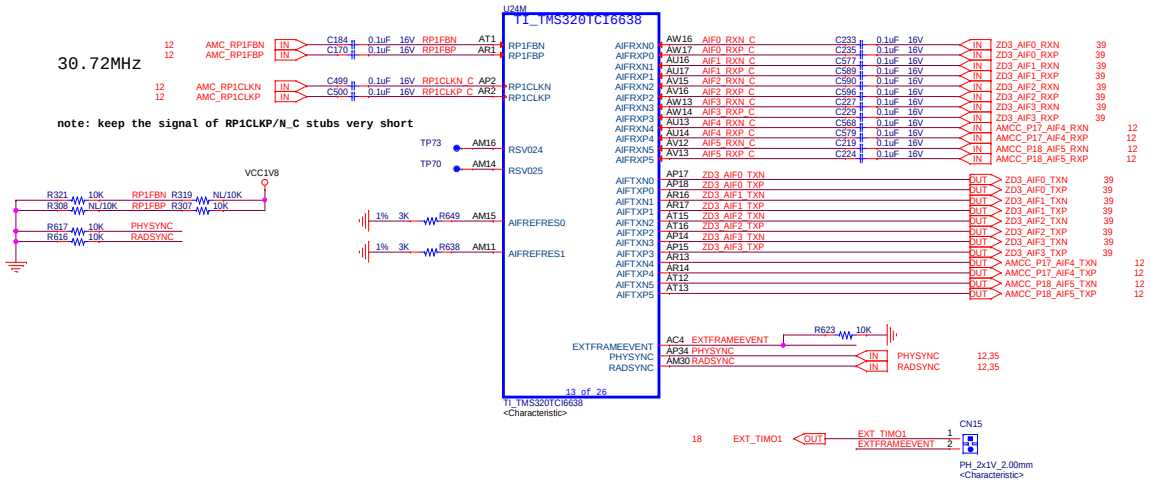
Designed for TI by ADVANTECH DSPM-8306E

TEXAS INSTRUMENTS ADVANTECH

Title		
SOC_JTAG_EMU		
Size: Custom	Document Number: K2EVM-HK	Rev: A103
Date: Thursday, May 30, 2013	Sheet 19 of 43	

SOC AIF

Note: AIF is only supported on K2H devices



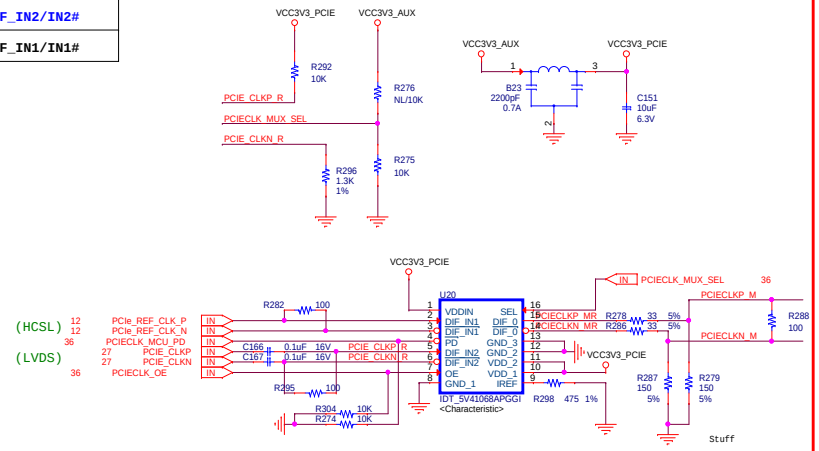
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

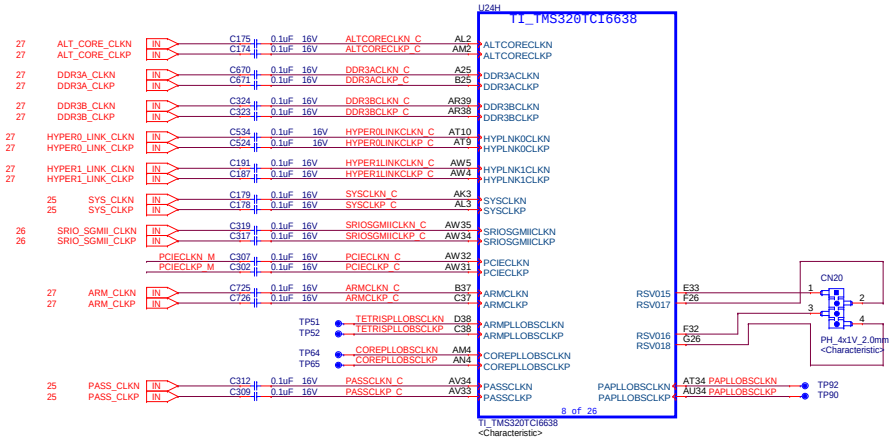
Title		
	SOC_AIF	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 20 of 43	

SOC CLOCK / RESET

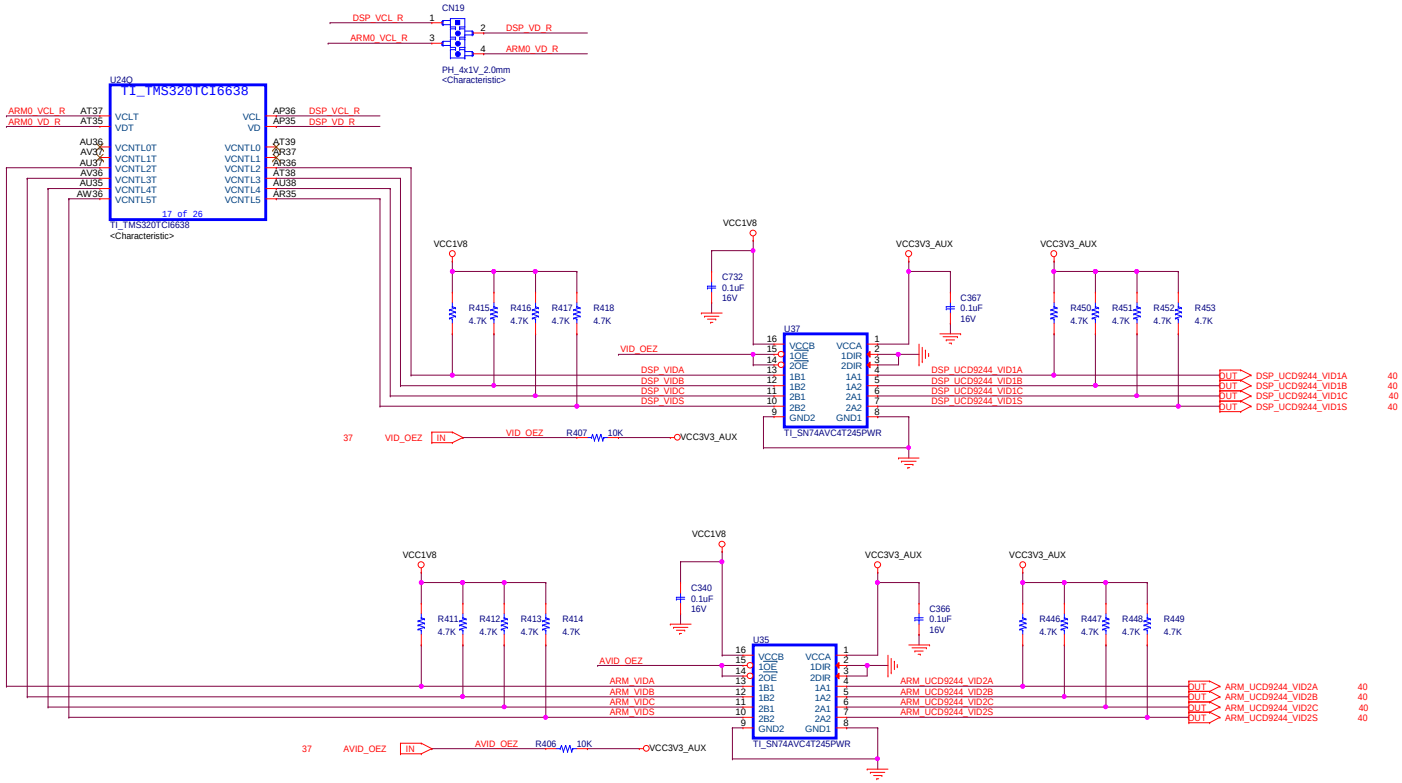
SEL	I/P PAIR SEL
LOW	DIF_IN2/IN2#
HIGH	DIF_IN1/IN1#



All blocking capacitors should be placed near SOC to keep connecting routes short and minimize vias



Smart Reflex

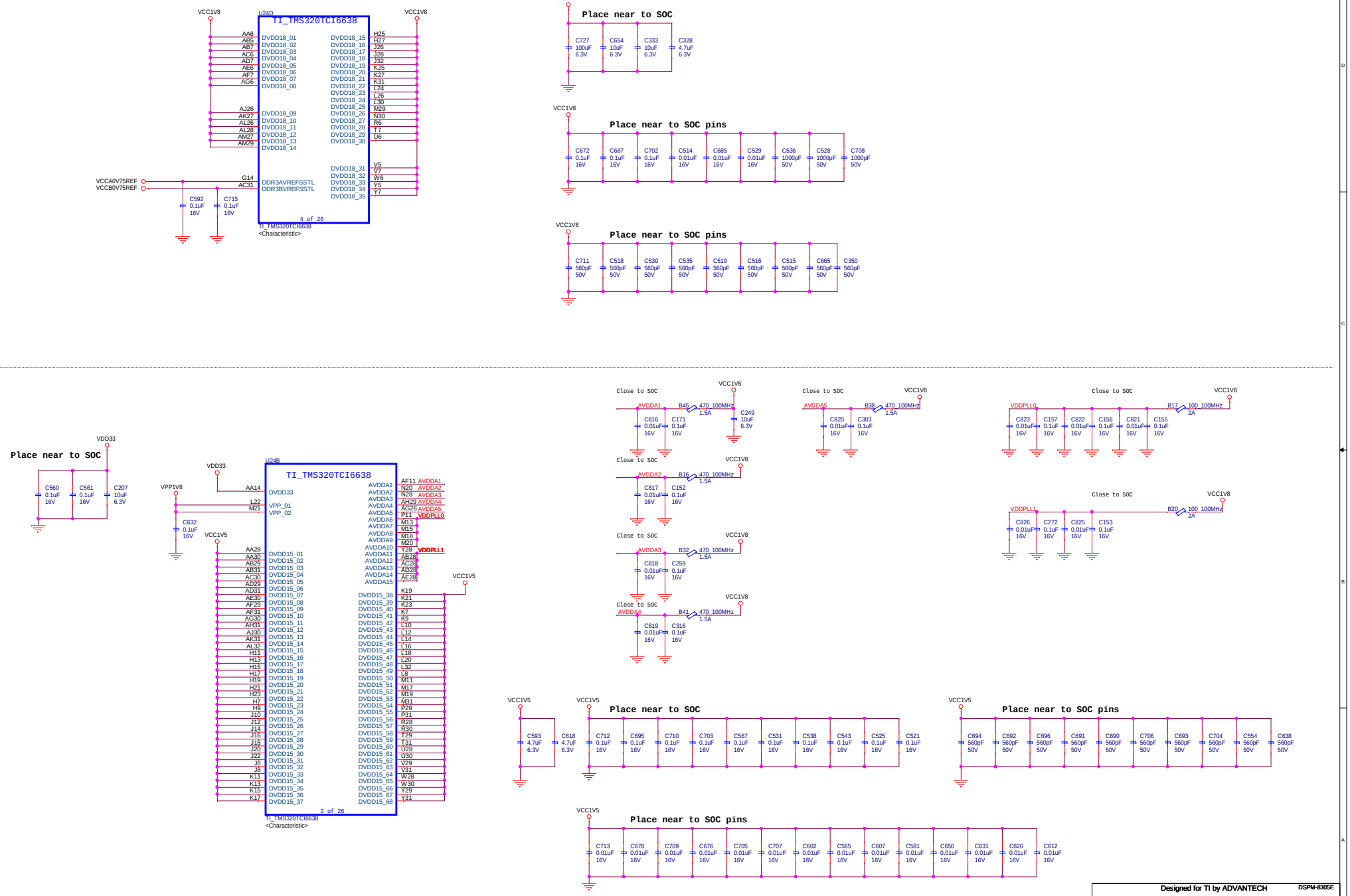


Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title	SOC_CLOCK & Smart-Reflex VID	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 21 of 43	

1.8V_1A

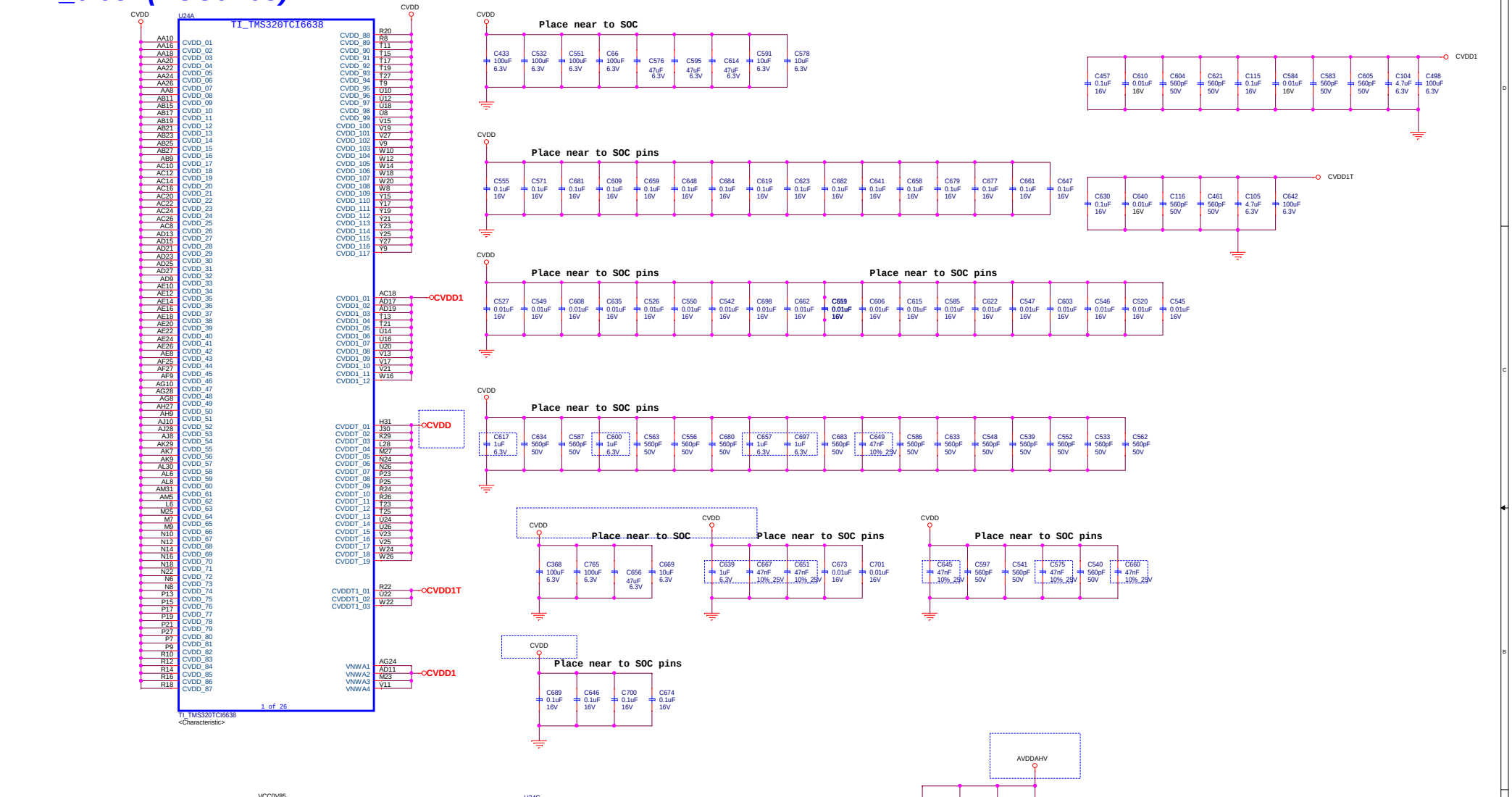


Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title		
SOC_POWERA		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 22 of 43	

0.85V - 1.05V (CVDD) (Smart Reflex) Fix_0.95V(VCC0V95)



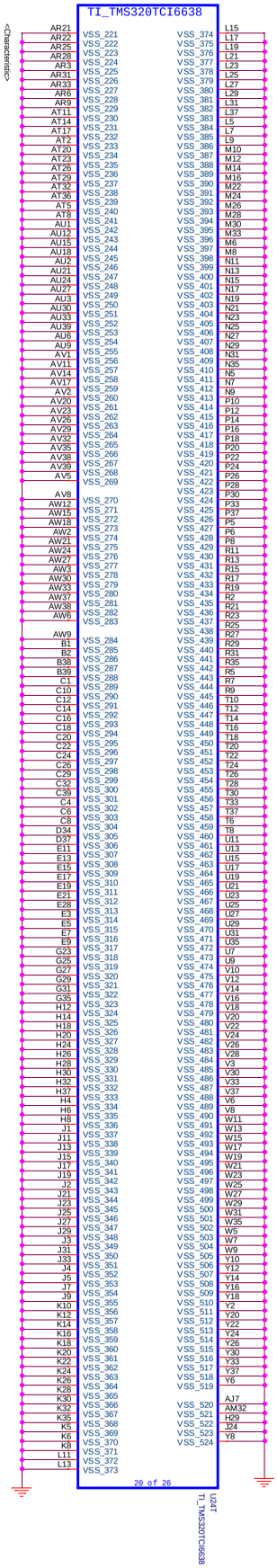
Designed for TI by ADVANTECH

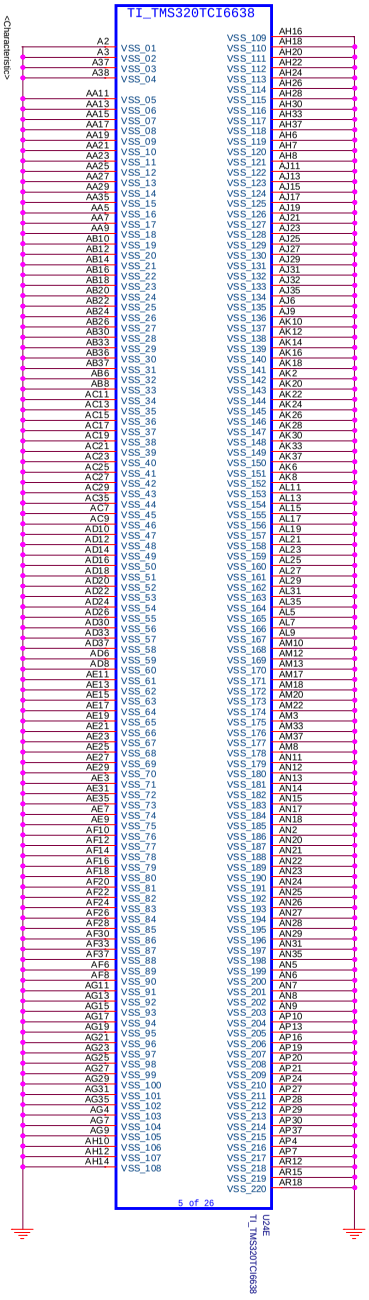
DSPM-8305E

Title = SOC_POWERB

Size	Document Number	Rev
C	K2EVM-HK	A103

Date: Thursday, May 30, 2013 Sheet 23 of 43





Designed for TI by ADVANTECH

DSPM-8806E

TEXAS INSTRUMENTS ADVANTECH

Title

SOC_GND

Size: C

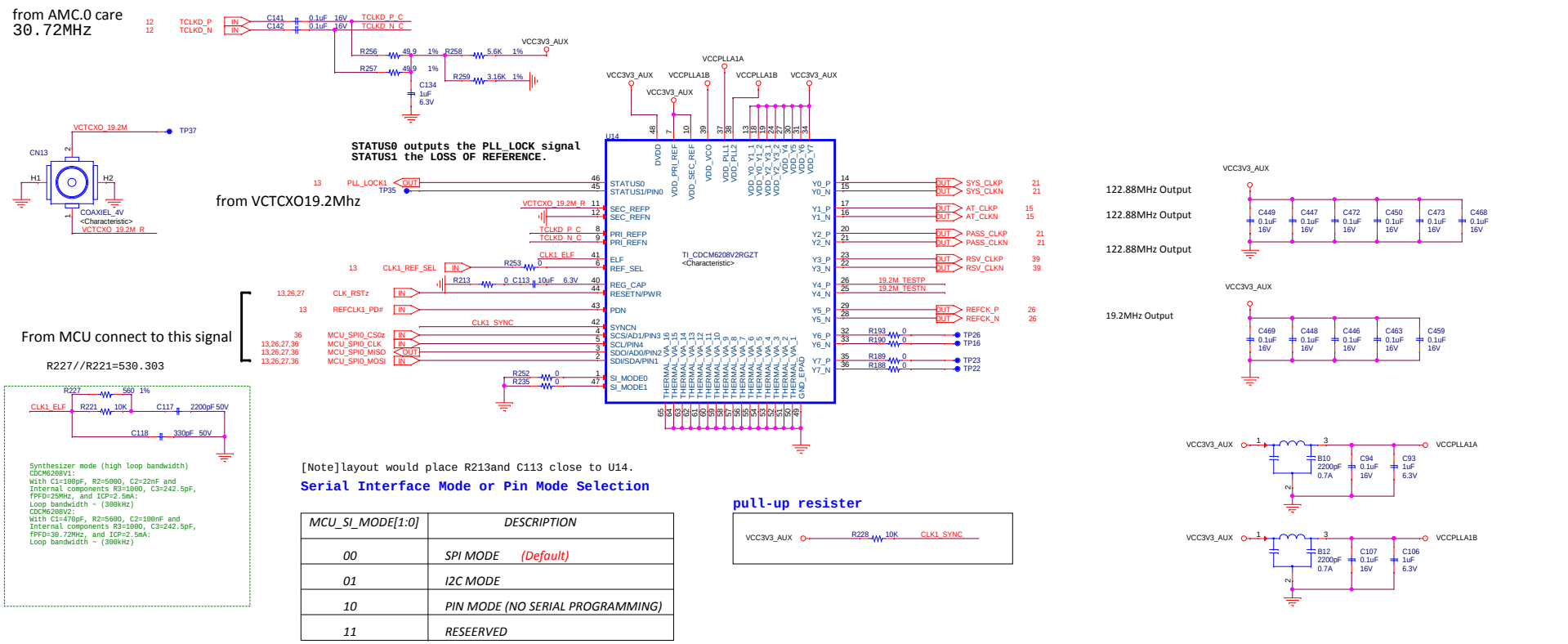
Document Number: K2EVM-HK

Rev: A103

Date: Thursday, May 30, 2013

Sheet 24 of 43

CLOCK GEN1



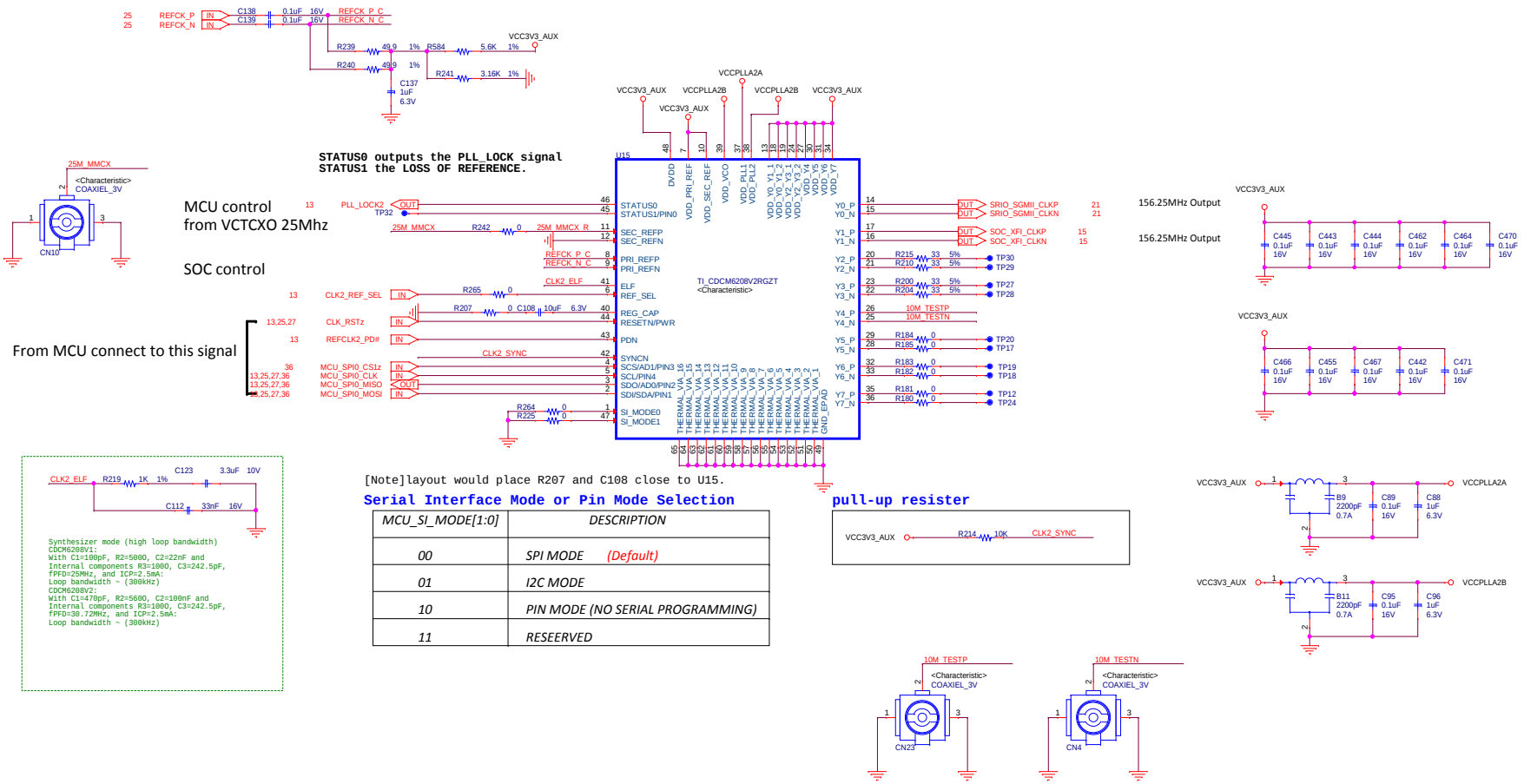
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

Designed for TI by ADVANTECH

TEXAS INSTRUMENTS ADVANTECH

Title	CLOCK GEN1	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 25 of 43	

CLOCK GEN2



[Note]layout would place R207 and C108 close to U15.

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

pull-up resister

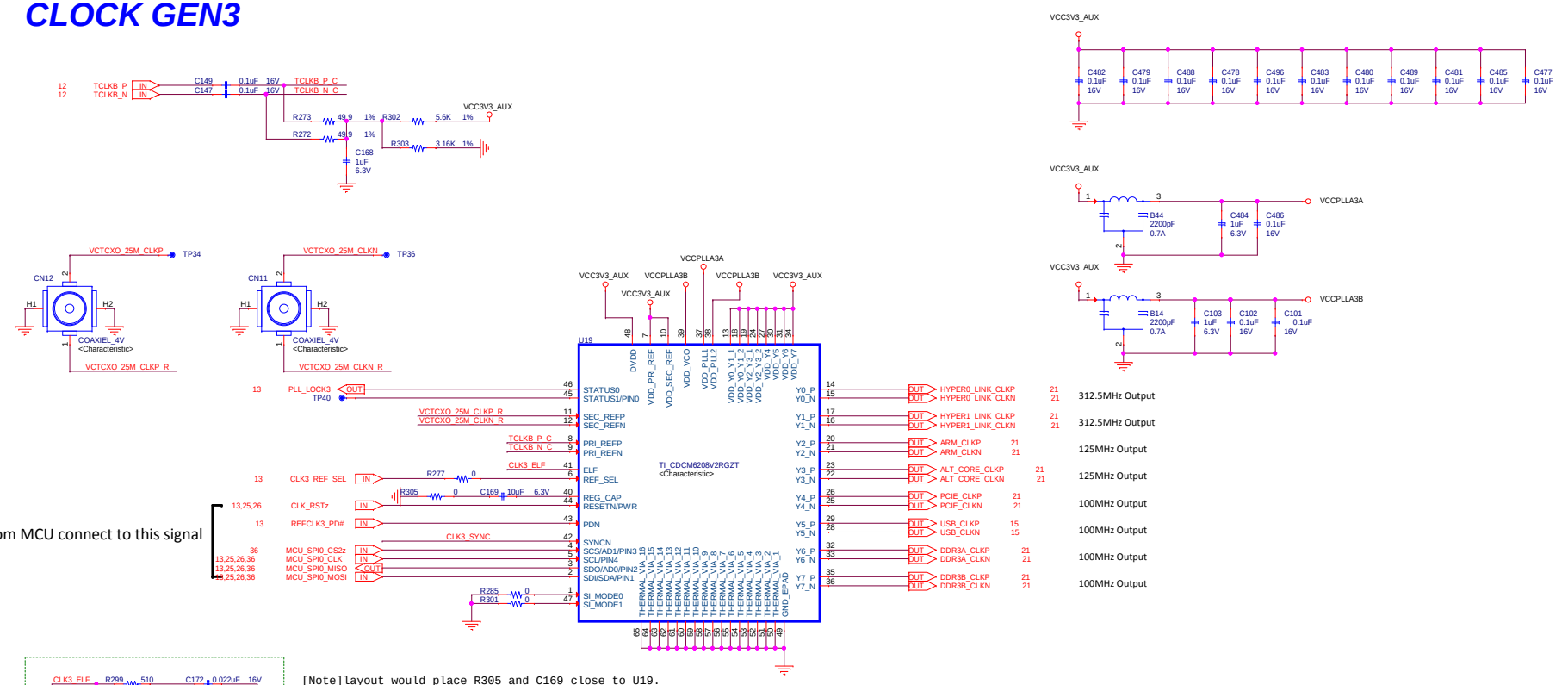
VCC3V3_AUX — R214 10K — CLK2_SYNC

Designed for TI by ADVANTECH

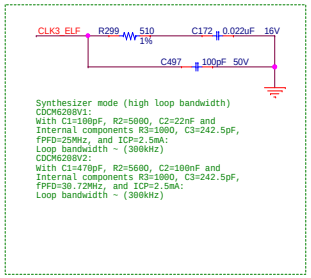
TEXAS INSTRUMENTS ADVANTECH

Title	CLOCK GEN2	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 26 of 43	

CLOCK GEN3

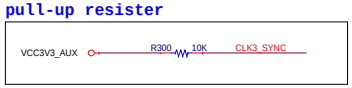


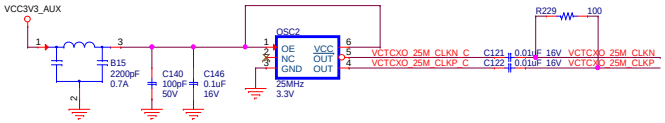
From MCU connect to this signal



[Note]layout would place R305 and C169 close to U19.

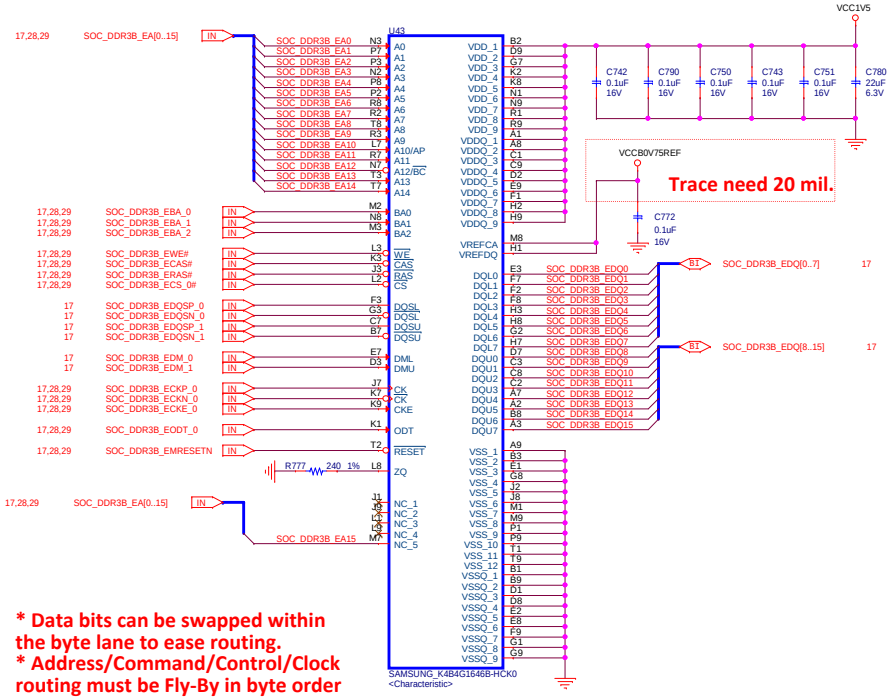
pull-up resister

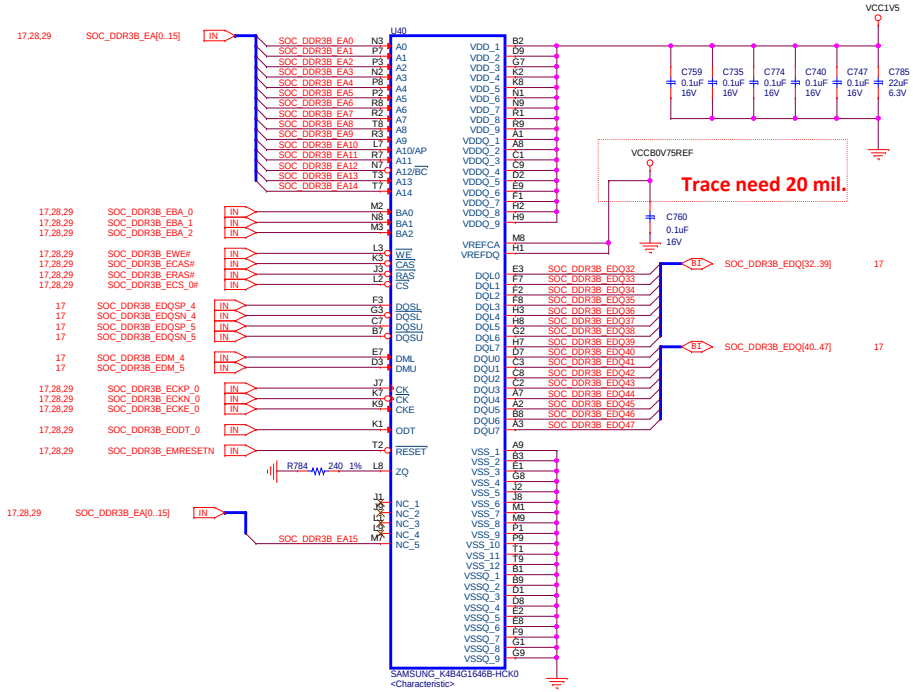




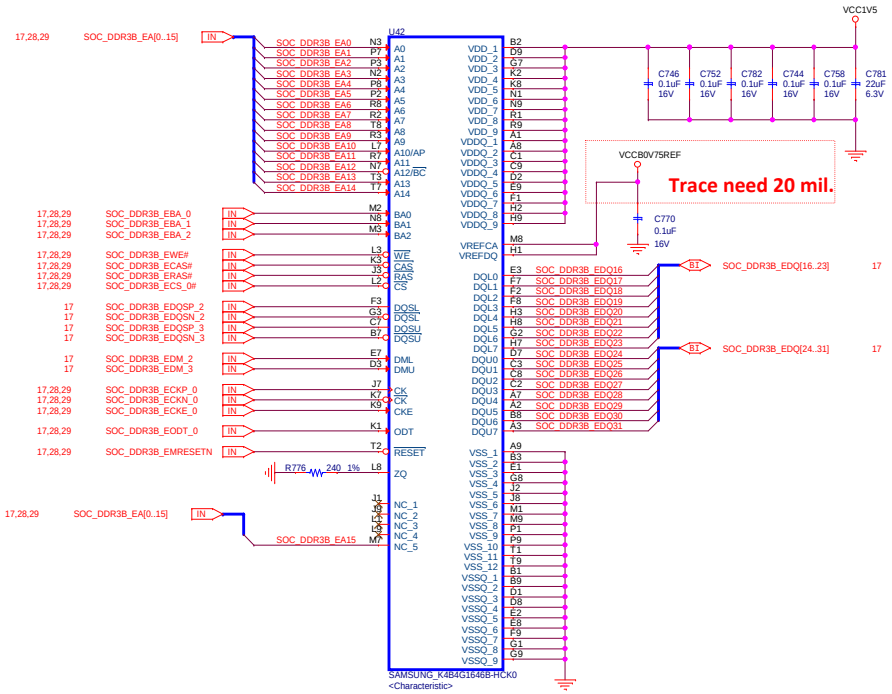
Designed for TI by ADVANTECH

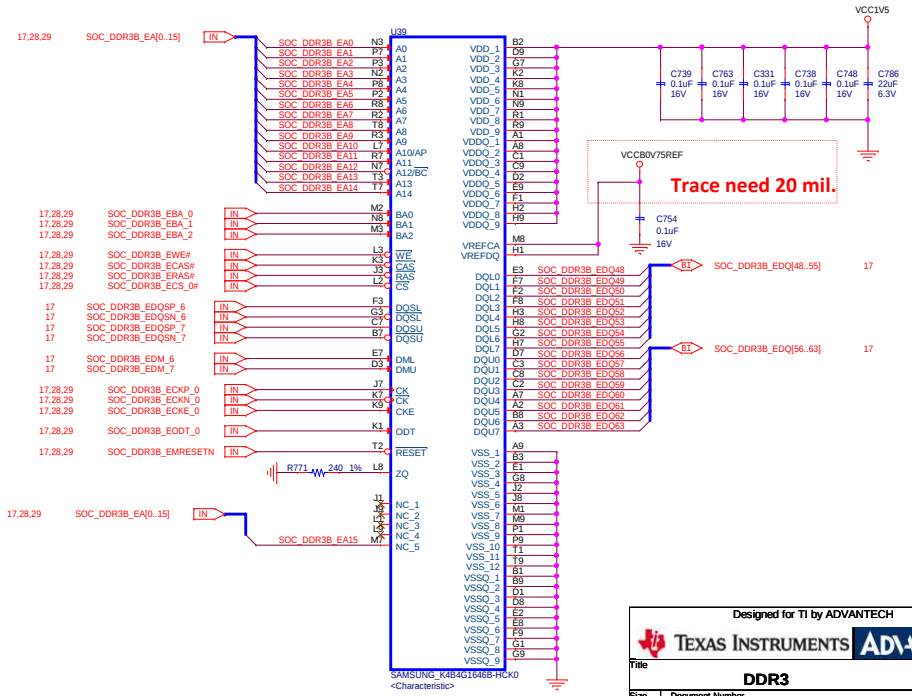
Title		
CLOCK GEN3		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 27 of 43	





*** Data bits can be swapped within the byte lane to ease routing.**
*** Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.**



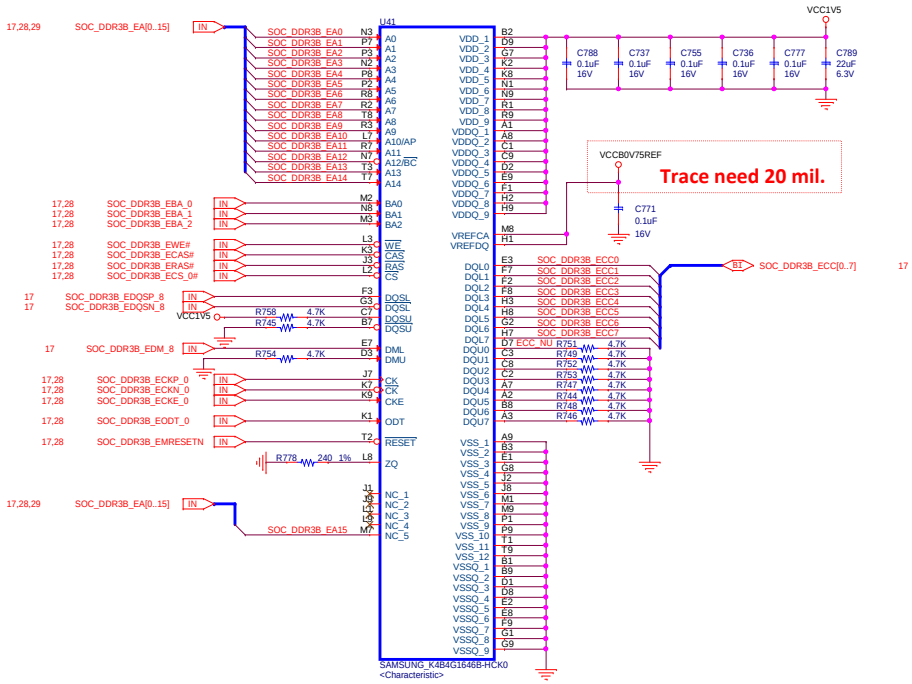


Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

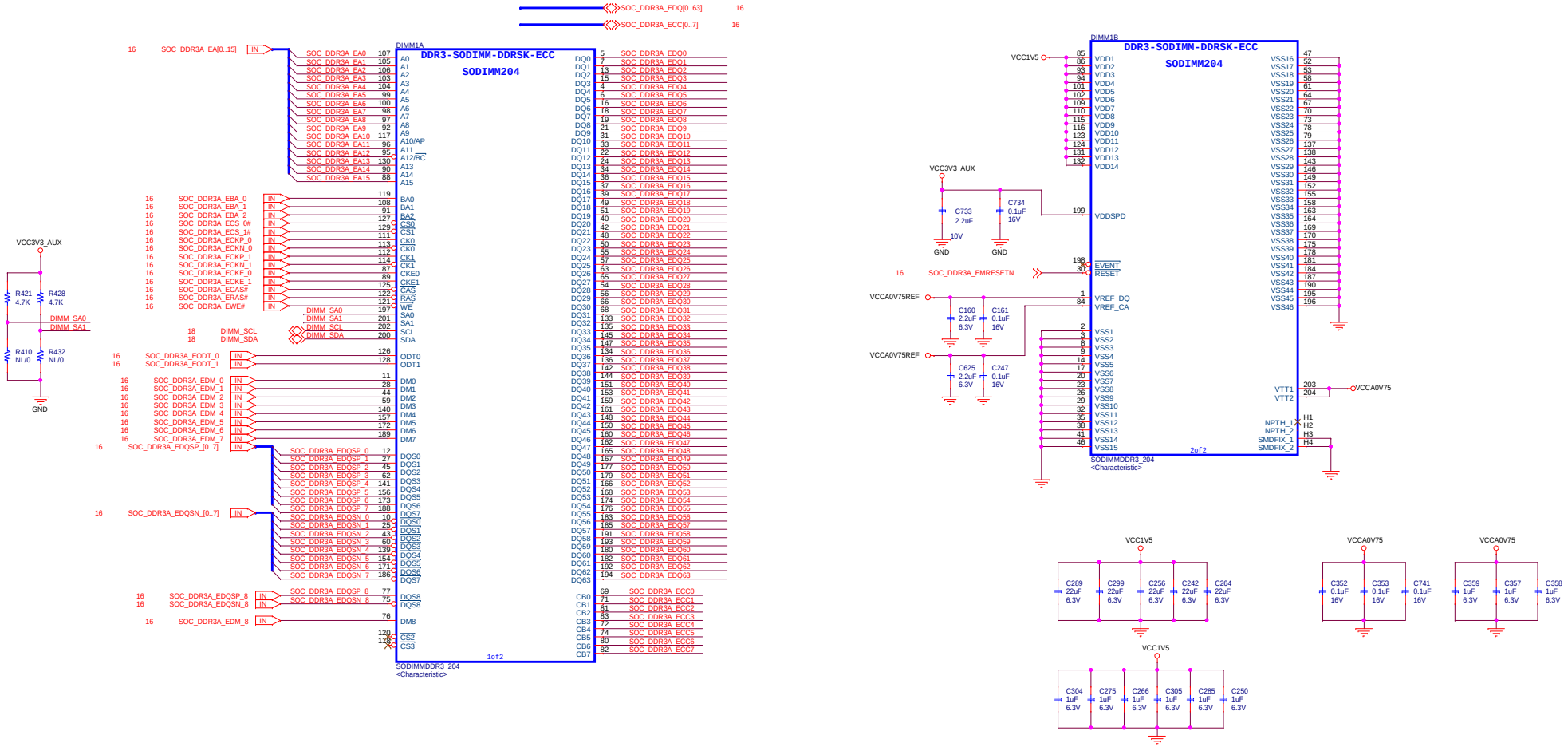
Title		
DDR3		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 28 of 43	

FOR ECC USE



Designed for TI by ADVANTECH DSPM-8305E

Title		
DDR3_ECC		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 29 of 43	

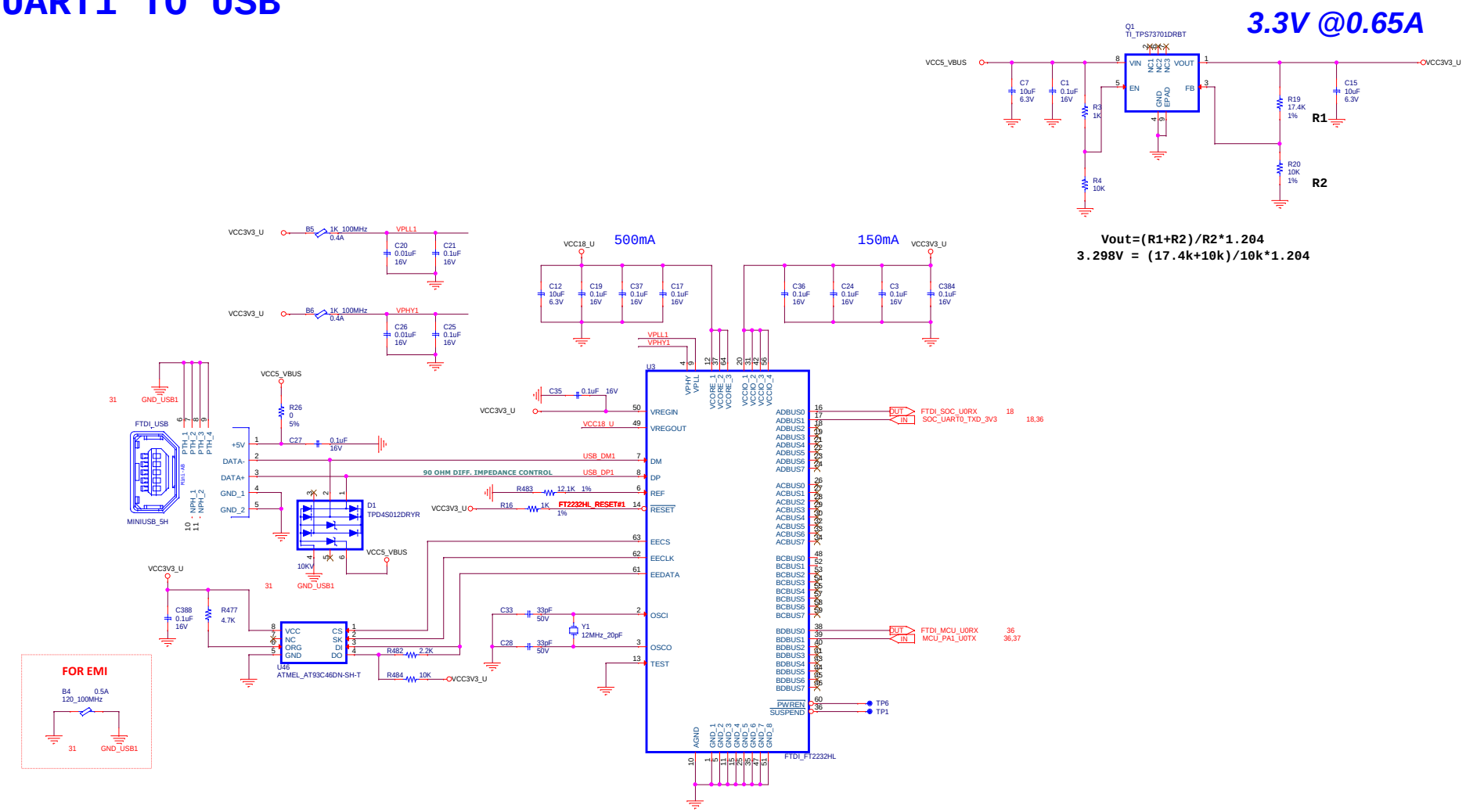


Designed for TI by ADVANTECH

Texas Instruments ADVANTECH

Title		
DDR3 SODIMM		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 30 of 43	

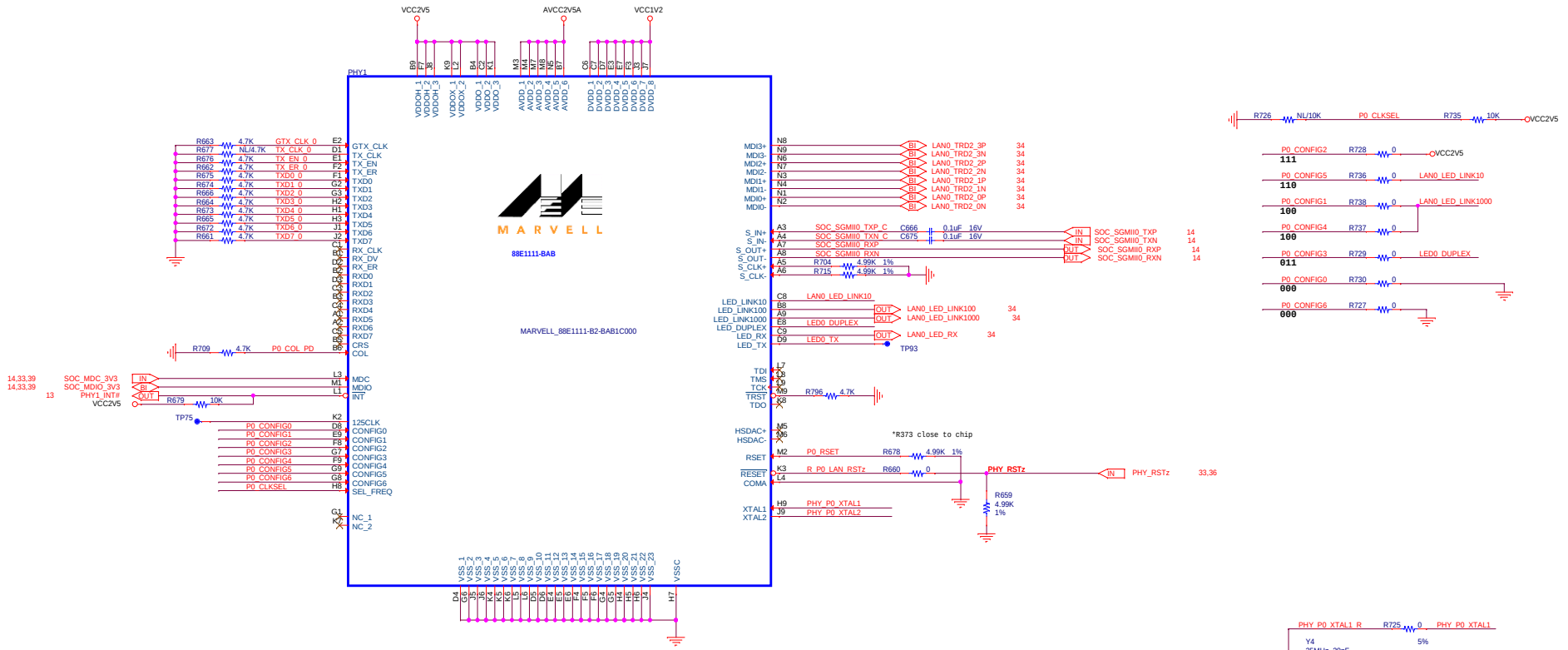
SoC UART1 TO USB



Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title		
SoC UART1 TO USB		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 31 of 43	



88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x00

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	000	LED_TX	PHY Address bit[2:0] 000
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4 CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

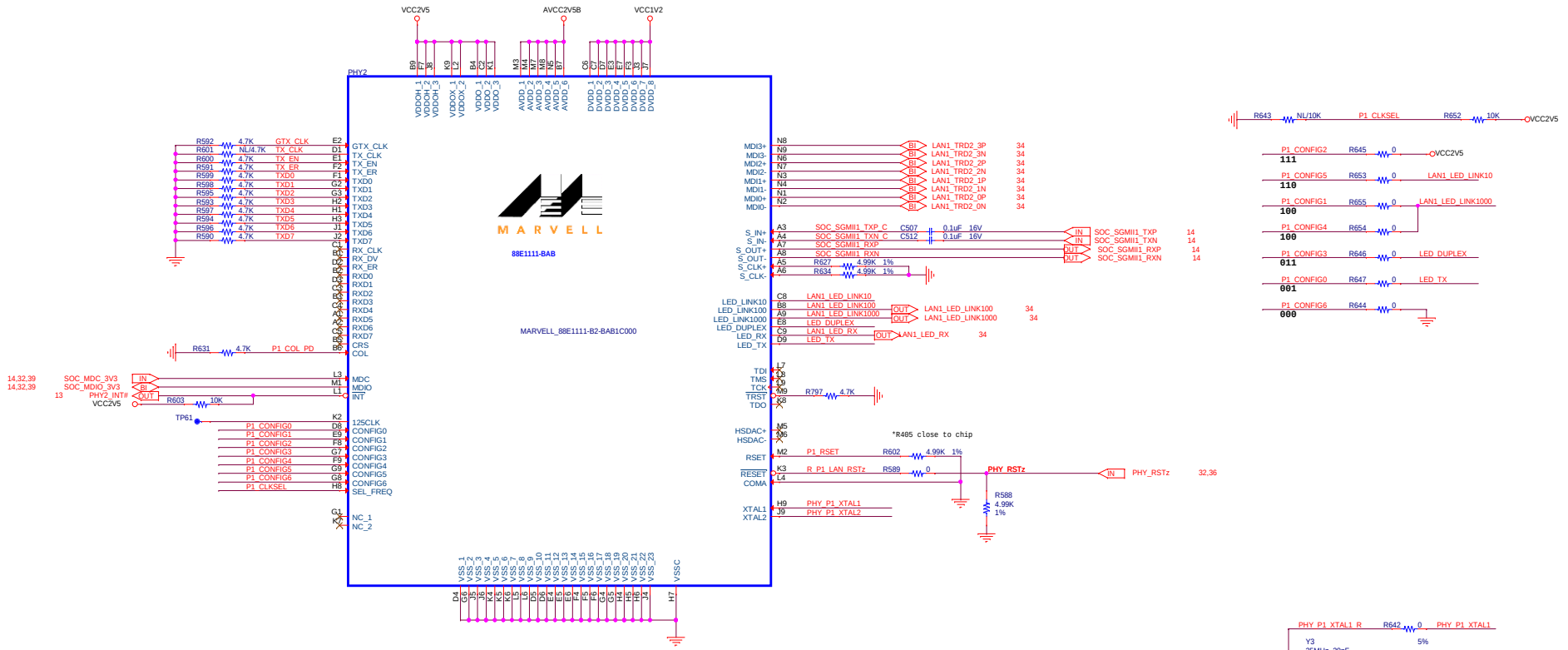
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: Gigabit Ethernet PHY1

Size: C | Document Number: K2EVM-HK | Rev: A103

Date: Thursday, May 30, 2013 | Sheet 32 of 43



88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4 CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: Gigabit Ethernet PHY2

Size: C | Document Number: K2EVM-HK | Rev: A103

Date: Thursday, May 30, 2013 | Sheet 33 of 43

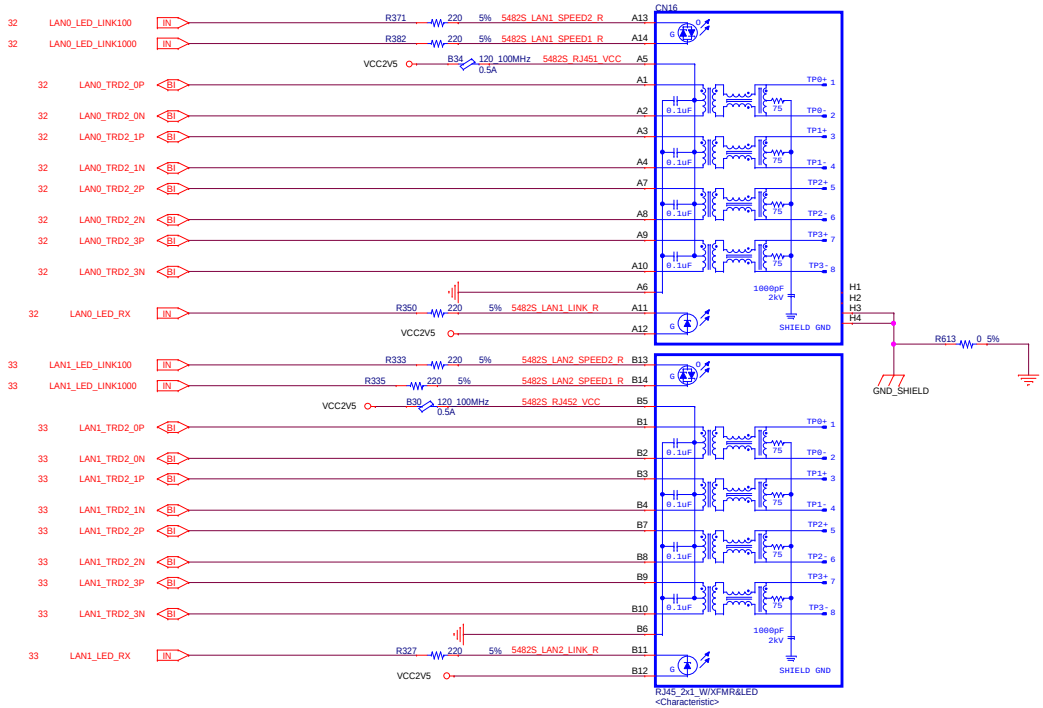
Bi-Color LED's on RJ45 controls from PHY

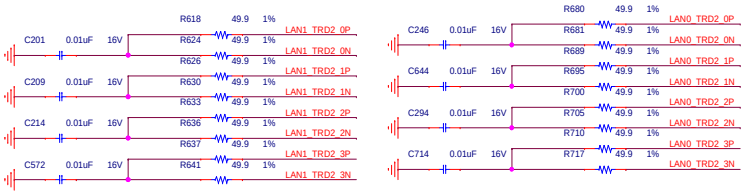
LAN-BI[88E1111 Output Port0]

	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

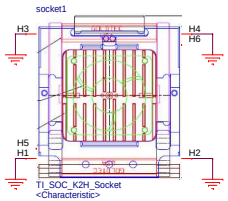
LAN-BI[88E1111 Output Port1]

	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

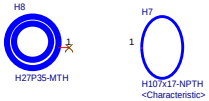




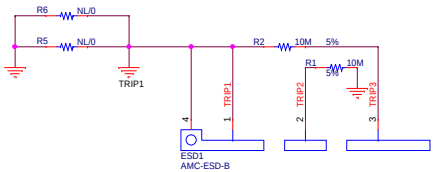
SoC Socket



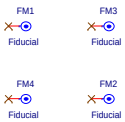
AMC Hole



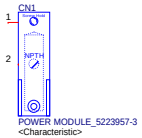
Front panel and ESD Strip



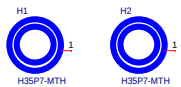
On board



Key Zone



XDS200 Holes

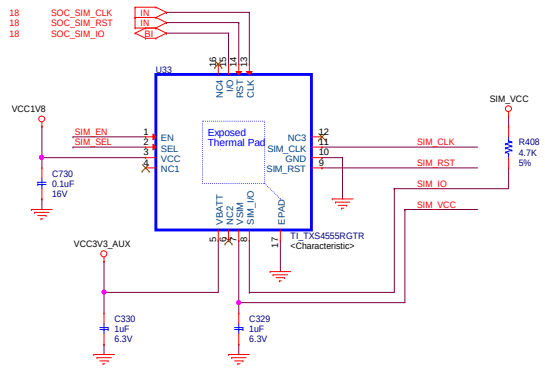


(Bottom Side 3mm) Placed Capacitors

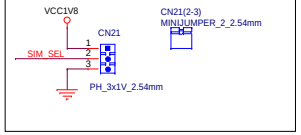
Designed for TI by ADVANTECH

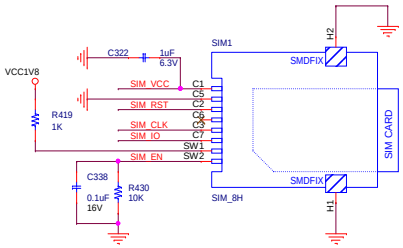
Title	88E1111 RJ45	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 34 of 43	

USIM

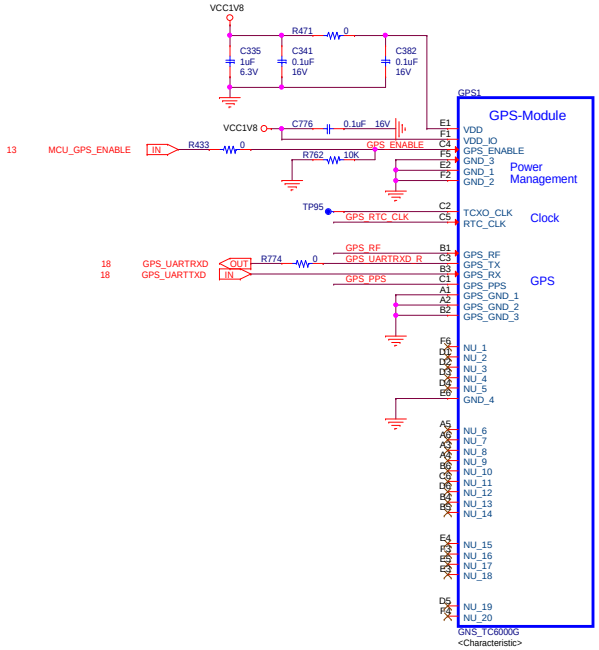


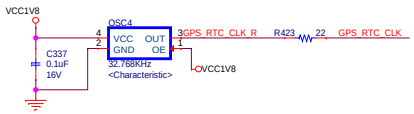
	High	Low (Default)
SIM_SEL	VCC_SIM Value = 2.95V	VCC_SIM Value = 1.8V

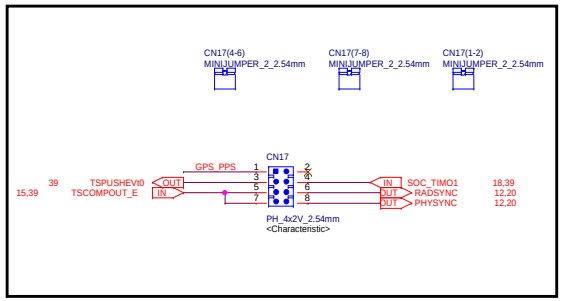




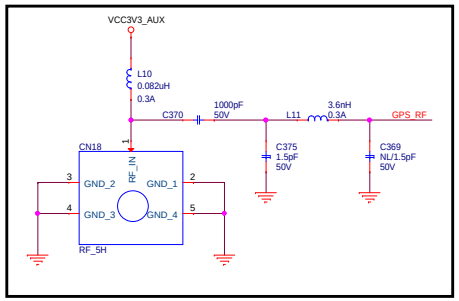
GPS







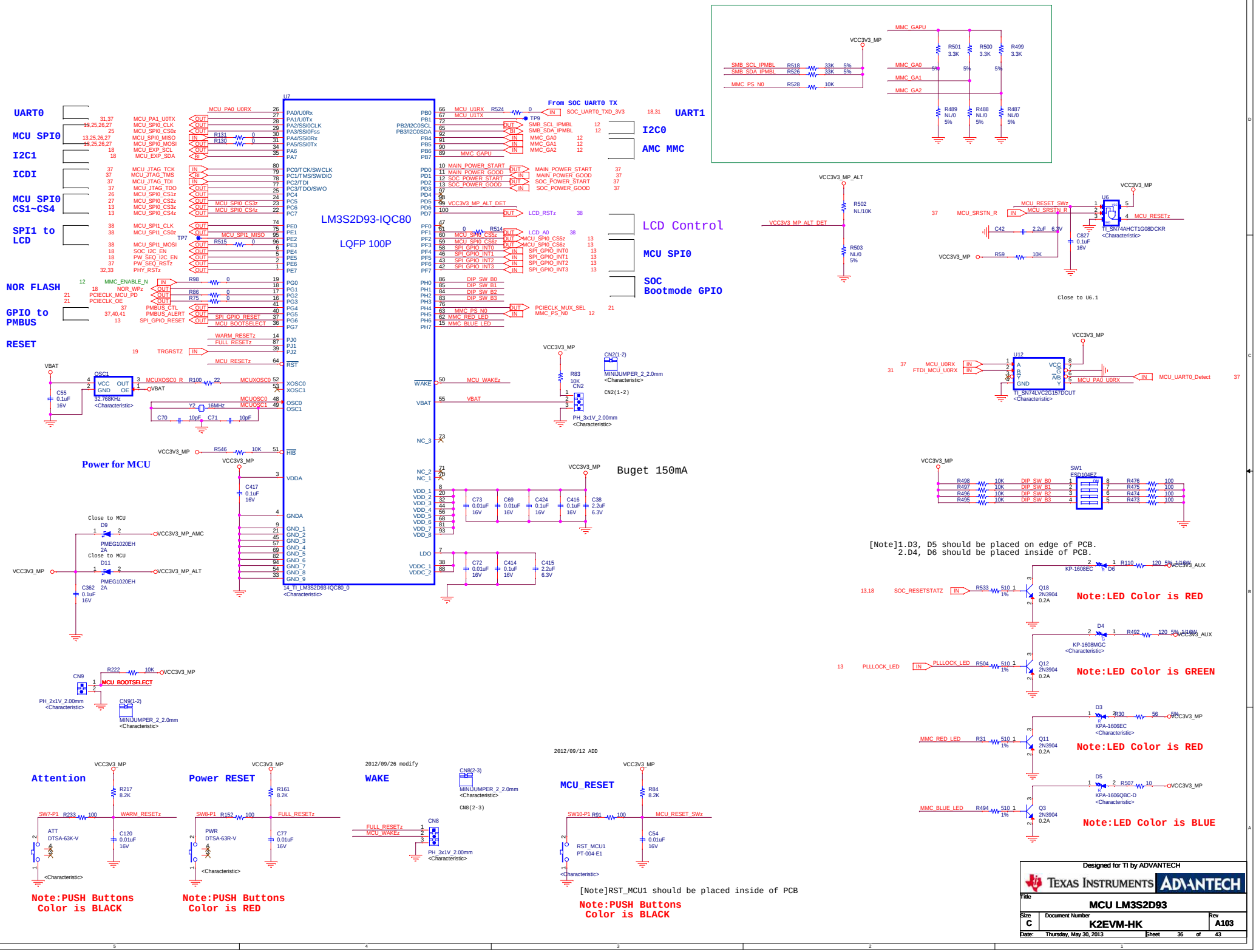
FOR ANTENNA CIRCUIT



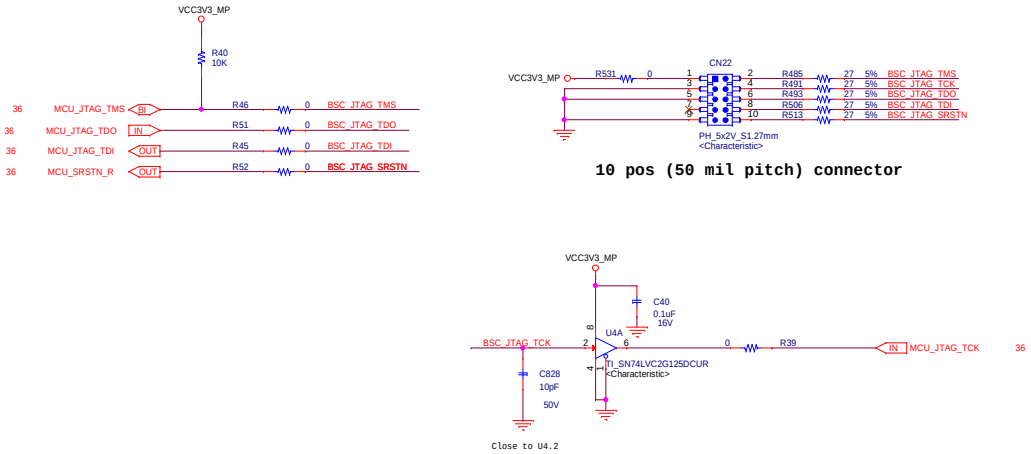
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

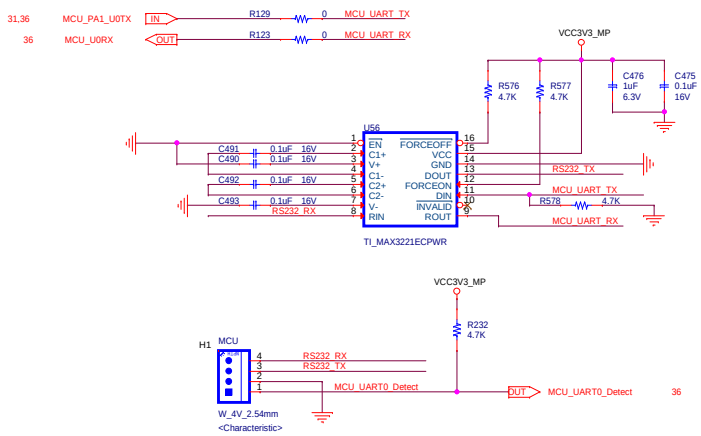
Title		
	GPS & SIM CARD	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 35 of 43	


UART0
MCU SPI0
I2C1
ICDI
MCU SPI0 CS1~CS4
SPI1 to LCD
NOR FLASH
GPIO to PMBUS
RESET
LM3S2D93-IQC80
LQFP 100P
UART1
I2C0
AMC MMC
LCD Control
MCU SPI0
SOC Bootmode GPIO
From SOC UART0 TX
Power for MCU
Buget 150mA
[Note]1.D3, D5 should be placed on edge of PCB.
2.D4, D6 should be placed inside of PCB.
Note:LED Color is RED
Note:LED Color is GREEN
Note:LED Color is RED
Note:LED Color is BLUE
Attention
Power RESET
WAKE
MCU_RESET
Note:PUSH Buttons Color is BLACK
Note:PUSH Buttons Color is RED
[Note]RST_MCU1 should be placed inside of PCB
Note:PUSH Buttons Color is BLACK
Designed for TI by ADVANTECH
TEXAS INSTRUMENTS
ADVANTECH
Title
MCU LM3S2D93
Size C
Document Number K2EVM-HK
Rev A103
Date: Thursday, May 30, 2013
Sheet 36 of 43

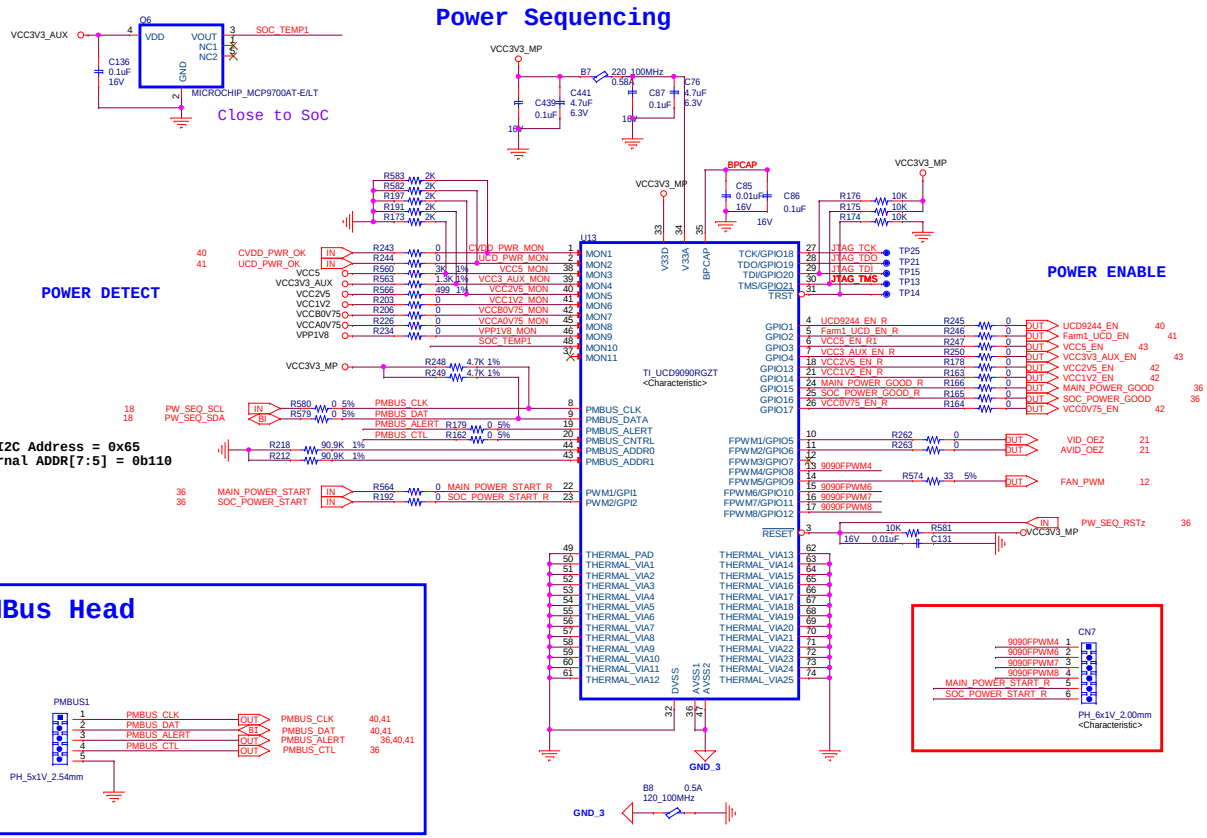
MCU JTAG



MCU UART



Power Sequencing



PMBus Head

PMBus Address Bins

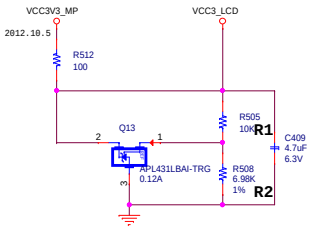
PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

Designed for TI by ADVANTECH

Title: MCU MISC

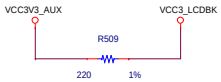
Size: C | Document Number: K2EVM-HK | Rev: A103

Date: Thursday, May 30, 2013 | Sheet 37 of 43

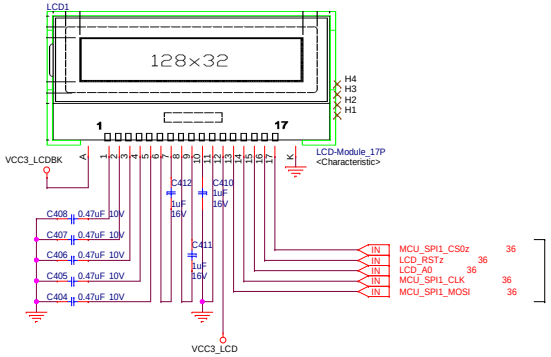


VO = 1.24v(1+R1/R2)+0.15uA*R1

3.018V =1.24 (1+10k/6.98k)+0.15u*10k



NHD-C12832A1Z-FSB-FBW-3V3



SPI1 CS0
LCD control

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

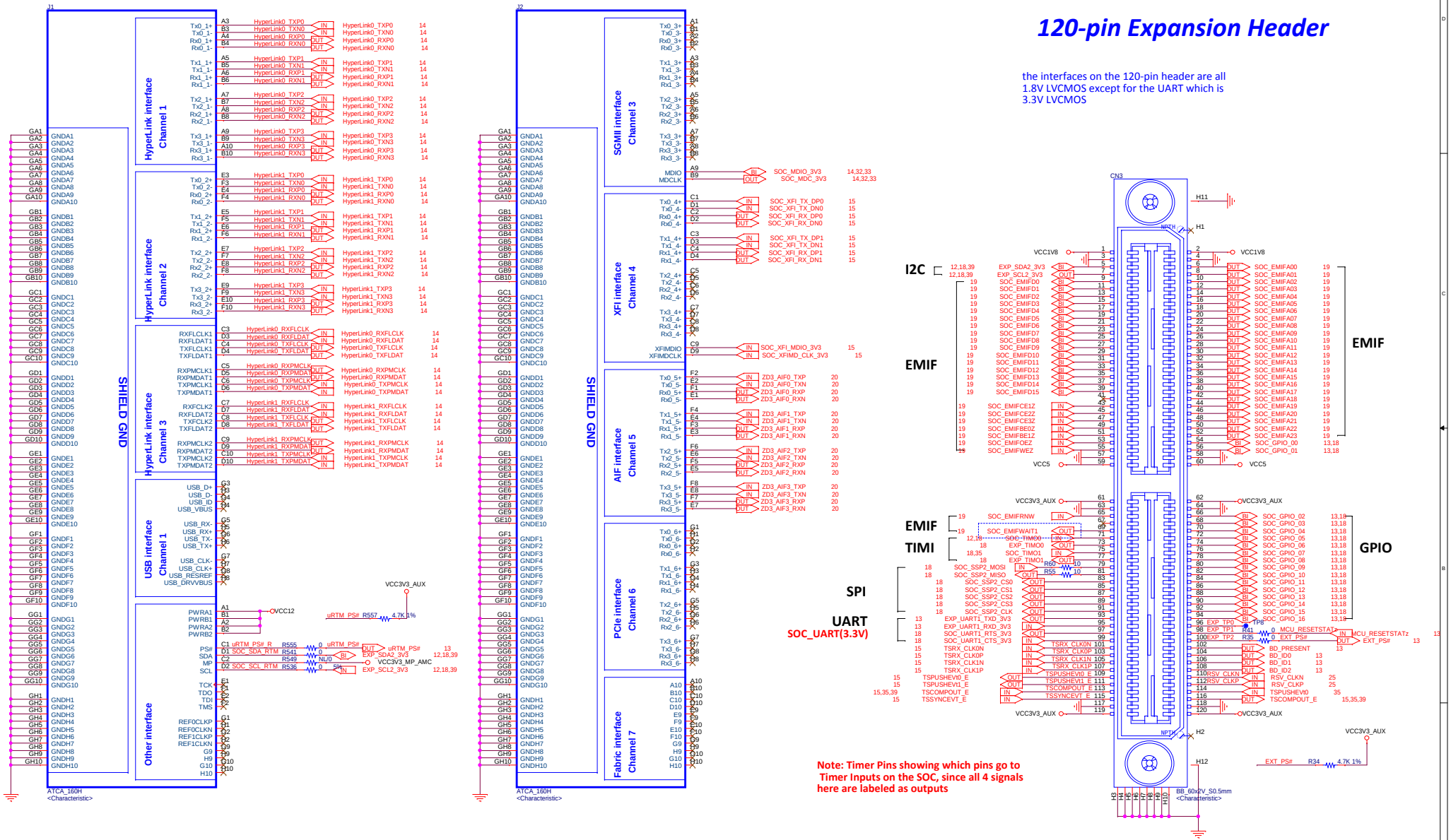
Title		
	MCU LCD	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 38 of 43	

Note : J1 connector close to AMC Interface.

Note : J2 connector close to Key socket.

120-pin Expansion Header

the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

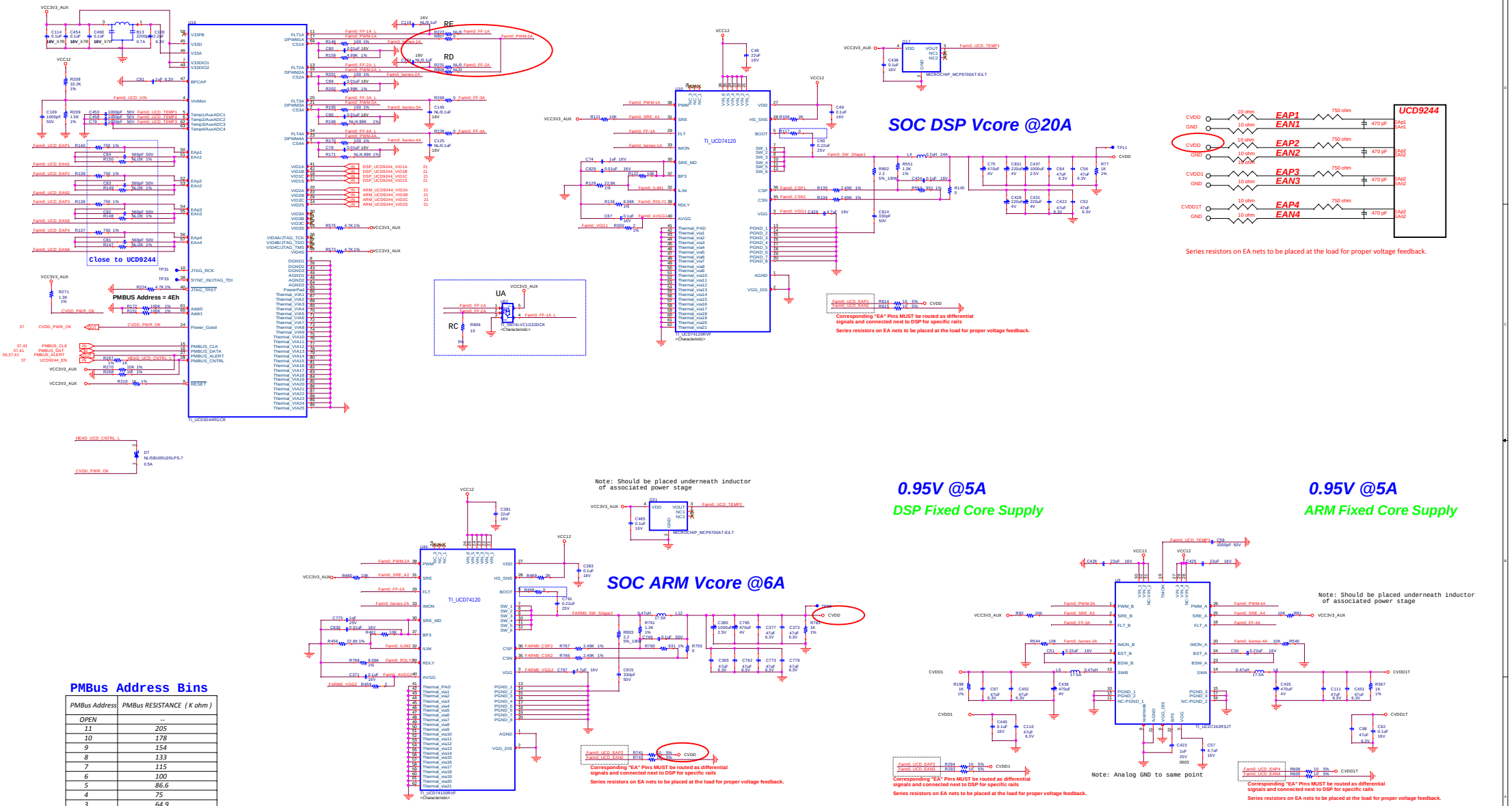


Note: Timer Pins showing which pins go to Timer Inputs on the SOC, since all 4 signals here are labeled as outputs

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title	mTCA_ZD3/120-pin Expansion	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 39 of 43	



PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

Designed for TI by ADVANTECH

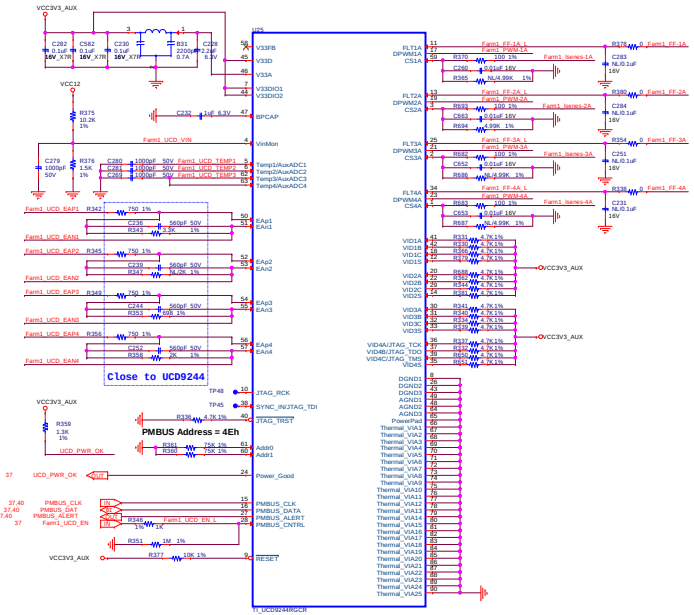
DSPM-6305E

TEXAS INSTRUMENTS ADVANTECH

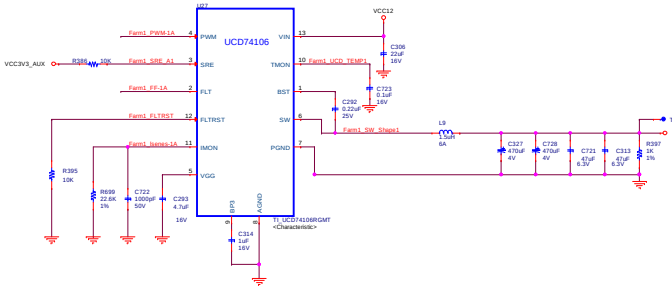
Title: Smart_Reflex AVS

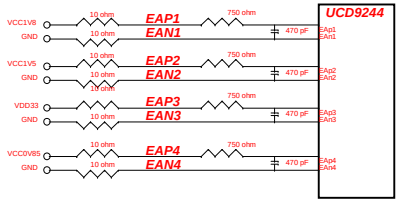
Size	Document Number	Rev
D	K2EVM-HK	A103

Date: Thursday, May 30, 2013 Sheet 40 of 43



PLL, 1.8V I/O and SERDES @5A





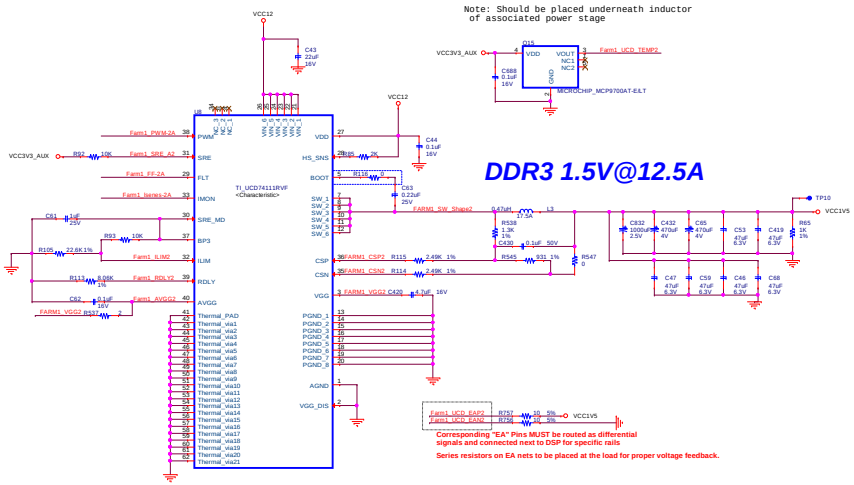
Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Series resistors on EA nets to be placed at the load for proper voltage feedback.

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--



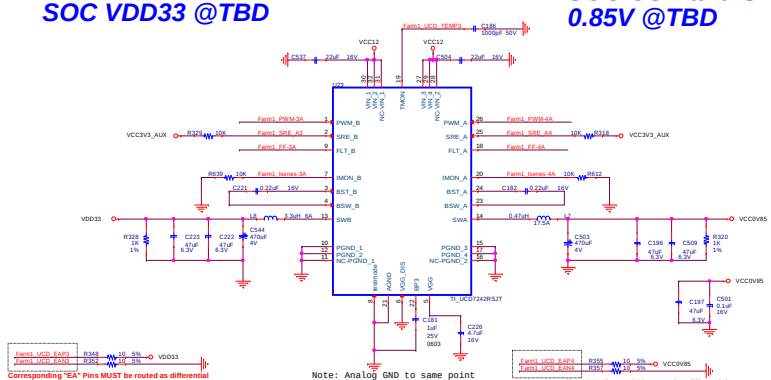
Note: Should be placed underneath inductor of associated power stage

DDR3 1.5V@12.5A

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

SOC VDD33 @TBD



SOC USB and SERDES 0.85V @TBD

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

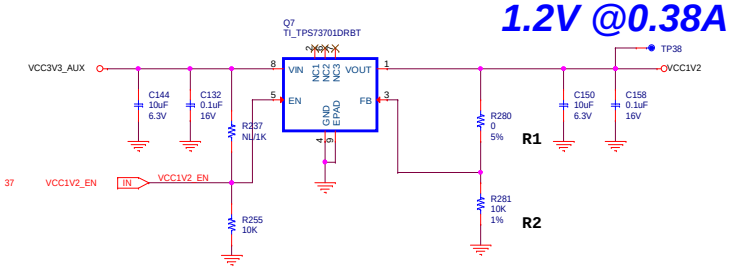
Title: Smart_Reflex VDD33/1.8V/1.5V/0.85V

Size	Document Number	Rev
D	K2EVM-HK	A103

Date: Thursday, May 30, 2013 Sheet 41 of 43

VCC1V2

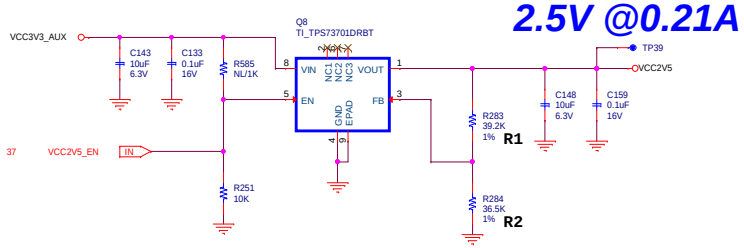
1.2V @0.38A



Vout=(R1+R2)/R2*1.204
1.204V = (0+10k)/10k*1.204

VCC2V5

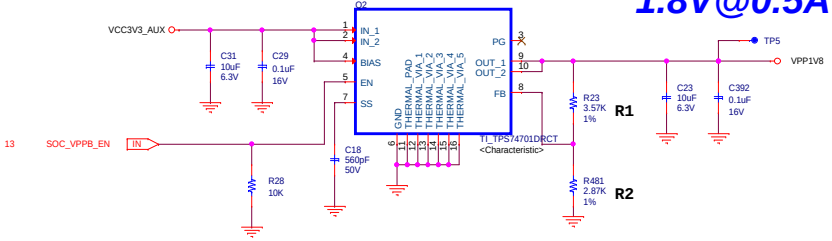
2.5V @0.21A



Vout=(R1+R2)/R2*1.204
2.50V =(39.2k+36.5k)/36.5k*1.204

VPP1V8

1.8V@0.5A

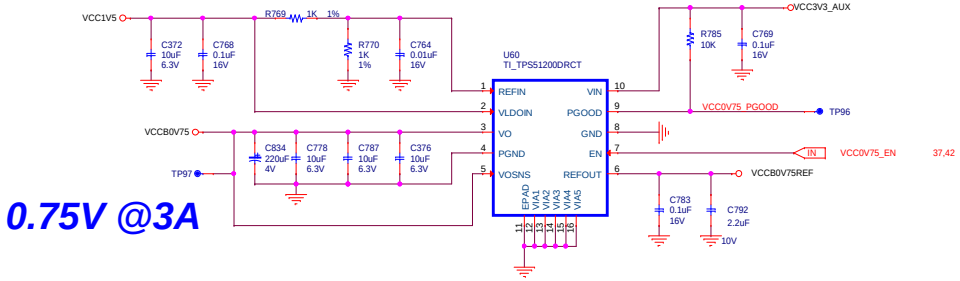


Vout=0.8*(1+R1/R2)

1.79512V =0.8*(1+3.57k/2.87k)

VCCB0V75

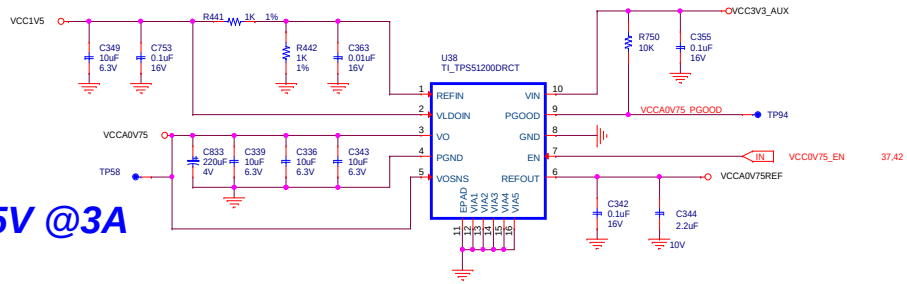
DDR3-1600
DiscreteSDRAM ArrayI



0.75V @3A

VCCA0V75

For DDR3-1600 SO-DIMM



0.75V @3A

Designed for TI by ADVANTECH
DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

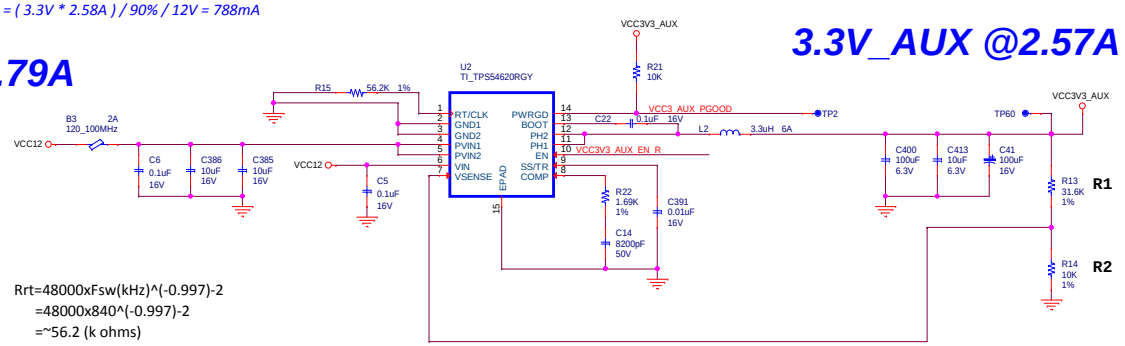
Title	Power_1.2V/2.5V/0.75V/1.8V	
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 42 of 43	

VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.57A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x840^(-0.997)-2
=~56.2 (k ohms)

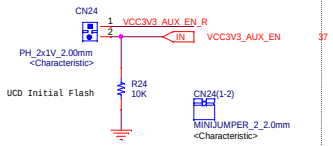
Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*3/(840kHz*0.0825)
Cout=~87uF

Reference Capacitor=100uF

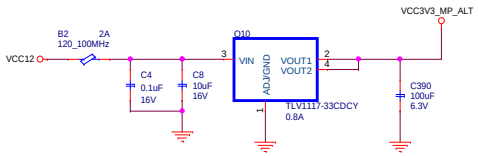
(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3A * 0.3) * (3.3 / (12 * 840kHz))
L = 9.67 * 0.33u
L = ~3.2 uH

Reference Inductor 3.3uH



VCC3V3_MP_ALT

3.3V_MP@150mA



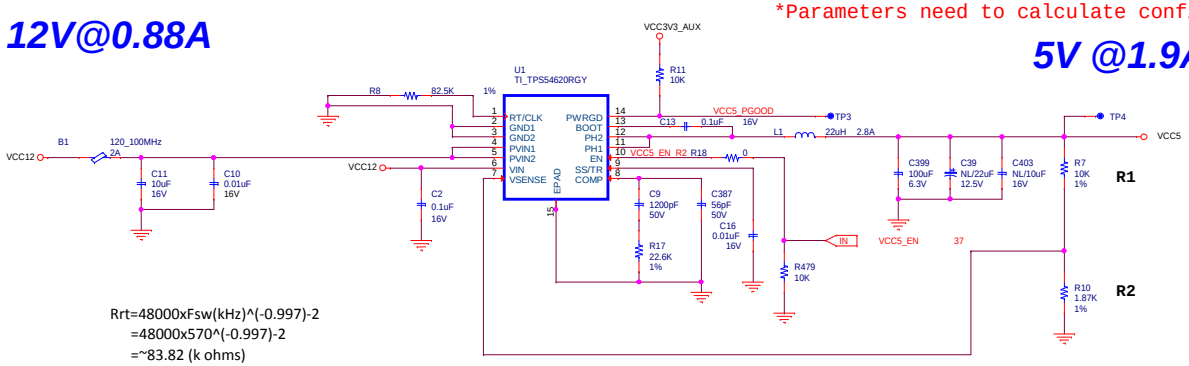
VCC5

Assume 90% Pe,
*Iin = (5V * 1.9A) / 90% / 12V = 880mA*

12V@0.88A

*Parameters need to calculate confirm

5V @1.9A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x570^(-0.997)-2
=~83.82 (k ohms)

Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2/(570kHz*0.125)
Cout=~56.14uF

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 5)/(2.3A * 0.3) * (5 / (12 * 570kHz))
L = 10 * 0.73u
L = ~7.3 uH

Reference Inductor 22uH

Designed for TI by ADVANTECH DSPM-8305E

Texas Instruments ADVANTECH

Title		
Power_VCC5 / VCC3V3_AUX/MP_ALT		
Size C	Document Number K2EVM-HK	Rev A103
Date: Thursday, May 30, 2013	Sheet 43 of 43	