A Keystone 2 EVM Board for TI

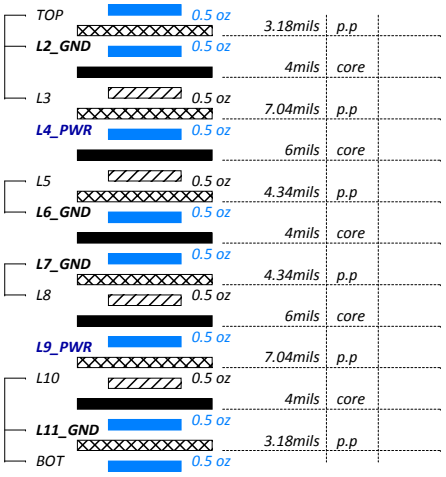
Product name : K2EVM-HK

Rev. A102-1

PCB PN :

Project Code :

PCB Thickness : 63 mils(1.6mm)
12 Layers



NOTE: TI Information – Selective Disclosure

NOTE: EVM design supports multiple devices. Check your device datasheet to determine if a given functionality is supported.

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title			
COVER PAGE			
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K2EVM-HK Revision Table

K2EVM-HK Rev 102-1 (Rev1 / PCB- 19C2830501-01)

Item	Description	Page
1	Stuff R287,R279 to 150 ohm for PCIECLKP/N_M Output Issue	Page.21
2	Cgange R30 value 10 ohm to 56 ohm for LED lightness Cgange R110,R492 value 10 ohm to 120 ohm for LED lightness	Page.36
3	U29 (TI_DAC8550IBDGKT) Change VDD Power Source VCC5 to VCC3V3_AUX Stuff R392 for DAC8550IBDGKT VREF	Page.25
4	R117, R468, R116 changes to 10 ohm for Reduce switching noise on CVDD/CVDD1/CVDDT	Page.40,41
5	Cgange R70 value 10 ohm to 56 ohm for LED lightness	Page.18
6	R586,R409,R611,R317 resistors change 100K to 0 ohm for I2C signal integrity	Page.18
7	Cgange R509 value 12 ohm to 220 ohm for Backlight lightness	Page.38
8	Change C32 33 pf to 10 pf for JTAG ISSUE Add R793 ,C796,C797 close to SOC for SOC_CLK	Page.19
9	CN11,CN12,CN13 Rotation for external CLK Source input	Page.25,27
10	R737.1 & R738.1 link Net name lan0_led_link100 change to lan0_led_link1000 for LAN ISSUE	Page.32
11	VCC2P5 change to VCC2V5 for LAN LED ISSUE	Page.34
12	Add&Reserve R799/R800 4.7K-0402 resistors voltage divider to the actual VBUS pin on the USB connector.	Page.15
13	Add&Reserve R801for each PHY INT go to a separate GPIO	Page.13,32,33
14	Add REF5025AID for DAC correct reference voltage input circiut	Page.15
15	Recommend the following signals: SOC_PORZ (AK4), SOC_TRST (AD1), SOC_RESETz (AD2), RESETFULLz (AD3) to be each connected to three decoupling caps to GND as close as possible to Kepler SOC on pcb: 1nF , 10nF and 100nF. This to prevent invalid duration reset's to be asserted during system ESD stress via system ESD EM pulse.	Page.18,19
16	Add D13/D14/D15 TPD2EUSB30DRTR for USB3.0 TVS	Page.15
17	Changer D9,D11 Schottky diode for Power Drop	Page.36
18	Add C814, R802 for CVDD reduce switching noise. Add C815, R803 for CVDDT reduce switching noise.	Page.40
19	Add CN24 for UCD Initial Flash	Page.43
20	Add B48 bead for VDDUSB	Page.15
21	Change AVDDA15:6 bead for Space and add CAPs	Page.22
22	Add R804 and R805 for SW integration for LOCK == 1 becomes difficult.	Page.19
23	RST_MCU1 now located by USIM socket - since SW is moved 4" away, need to add a new 0.1uF(C827) cap to GND adjacent to U6.1 on net MCU_RESET_SWz.	Page.36
24	MCU JTAG header CN22 now located by USIM socket - since it is moved 4" away, add 10pF(C828) cap to GND adjacent to U4.2 on net BSC_JTAG_TCK.	Page.37
25	Add a small C829 and C830 0.01uF capacitor between pin37 and ground of U10 and U44	Page.40
26	On page 18 of the schematic U26 is not connected correctly. SOC_UART1_TXD_1V8 should be connected to the enable on pin 3 and SOC_GPIO_11 should be connected to the A signal on pin 1 (flagged by BillT last week).	Page.18

Item	Description	Page
27	Add C831 1000uf and change C437 to 1000uf from 470uf ;change C422/C431/C428 to 220uf from 47uf) Change C380 to 1000uf from 470uf	Page.40
28	Add C832 1000uf for VCC1V5	Page.41
29	VCCB0V75 buck CAPs: Add C834 220uf VCCA0V75 buck CAPs: Add C833 220uf	Page.42
30	SoC Socket holes link to GND	Page.34
31	NAND FLASH change to MT29F4G08ABBDAHC from _MT29F1G08ABBDAHC	Page.19
32	D1/D2 change to TPD4S012DRYR from PGB1010603	Page.31
33	Add R799 to 100 ohm for VBUS	Page.15
34	Change SN74LVC2G241DCUT to SN74LVC2G125DCUR from UU1	Page.18
35	Change location name from JUMPER1 to CN2(1-2) Change location name from JUMPER2 to CN8(2-3) Add CN9(1-2) for Bootselect feature	Page.36
36	Add R343 to 3.3Kohm for 1.8V monitor correct	Page.41
37	Change location name from JUMPER3 to CN24(1-2)	Page.43

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TEXAS INSTRUMENTS ADVANTECH

Title: K2EVM-HK Revision Table II

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TITLE & TABLE OF CONTENTS

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: TITLE & TABLE OF CONTENTS

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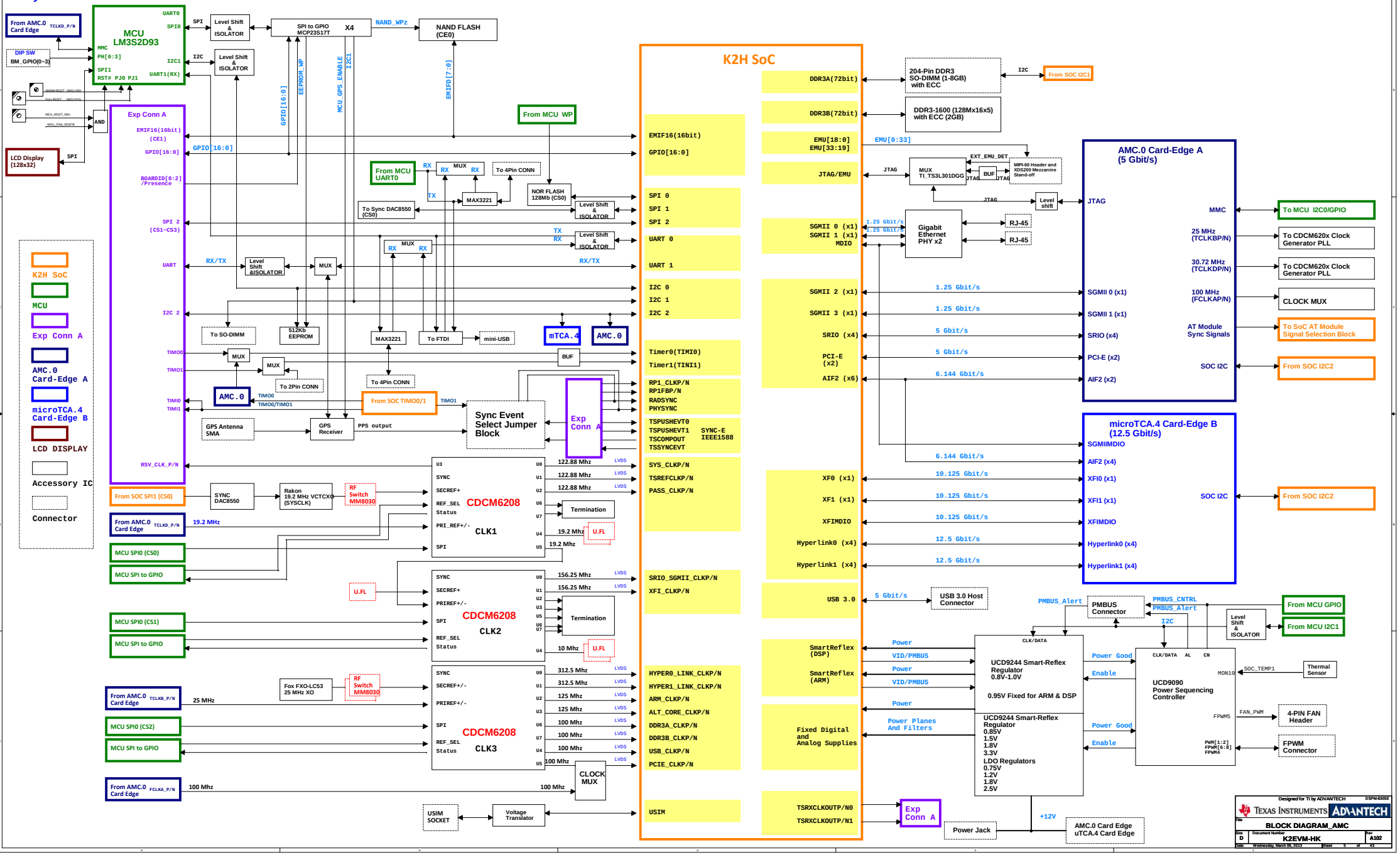
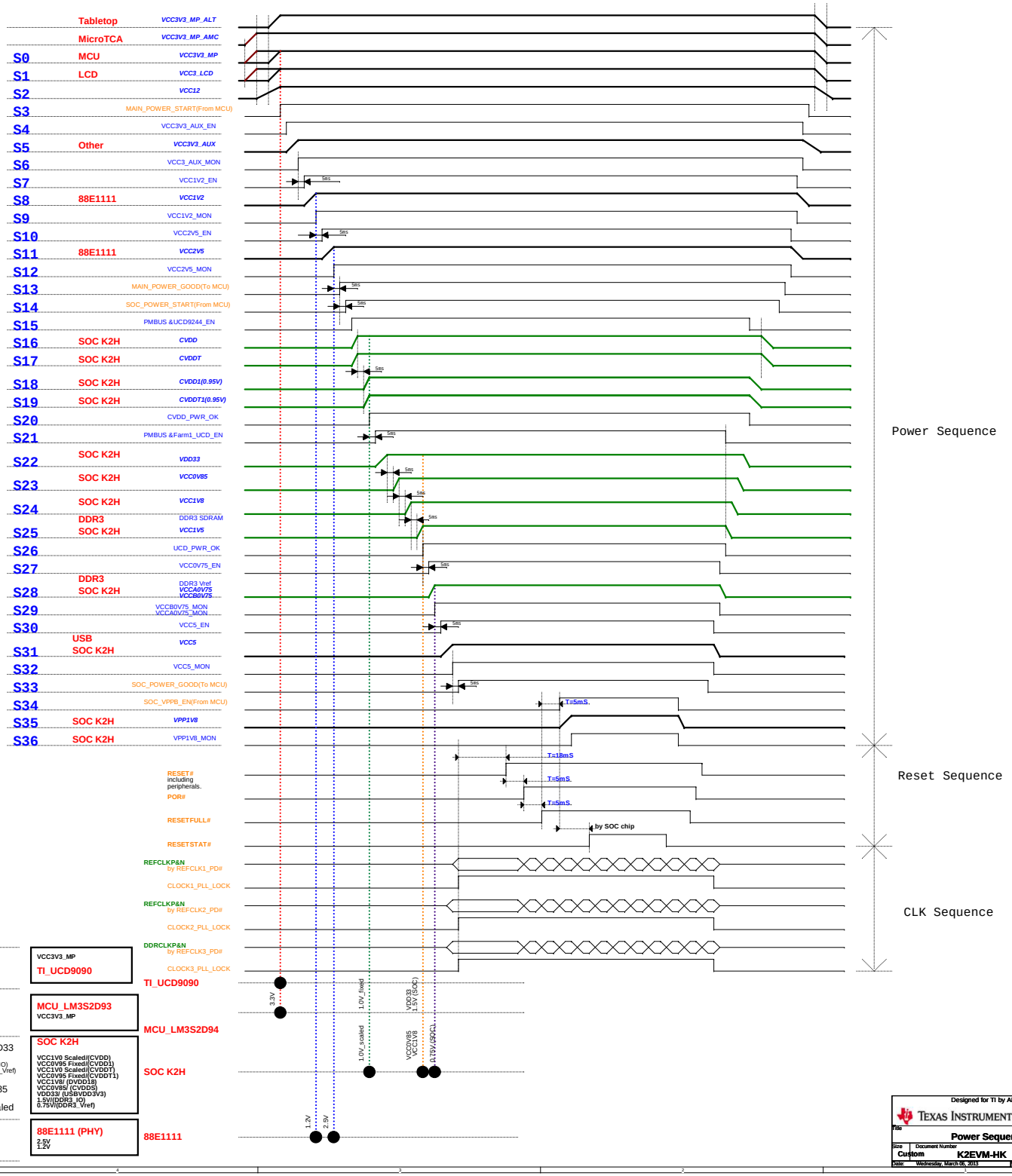
Keystone-2 EVM BLOCK DIAGRAM



Power Sequence

Has not been modify , wait TI provide document.



Ther is no specific power-up nor power-down sequence.

VCC3V3_MP
TI_UCD9090

TI_UCD9090

3.3V

Ther is no specific power-up nor power-down sequence.

MCU_LM3S2D93
VCC3V3_MP

MCU_LM3S2D94

When power on VCC_1V0 scaled → VCC_1V0 Fixed → VDD33 → VCC0V85 → VCC1V8 → 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref)

When power down 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref) → VCC1V8 → VCC0V85 → VDD33 → VCC_1V0 Fixed → VCC_1V0 scaled

SOC K2H

VCC1V0 Scaled/(CVDD)
VCC0V95 Fixed/(CVDD1)
VCC1V0 Scaled/(CVDDT)
VCC0V95 Fixed/(CVDDT1)
VCC1V8/ (DVDD18)
VCC0V85/ (CVDDS)
VDD33/ (USBVDD3V3)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

SOC K2H

1.0V_fixed
VDD33
1.5V (SOC)
1.0V_scaled
VCC0V85
VCC1V8
0.75V (SOC)

Ther is no specific power-up nor power-down sequence.

88E1111 (PHY)
2.5V
1.2V

88E1111

1.2V
2.5V

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DSPM-8355E

TEXAS INSTRUMENTS ADVANTECH

Title: Power Sequence

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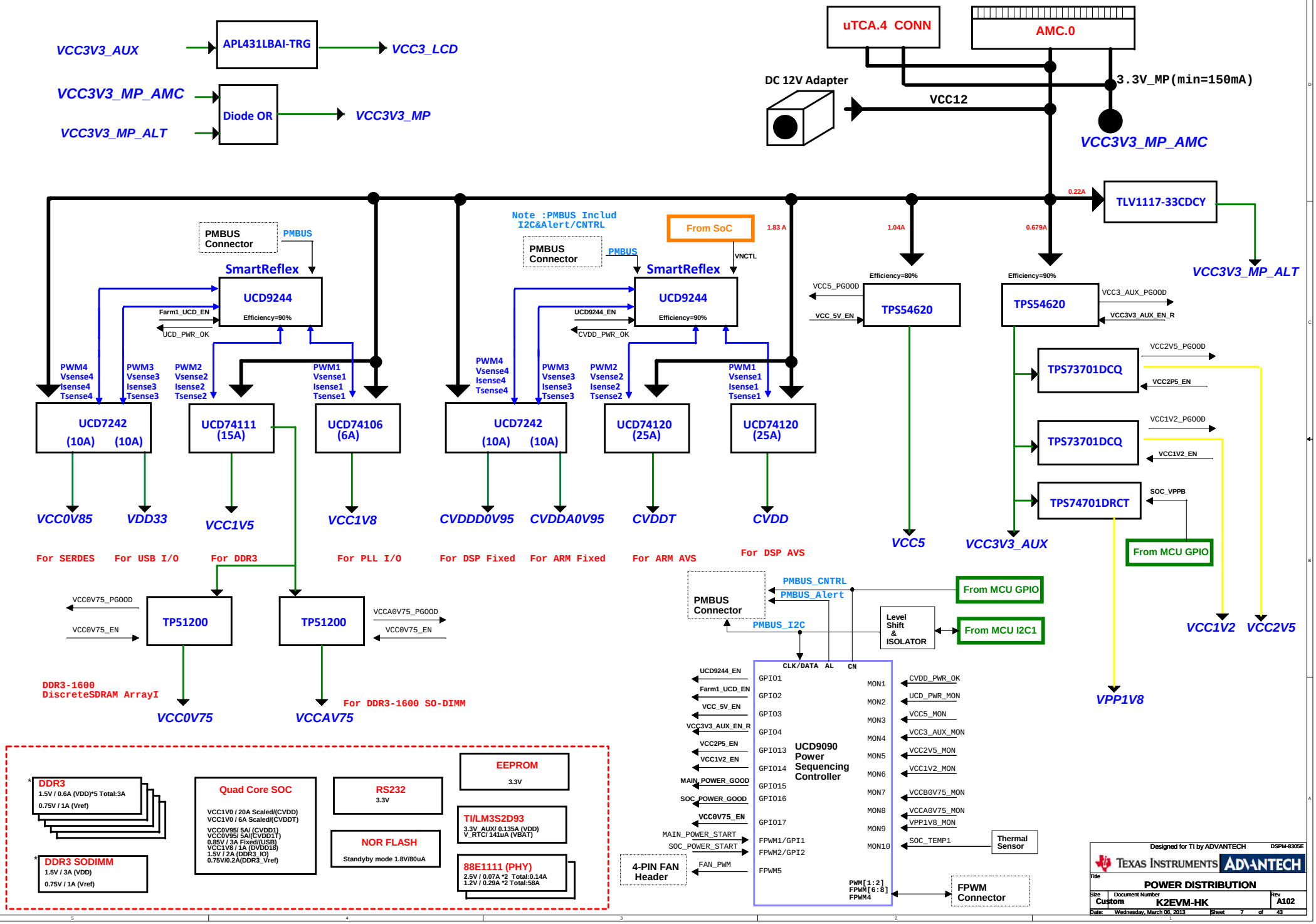
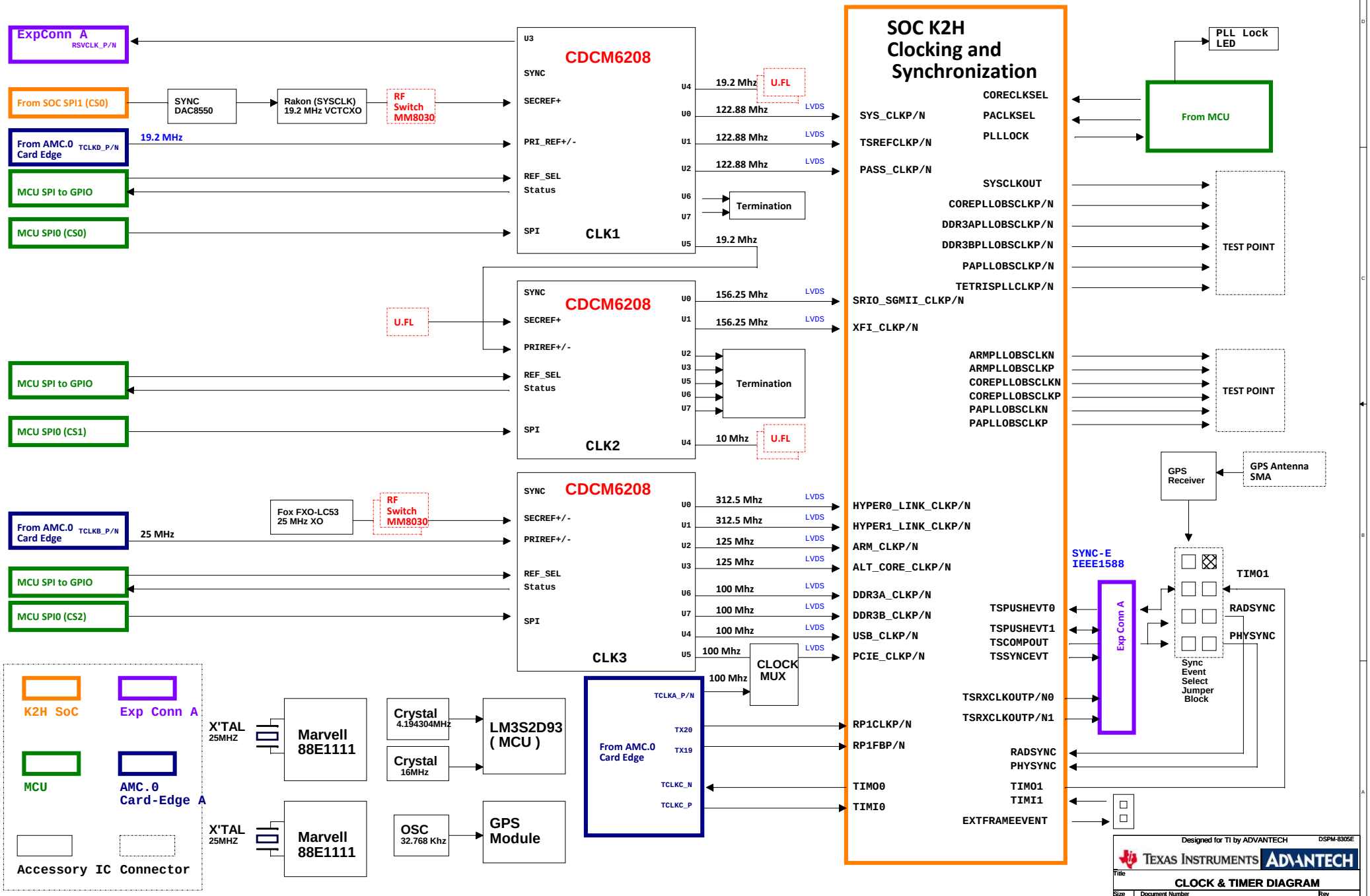
POWER DISTRIBUTION



CLOCK & TIMER DIAGRAM



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Title			
CLOCK & TIMER DIAGRAM			
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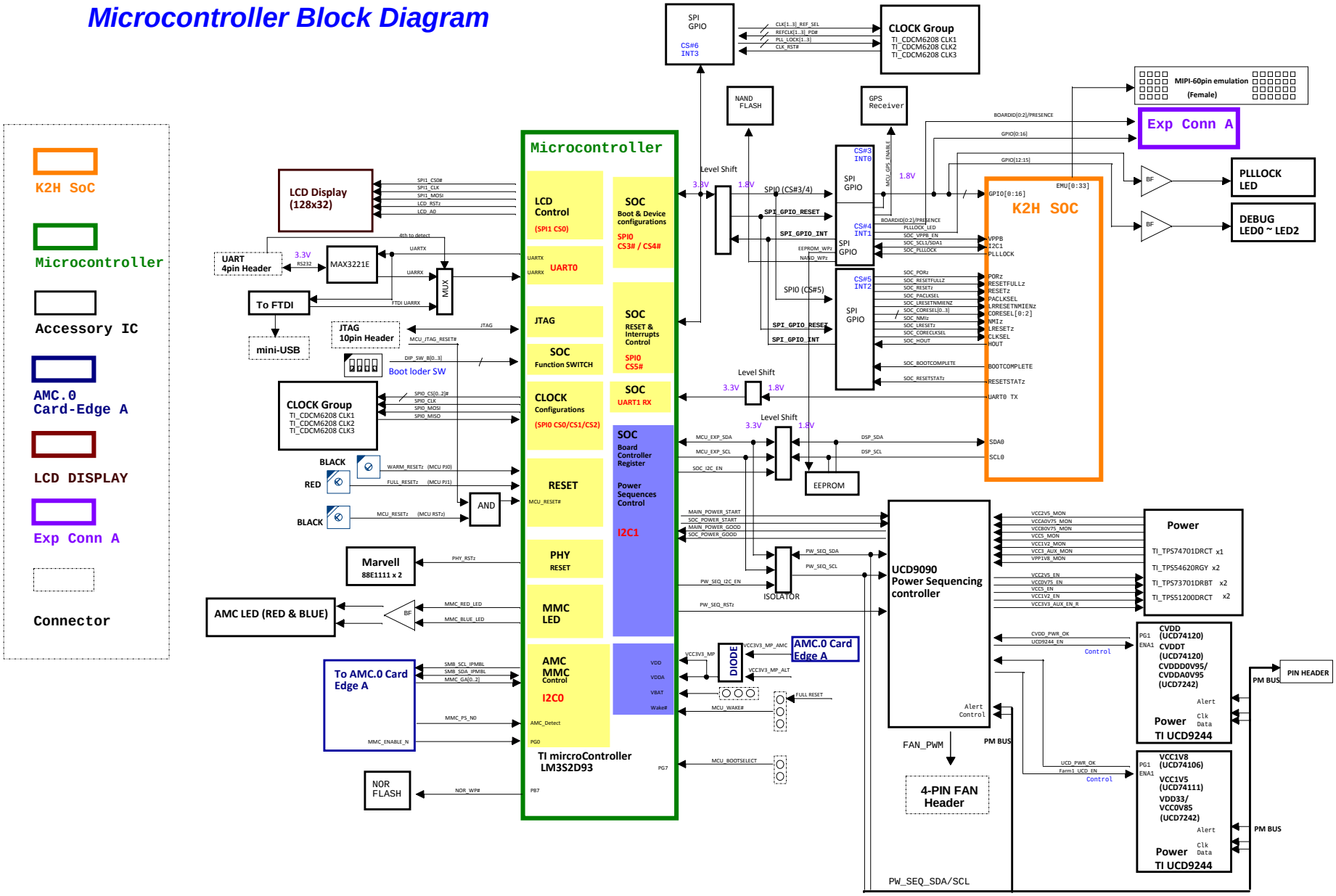
Microcontroller Block Diagram



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Title	Microcontroller Block Diagram	
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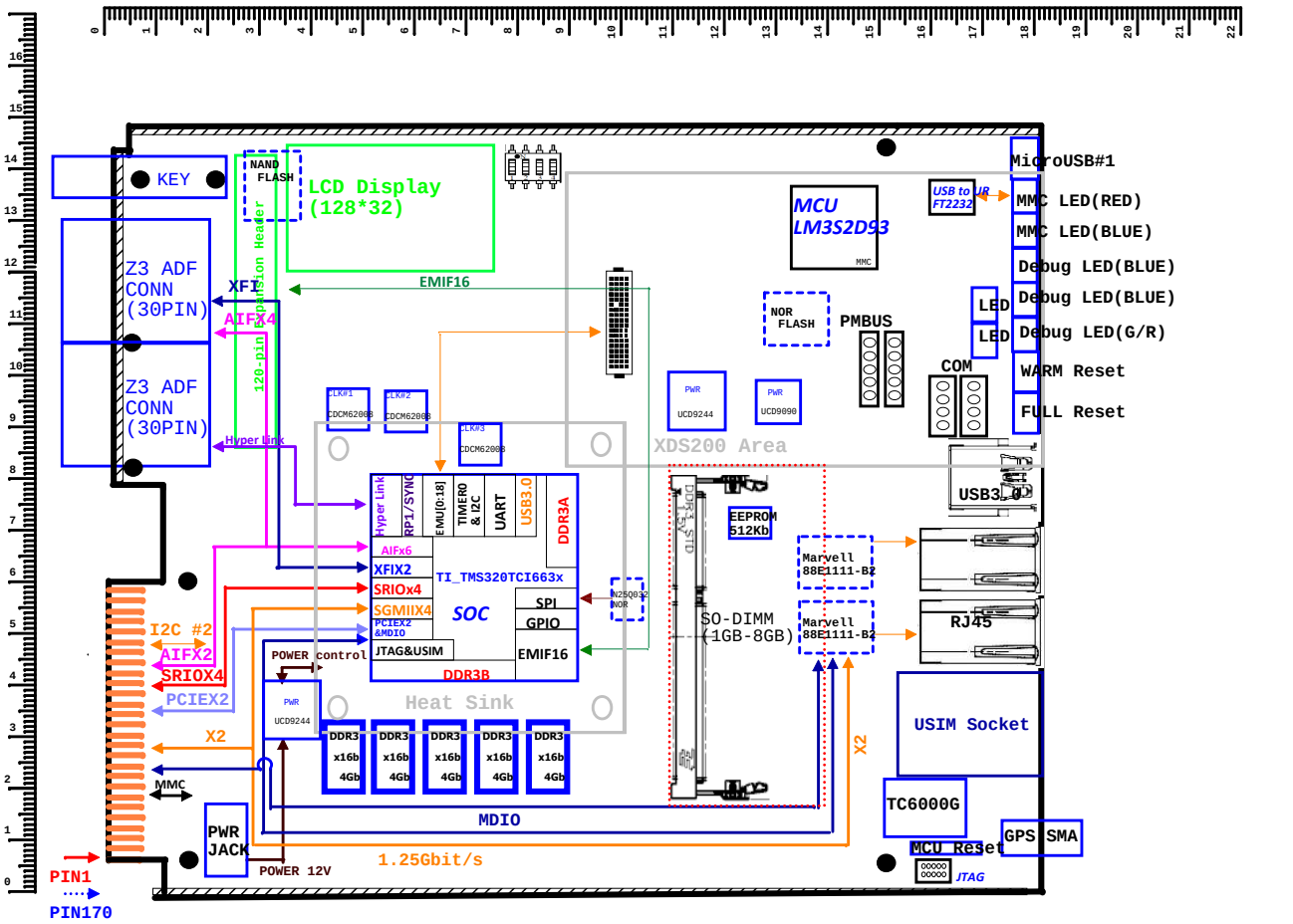
K2EVM-HK EVM PLACEMENT (TOP SIDE)



PCB Half Length = 181.5x148.5mm

Note: Dotted line is Bottom SIDE Component

Note: EVM with K2H device does not support XGMII

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Title			
K2EVM-HK Placement			
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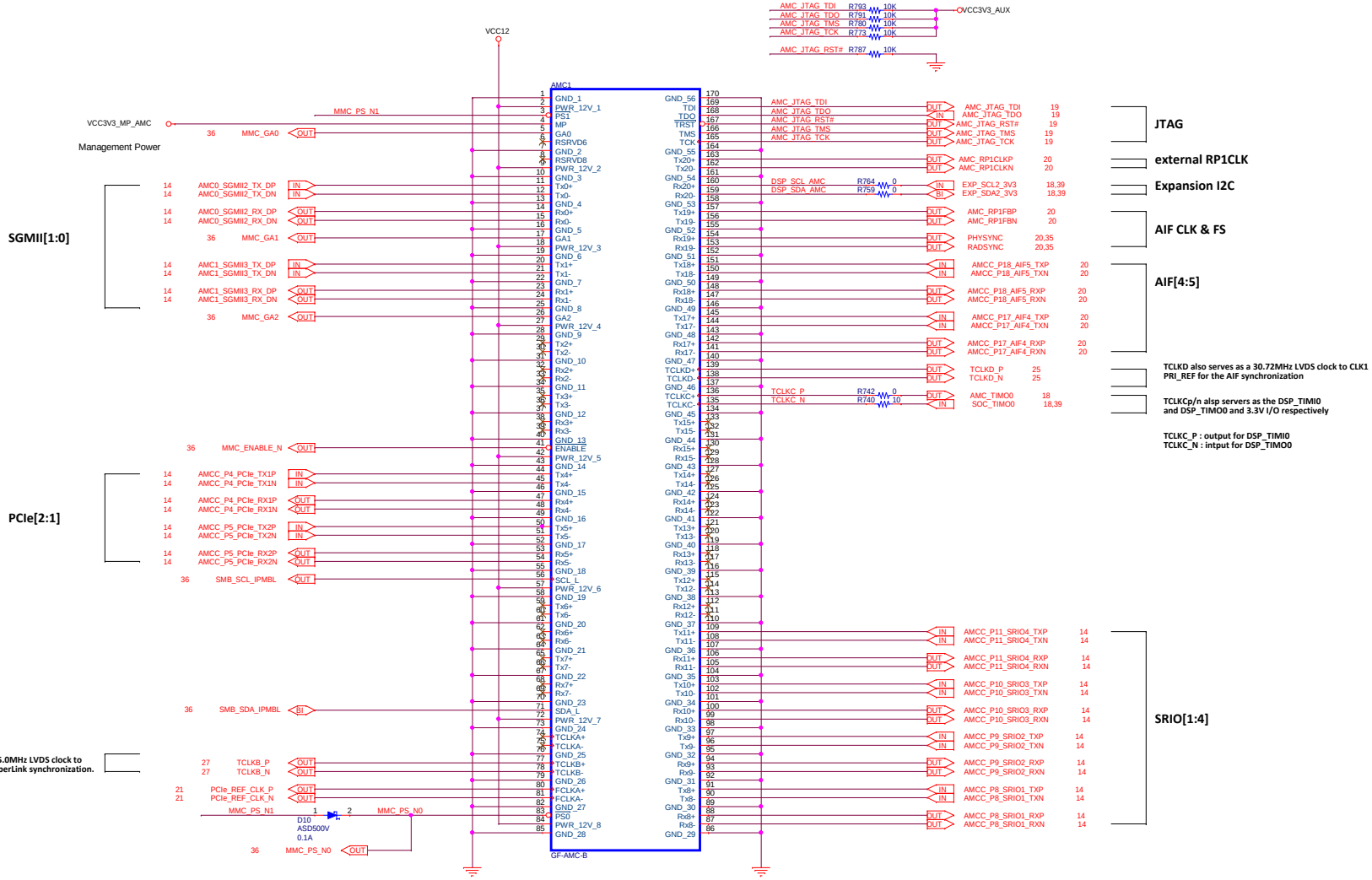
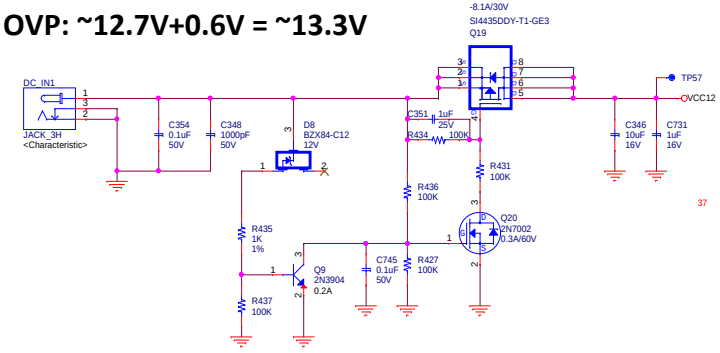
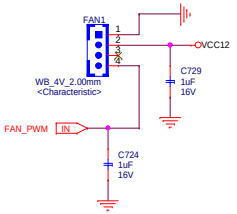


OVP: ~12.7V+0.6V = ~13.3V



DC FAN Connector for SOC



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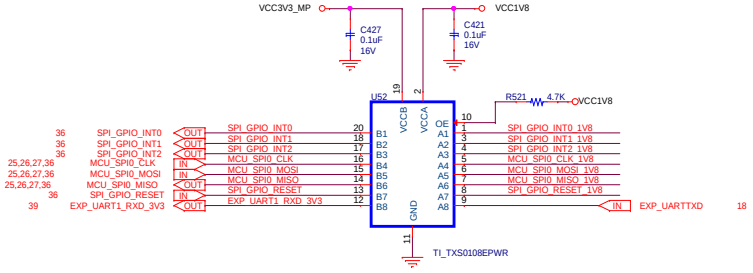
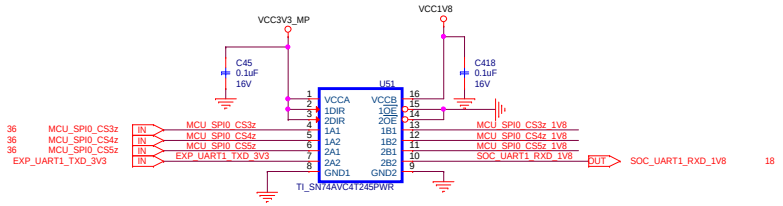
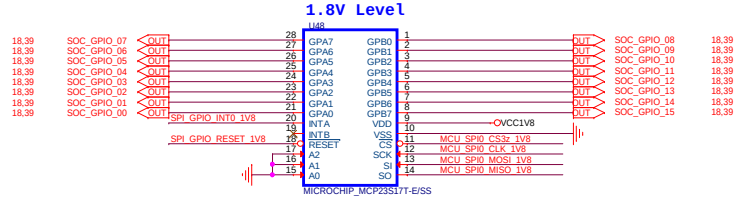
SPI level shift 3.3V <=> 1.8V



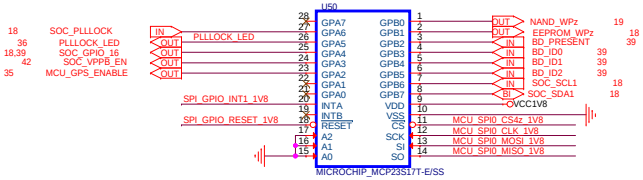


1.8V Level



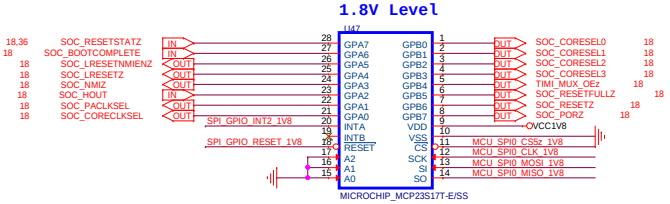
MicroChip SPI to GPIO

1.8V Level



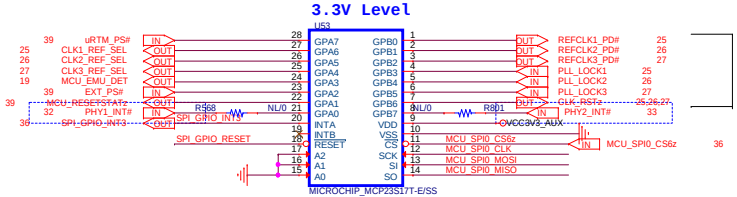
MicroChip SPI to GPIO

1.8V Level



MicroChip SPI to GPIO

3.3V Level



MicroChip SPI to GPIO

CDCM-620X Control

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Title			
SPI to GPIO Converter			
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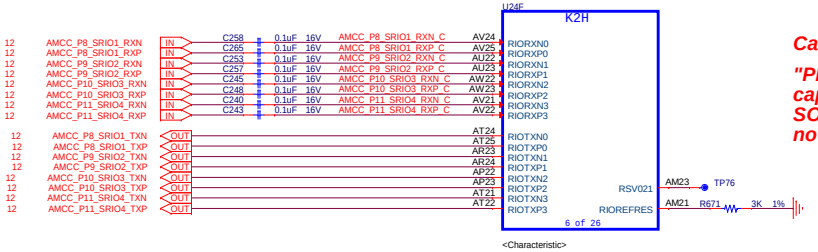
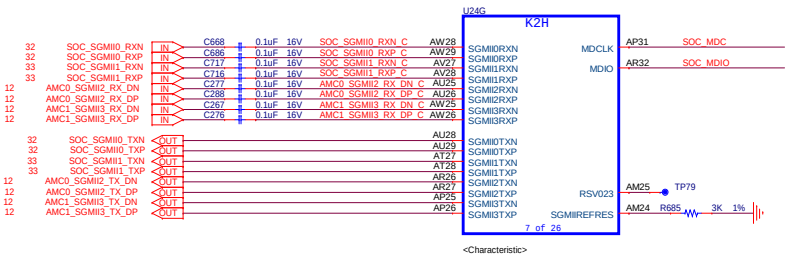
SRIO X4

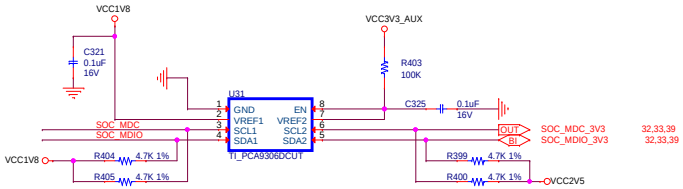


Caution!

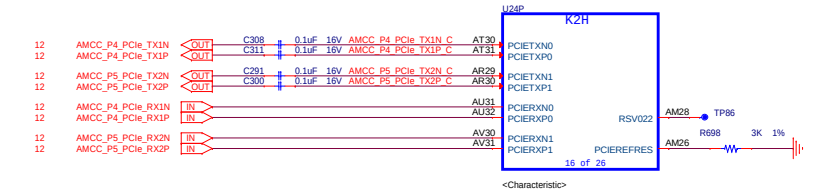
"Place ALL SRIO DC-blocking caps on top layer adjacent to the SOC's RX pins so that there are no additional vias"

SGMII X4





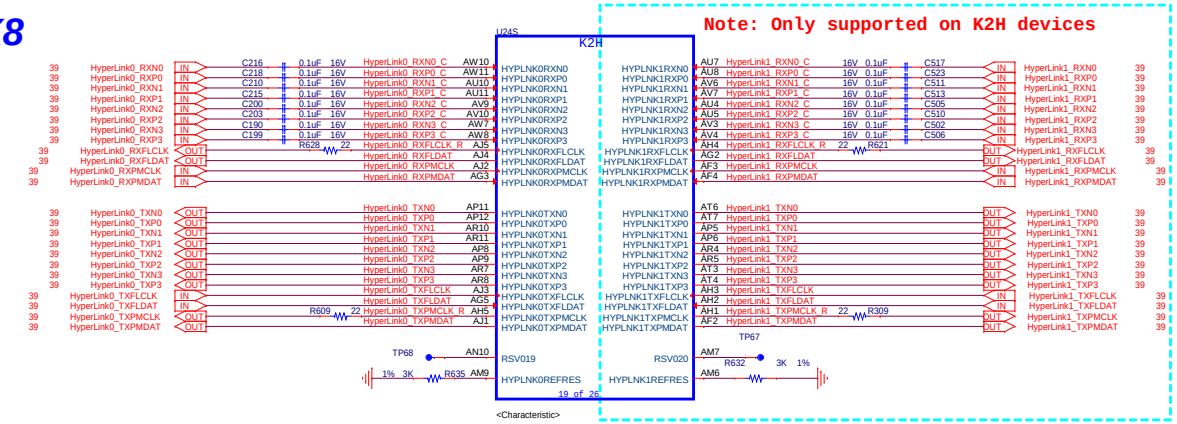
PCIE X2



Caution!

"Place ALL PCIe DC-blocking caps close to the TX pins"

HyperLink X8



Note: Only supported on K2H devices

"The HyperLink routes should have a maximum of 2 vias and no via stubs – All routes should be on the outer layer of the board."

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Title: **SOC_SERDES_PORTS**

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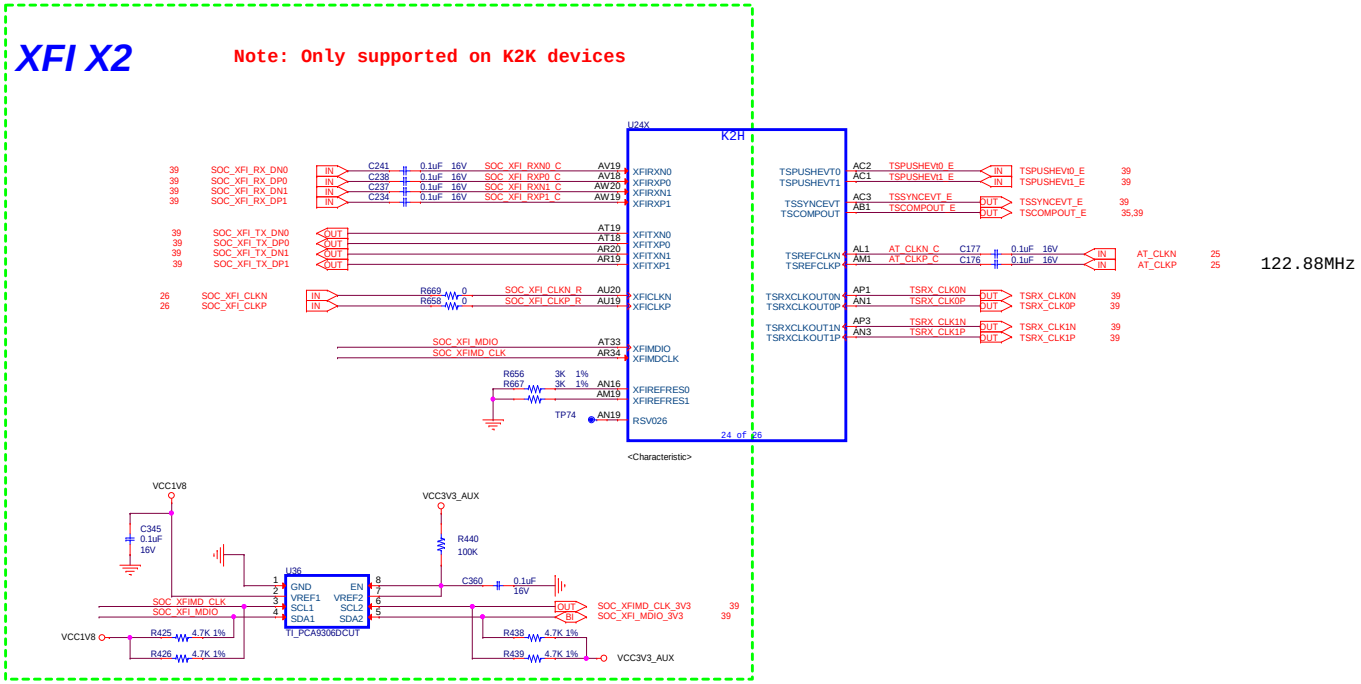
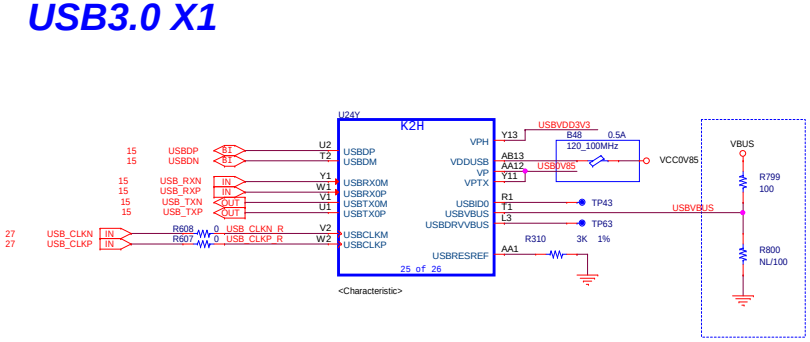
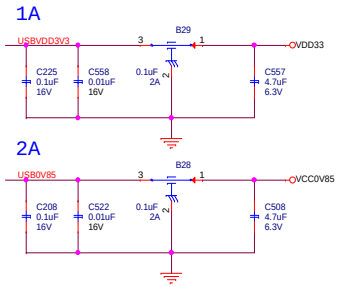
XFI X2

Note: Only supported on K2K devices

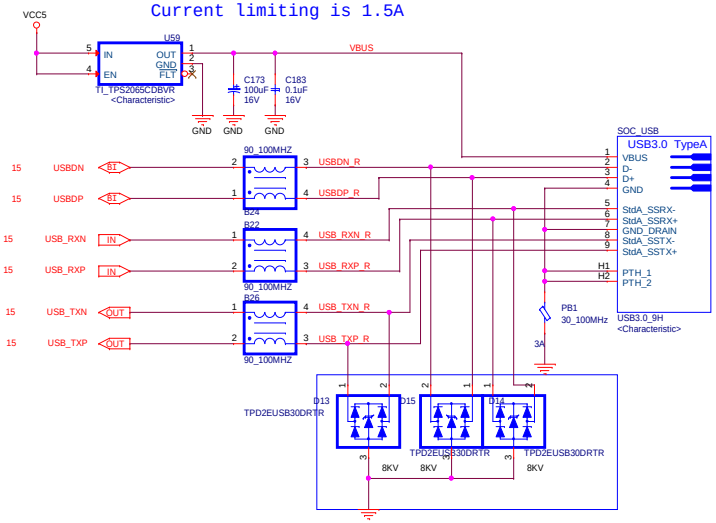


USB3.0 X1





Current limiting is 1.5A



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Title	SOC_XFI_USB	
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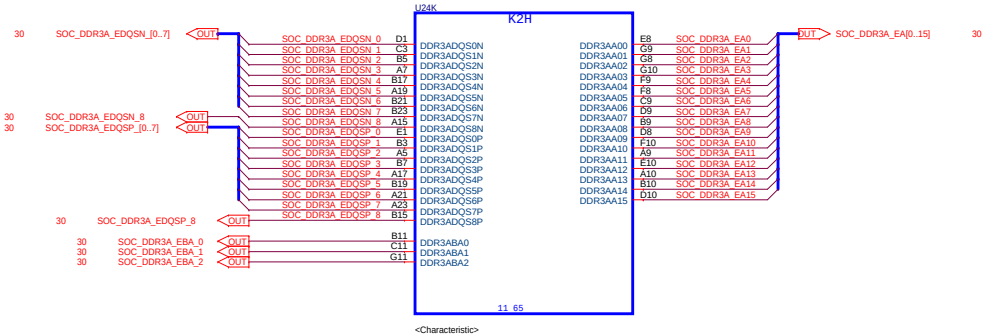

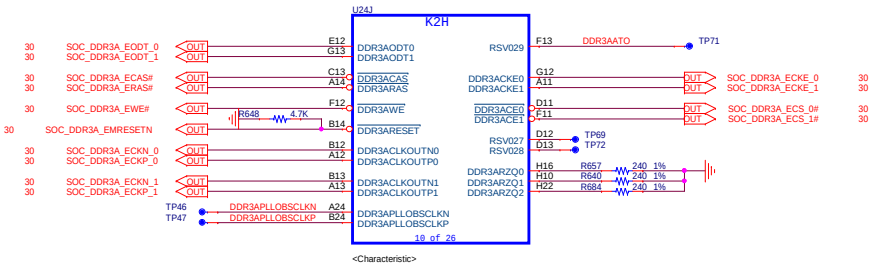

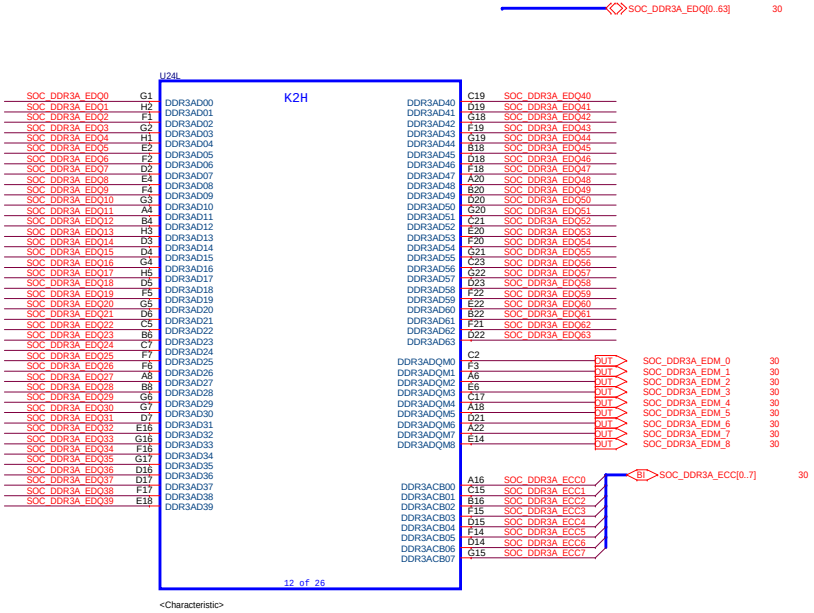

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Title

SOC_DDR3A

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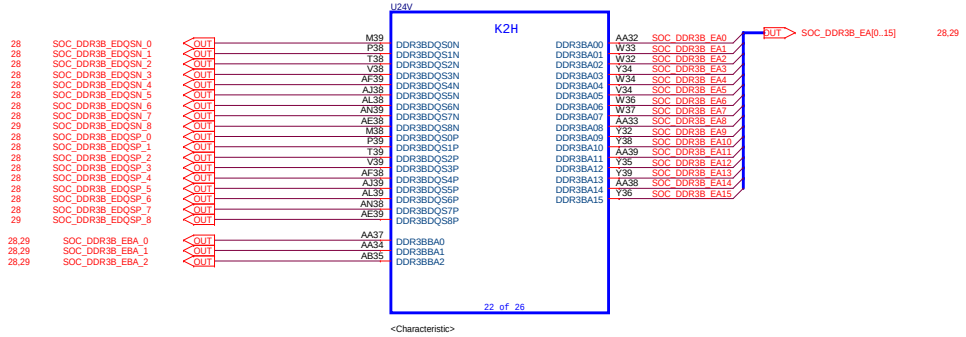
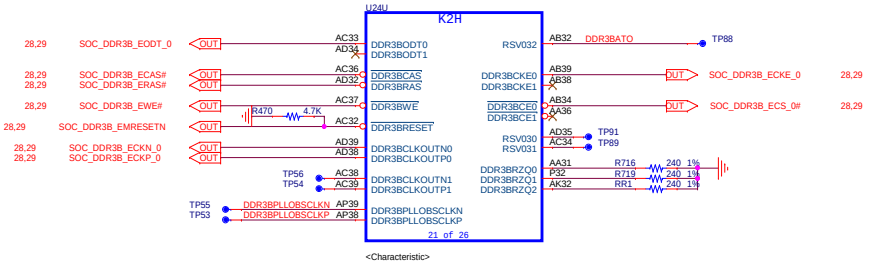
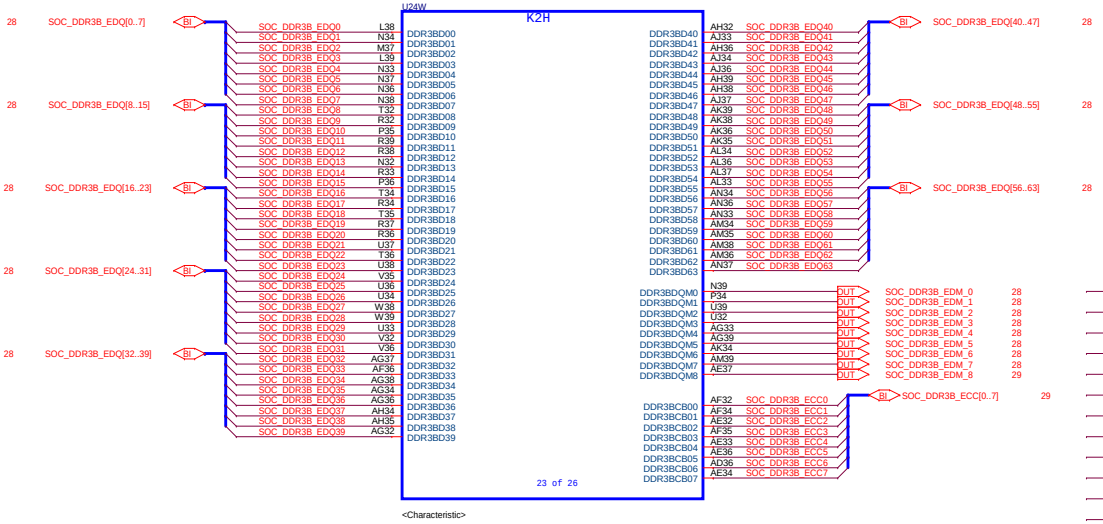
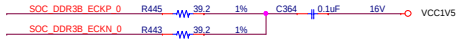
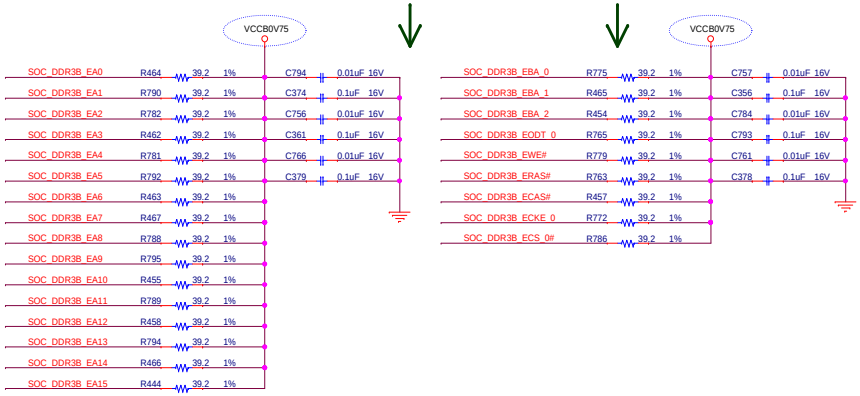








Place these resistors at the end of the trace.



Designed for TI by ADVANTECH

DSPM-8305E

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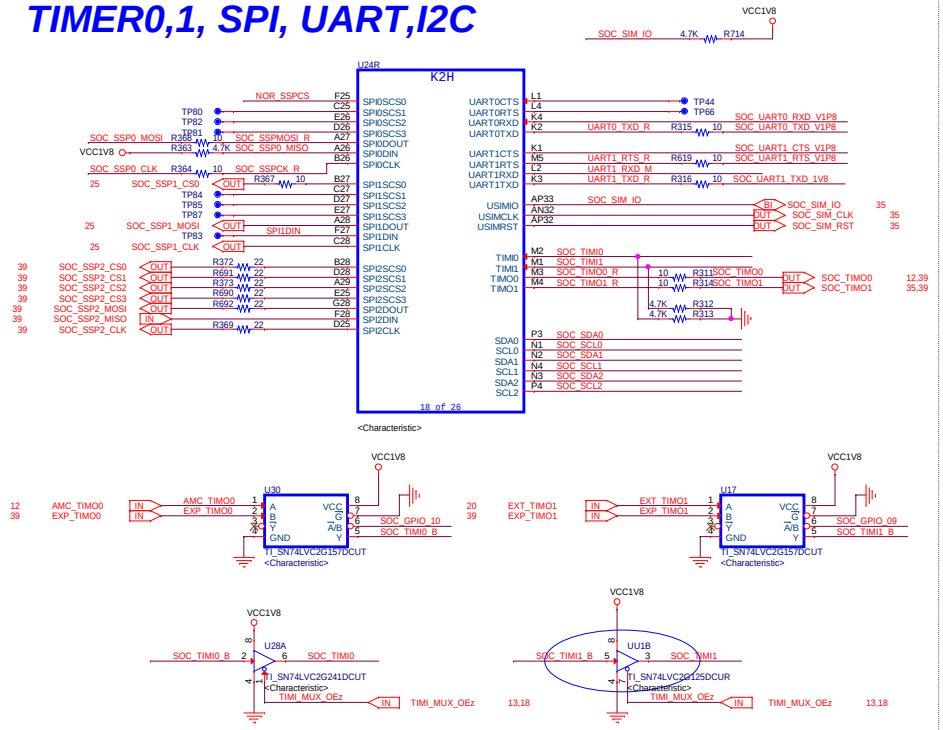
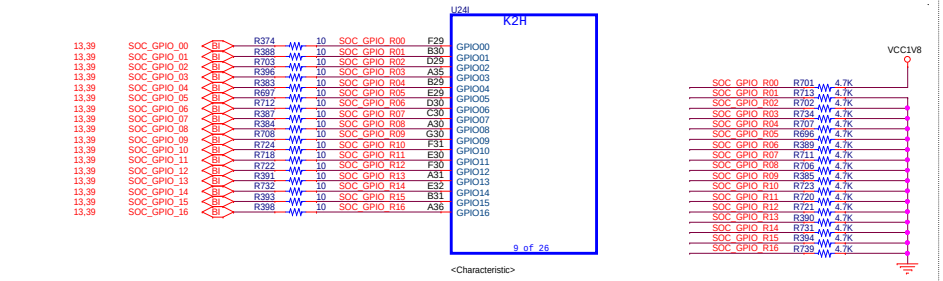
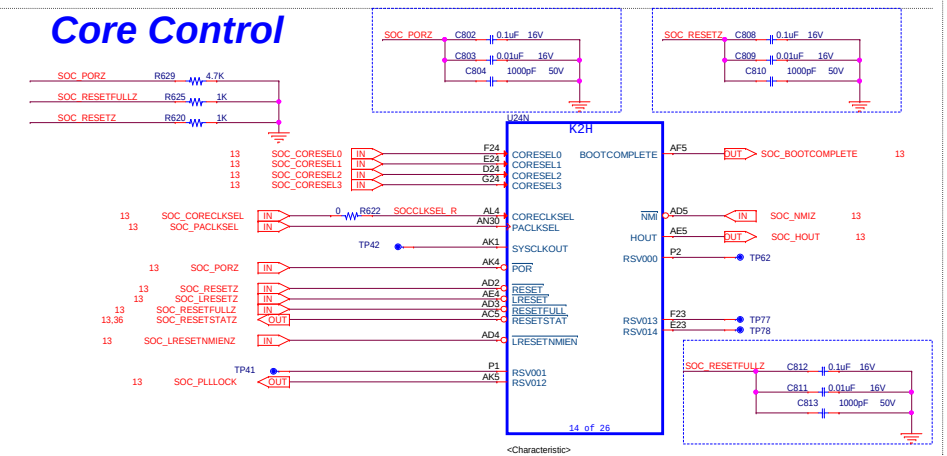
TIMER0,1, SPI, UART,I2C

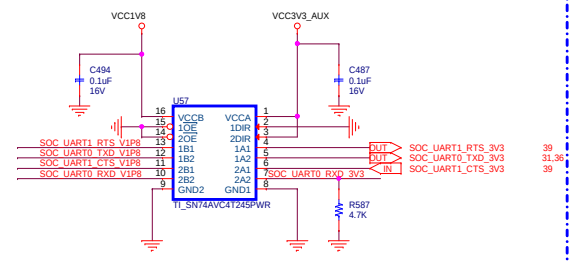


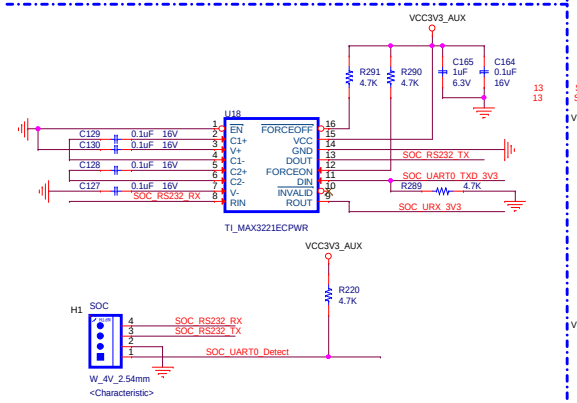
GPIO

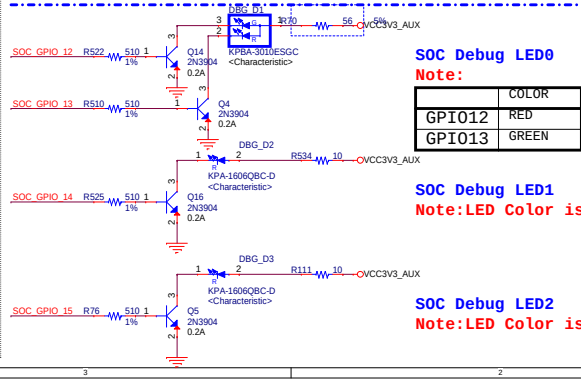


Core Control









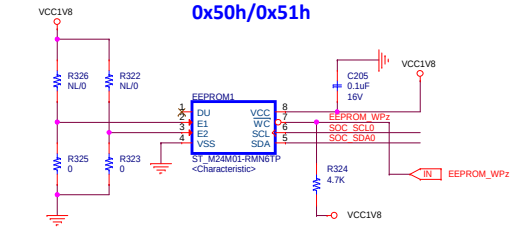
SOC Debug LED0
Note:

	COLOR
GPIO12	RED
GPIO13	GREEN

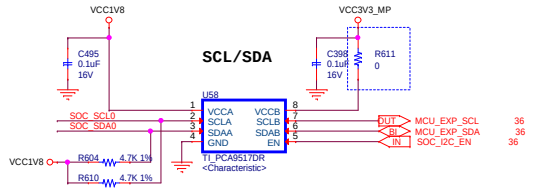
SOC Debug LED1
Note:LED Color is BLUE

SOC Debug LED2
Note:LED Color is BLUE

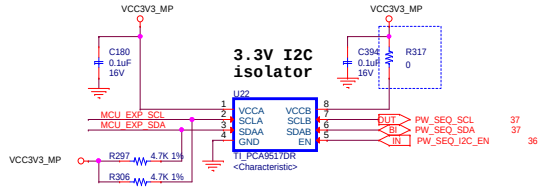
1M-bit I2C EEPROM 0x50h/0x51h



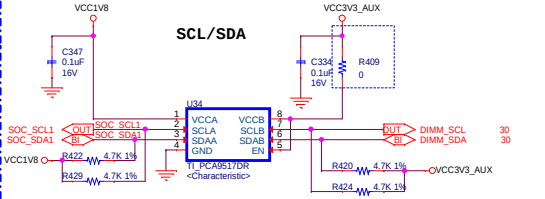
SCL/SDA



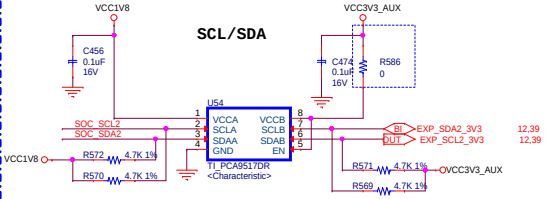
3.3V I2C isolator



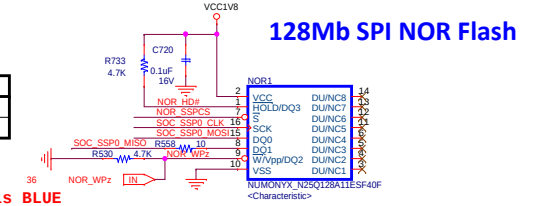
SCL/SDA



SCL/SDA



128Mb SPI NOR Flash



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TEXAS INSTRUMENTS ADVANTECH

Title	SOC_MISC	
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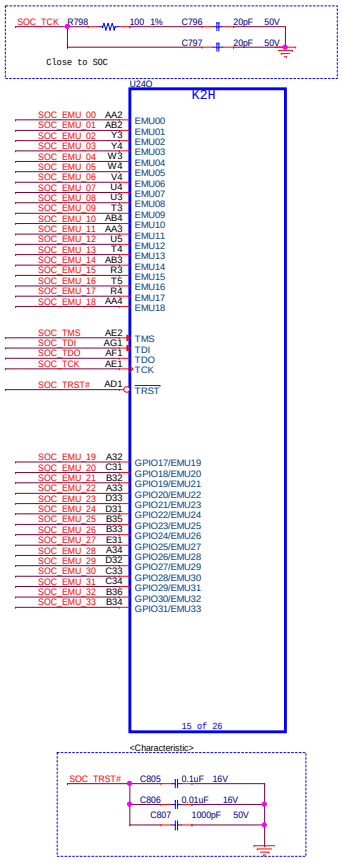
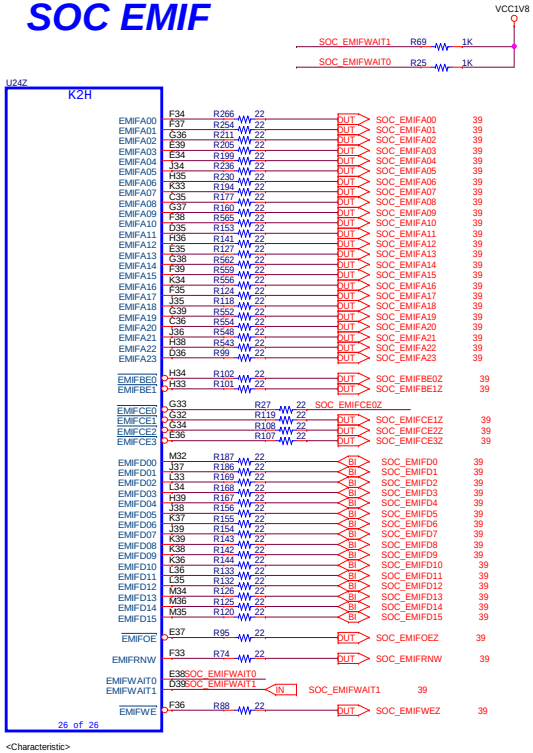
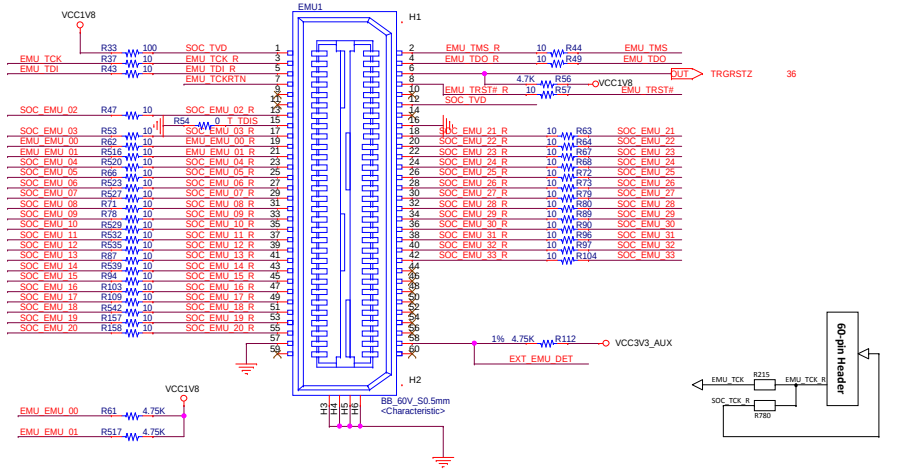
EMU & JTAG



SOC EMIF

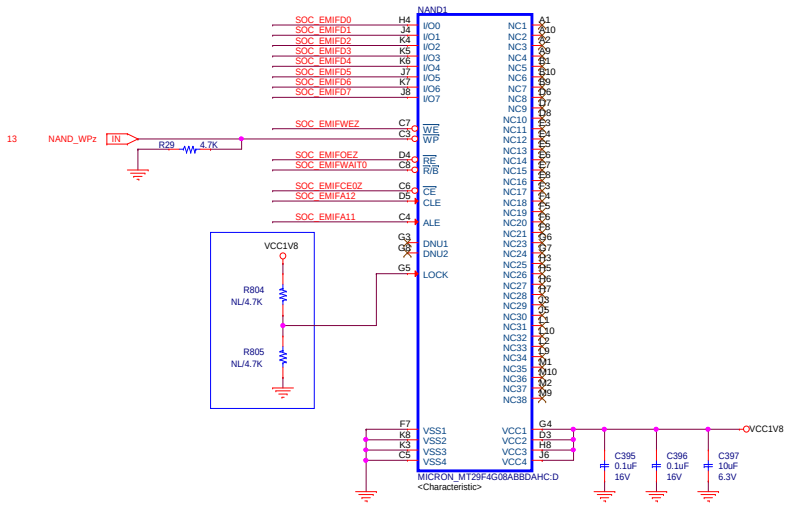


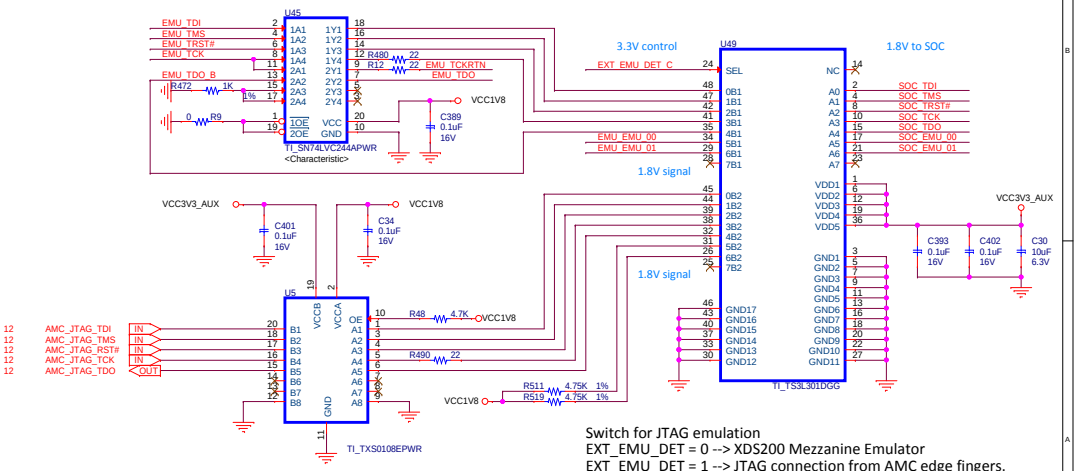
EMU CONN.



NAND FLASH

Note: NAND FLASH Device size is 4Gb.





Switch for JTAG emulation
EXT_EMU_DET = 0 --> XDS200 Mezzanine Emulator
EXT_EMU_DET = 1 --> JTAG connection from AMC edge fingers.

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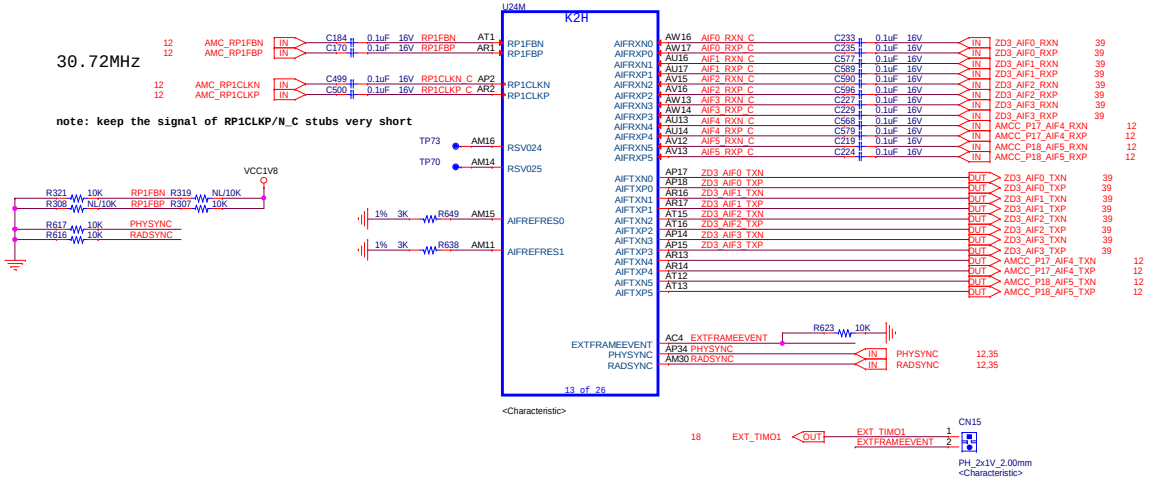
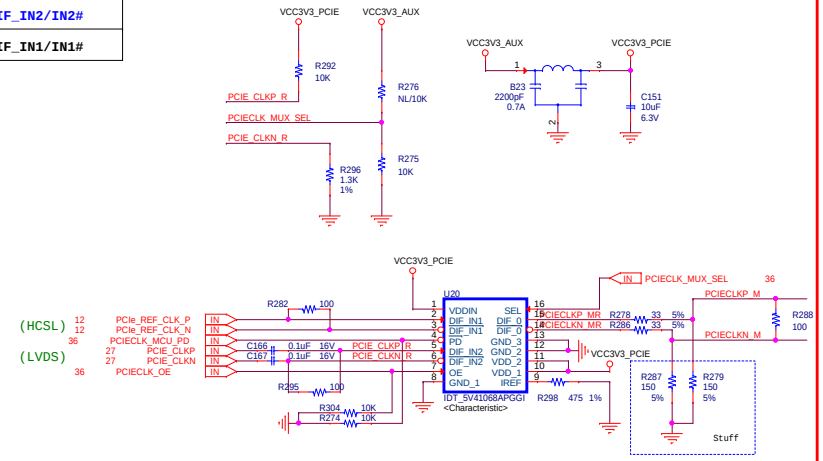
SOC AIF

Note: AIF is nnly supported on K2H devices

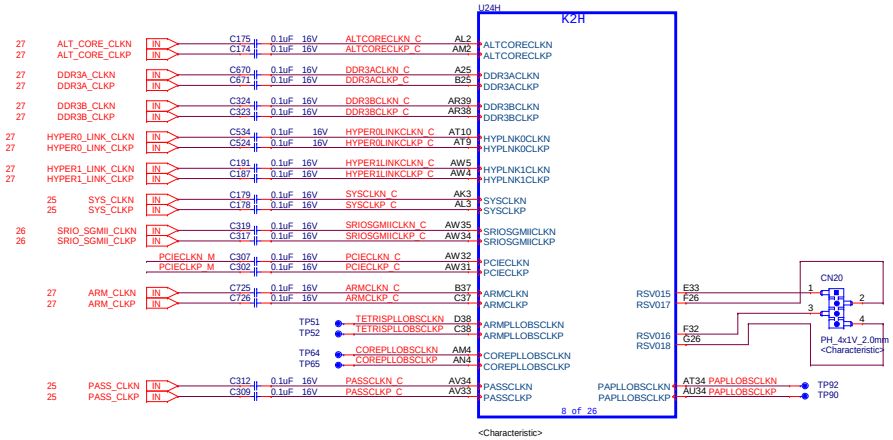


SOC CLOCK / RESET

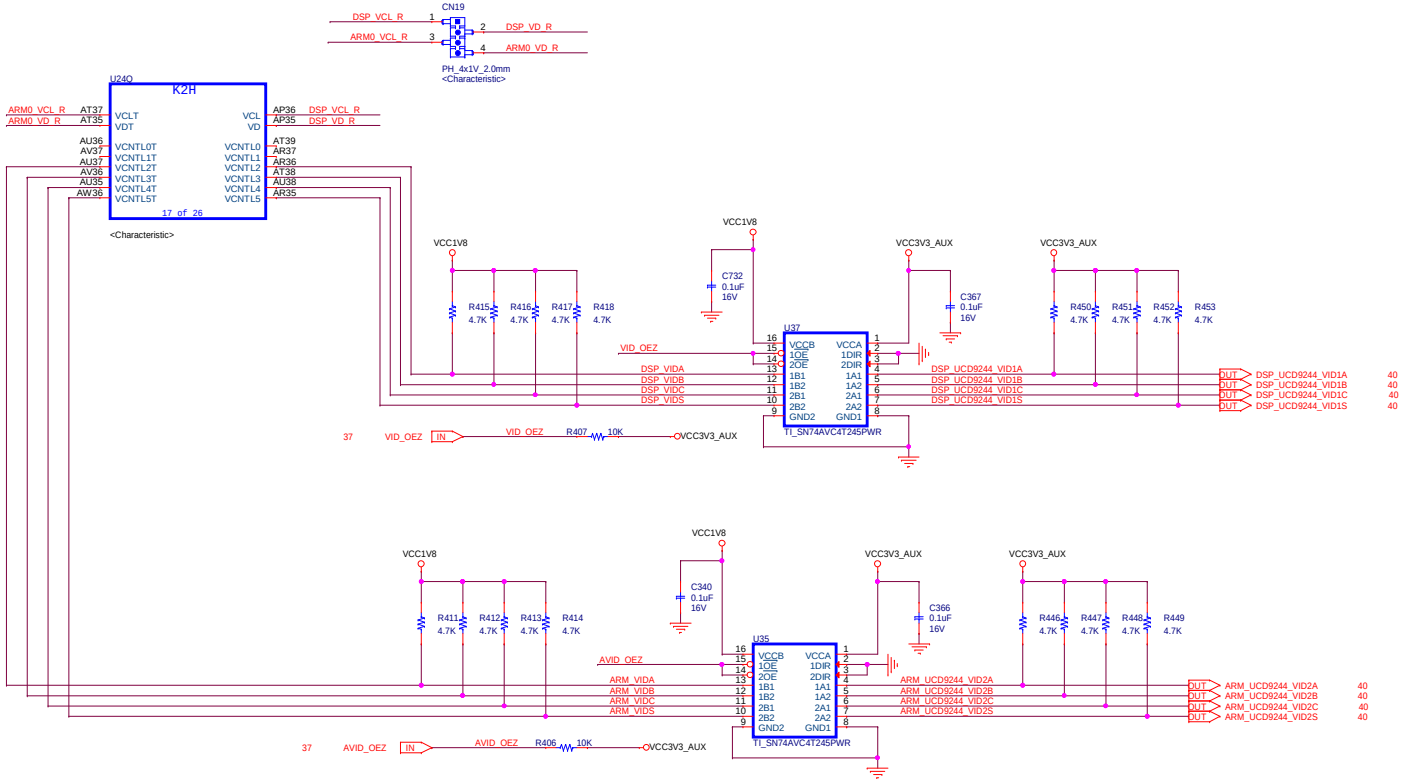
SEL	I/P PAIR SEL
LOW	DIF_IN2/IN2#
HIGH	DIF_IN1/IN1#



All blocking capacitors should be placed near SOC to keep connecting routes short and minimize vias



Smart Reflex



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Title	SOC_CLOCK & Smart-Reflex VID		
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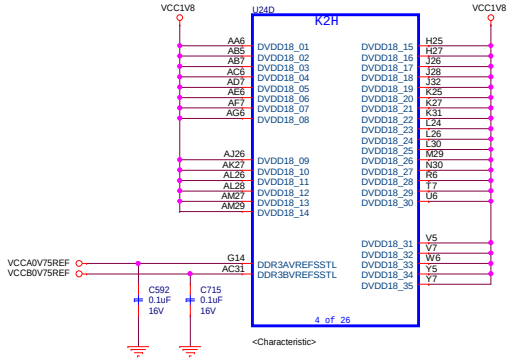
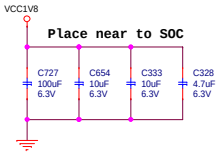
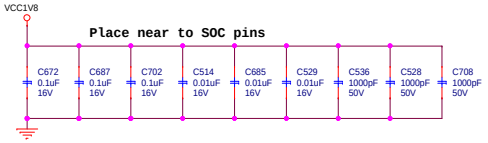
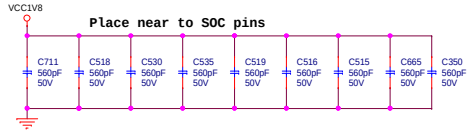
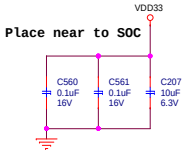
1.8V_1A

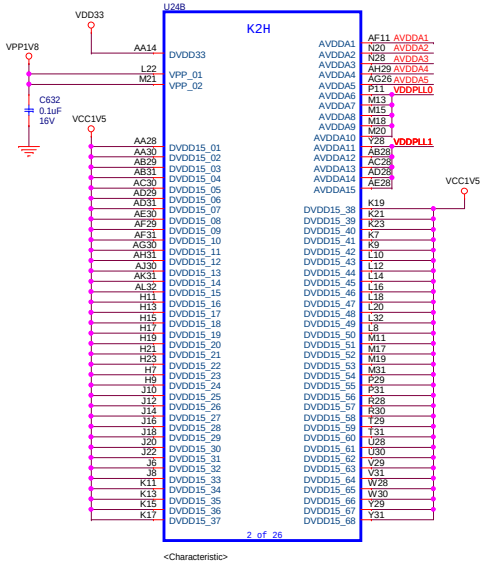


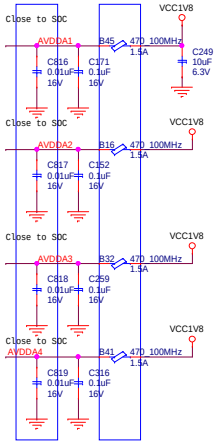


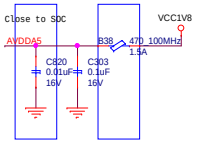


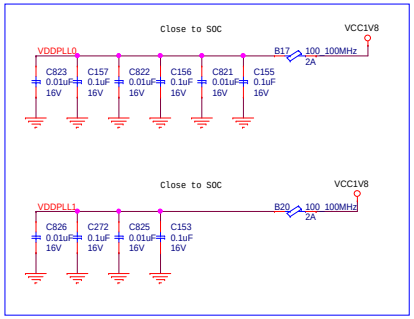


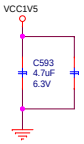


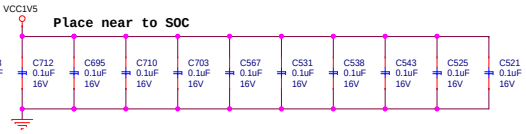


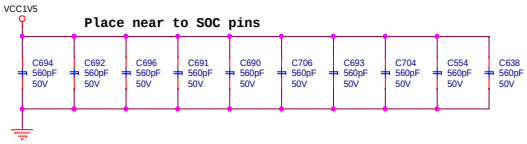


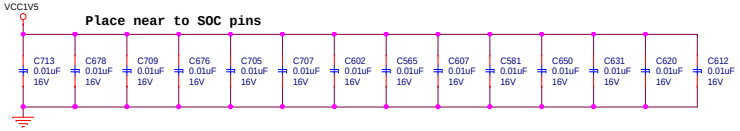












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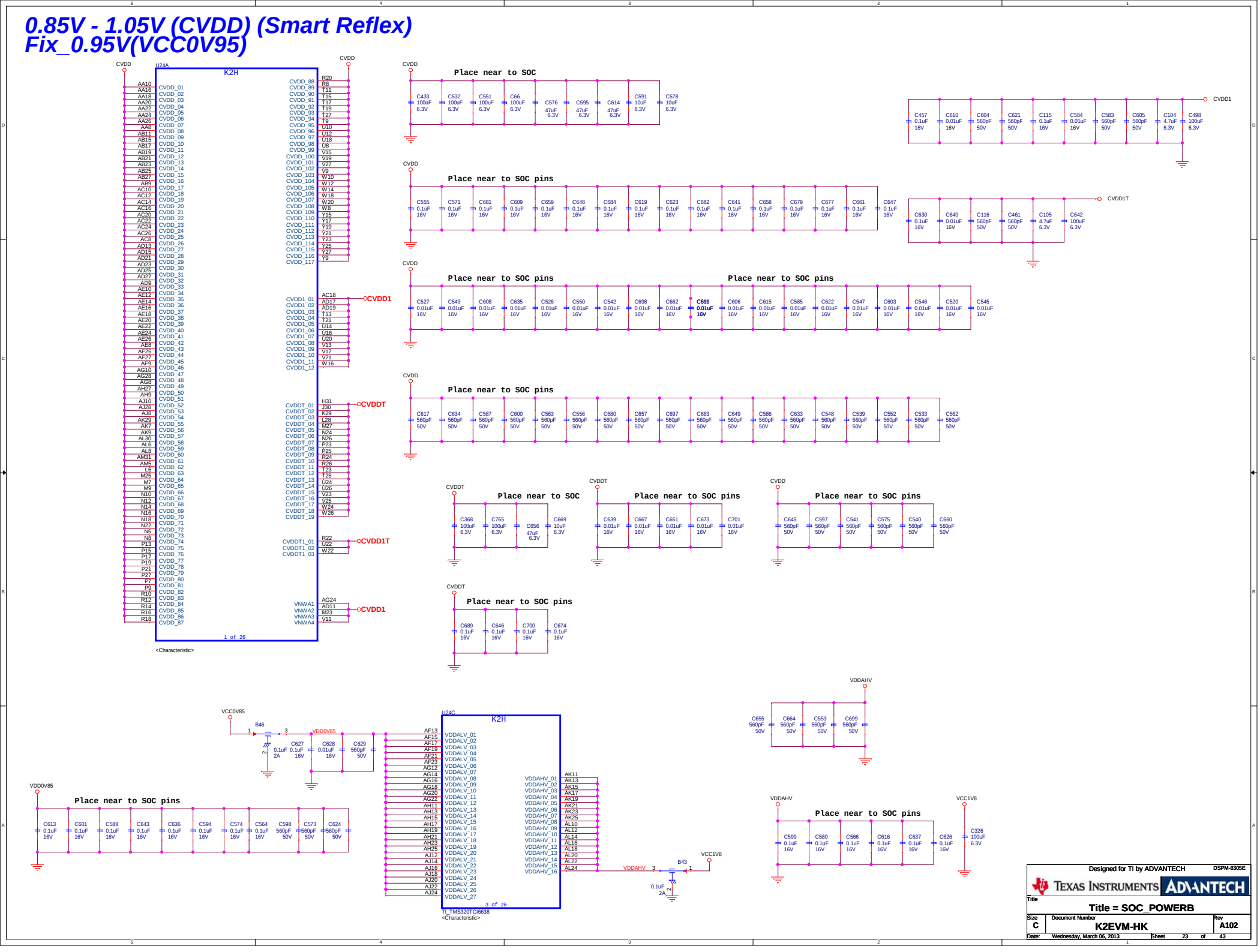
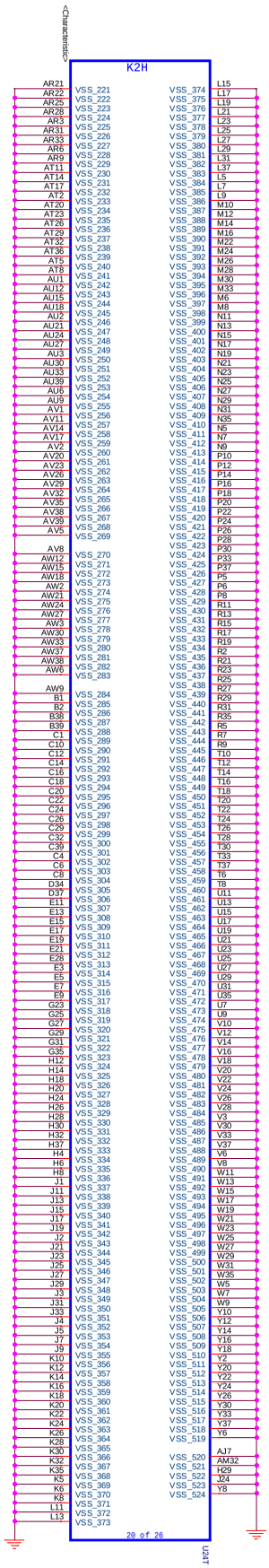
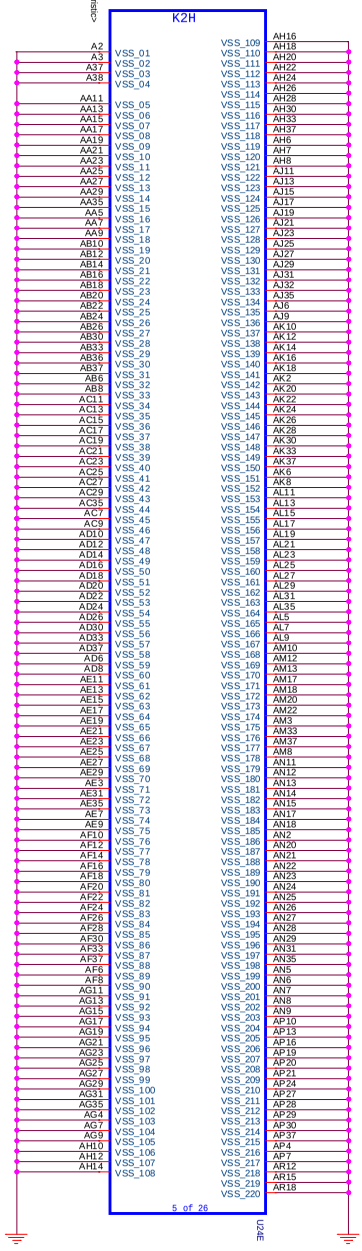
0.85V - 1.05V (CVDD) (Smart Reflex)
Fix_0.95V(VCC0V95)







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DSPM-6806E

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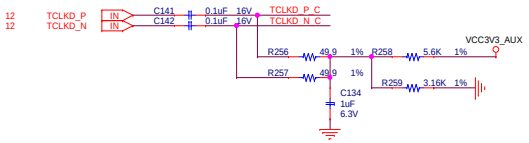
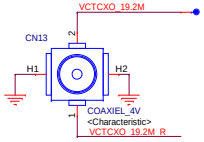
Title: SOC_GND

CLOCK GEN1

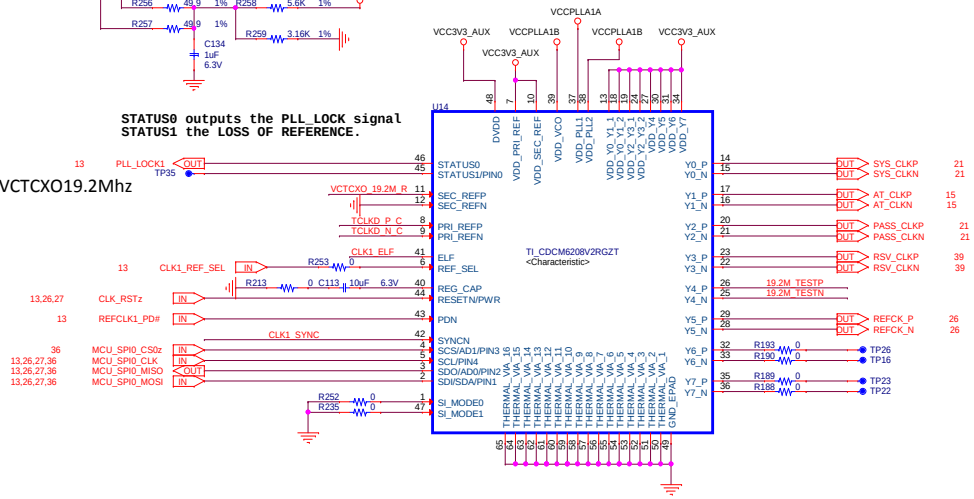
from AMC.0 care
30.72MHz





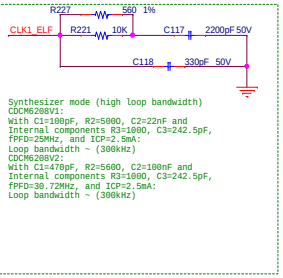
STATUS0 outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

from VCTCXO19.2Mhz



From MCU connect to this signal

R227//R221=530.303



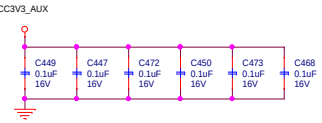
[Note]layout would place R213and C113 close to U14.

Serial Interface Mode or Pin Mode Selection

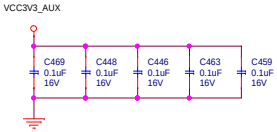
MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

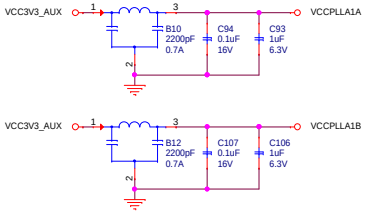
pull-up resister

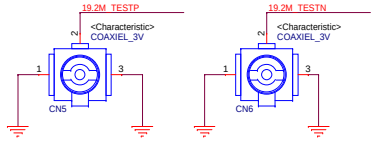
122.88MHz Output
122.88MHz Output
122.88MHz Output



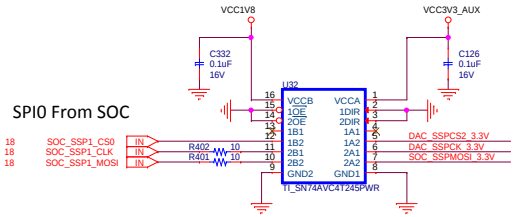
19.2MHz Output

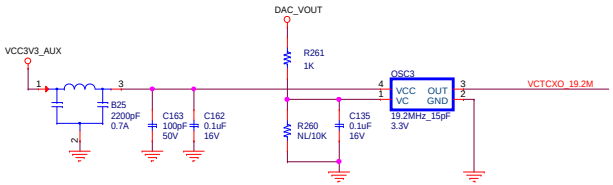


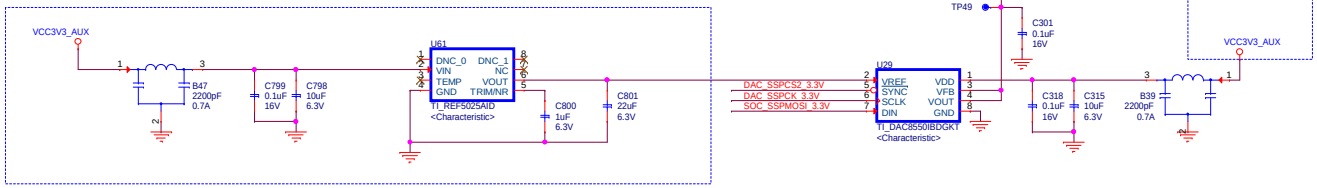




SPI0 From SOC







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Title	CLOCK GEN1	
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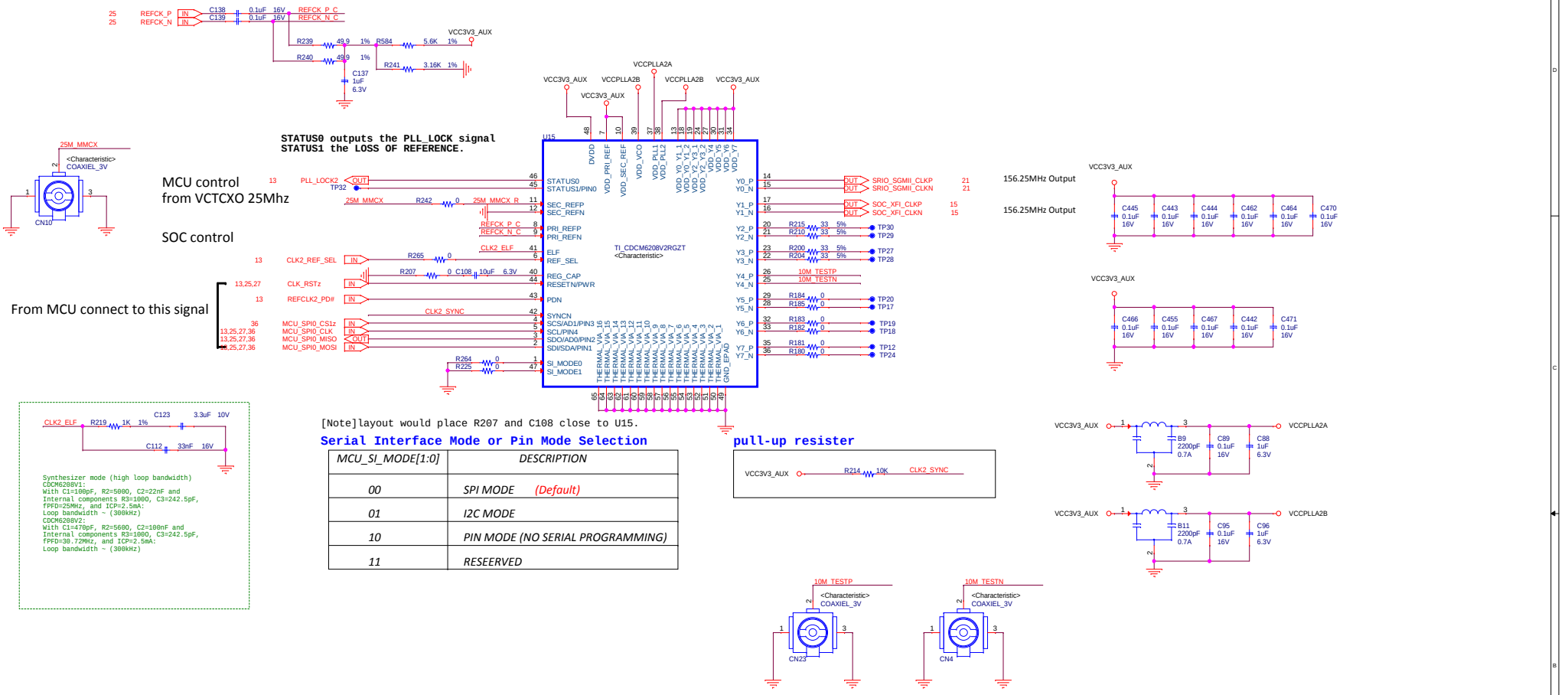
CLOCK GEN2



[Note]layout would place R207 and C108 close to U15.

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

pull-up resister

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TEXAS INSTRUMENTS ADVANTECH

Title	CLOCK GEN2	
Size C	Document Number K2EVM-HK	Rev A102
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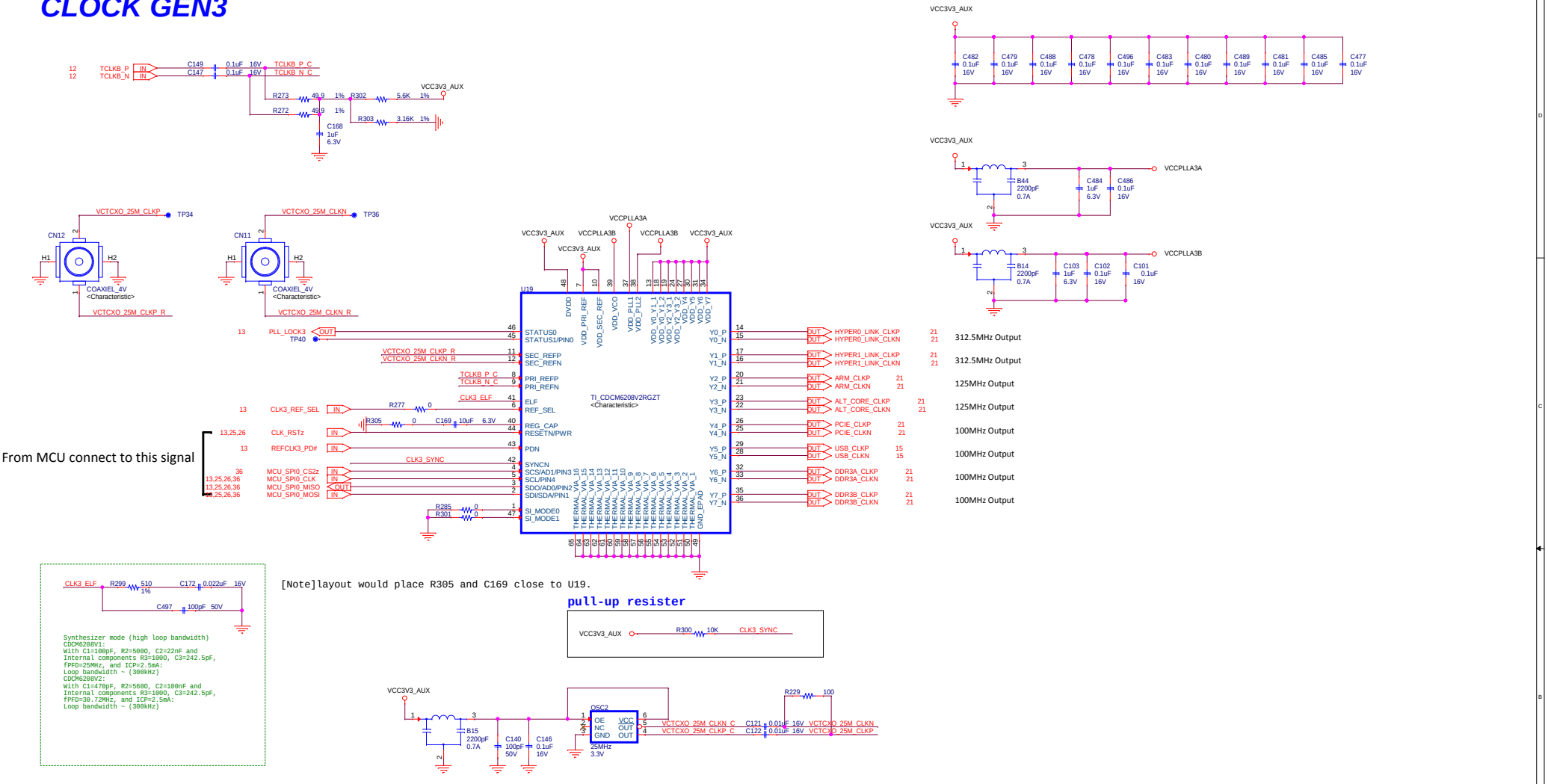
CLOCK GEN3



From MCU connect to this signal

[Note]layout would place R305 and C169 close to U19.

pull-up resister

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Title	CLOCK GEN3	
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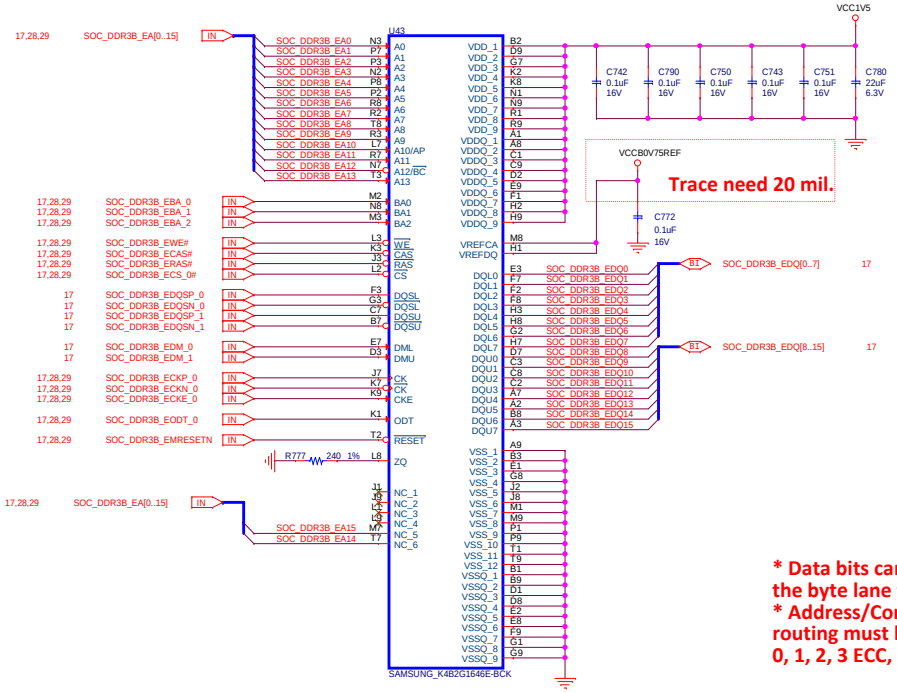
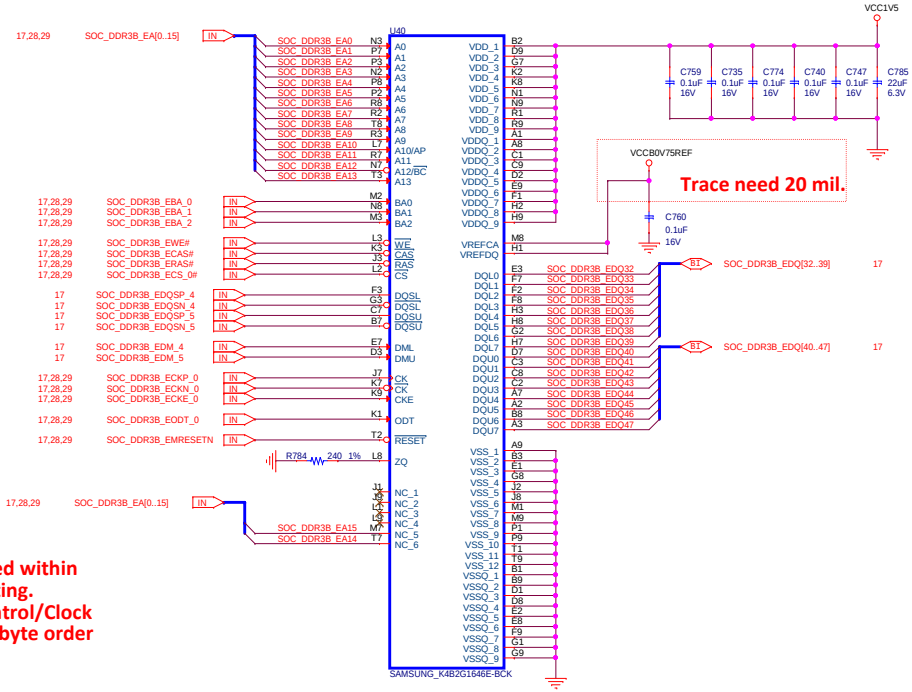
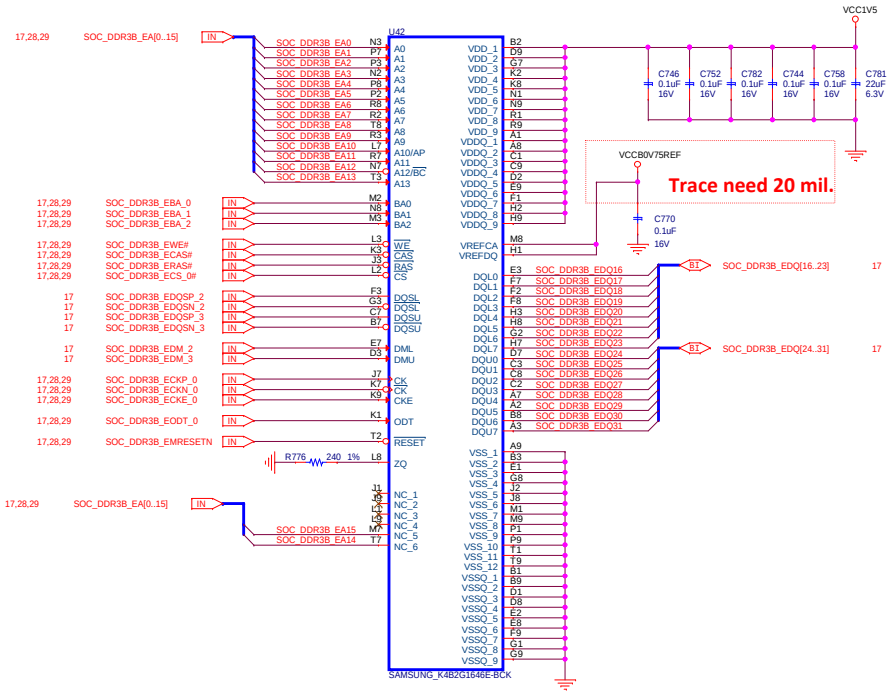
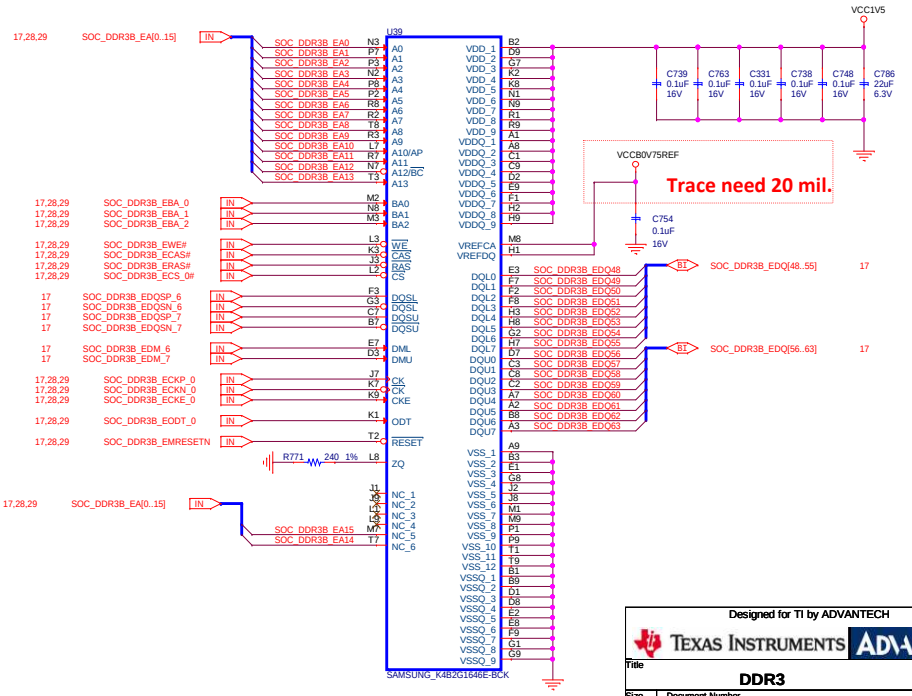




*** Data bits can be swapped within the byte lane to ease routing.**
*** Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.**





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TEXAS INSTRUMENTS ADVANTECH

Title			
DDR3			
Size: C	Document Number: K2EVM-HK		Rev: A102
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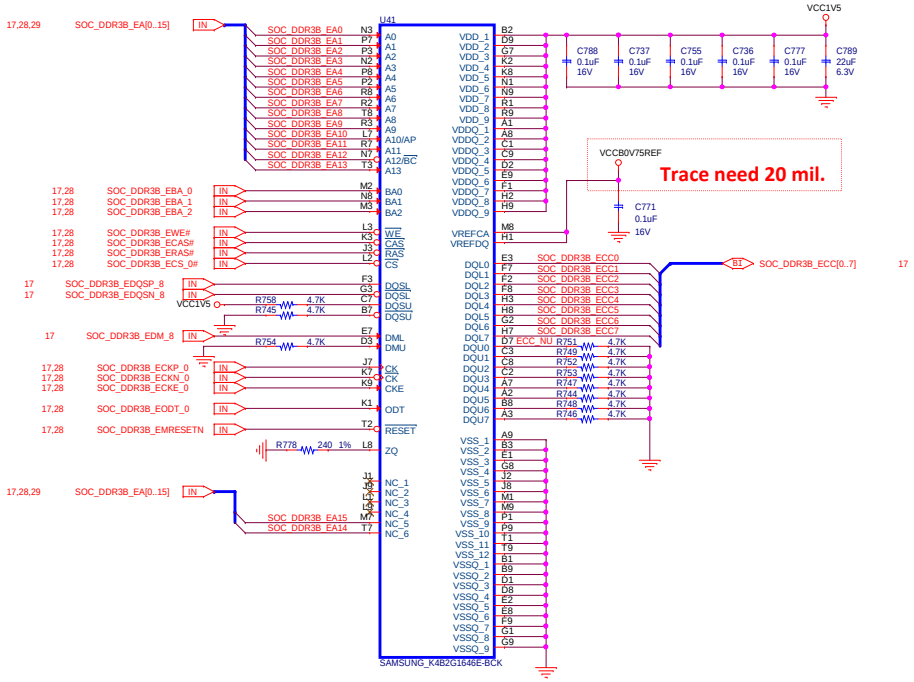
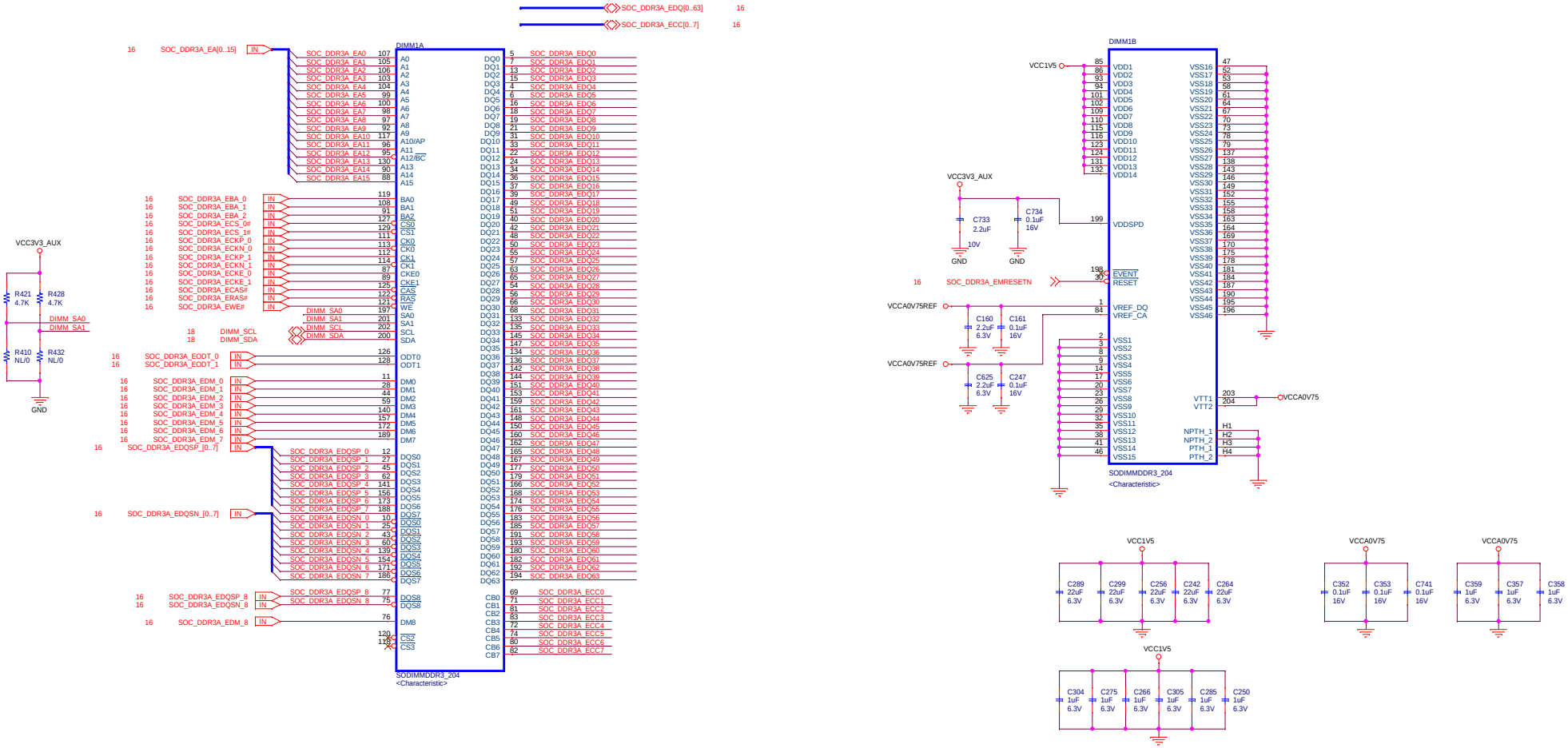
FOR ECC USE



Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title			
DDR3_ECC			
Size: C	Document Number: K2EVM-HK		Rev: A102
Date: Wednesday, March 06, 2013	Sheet 29 of 43		

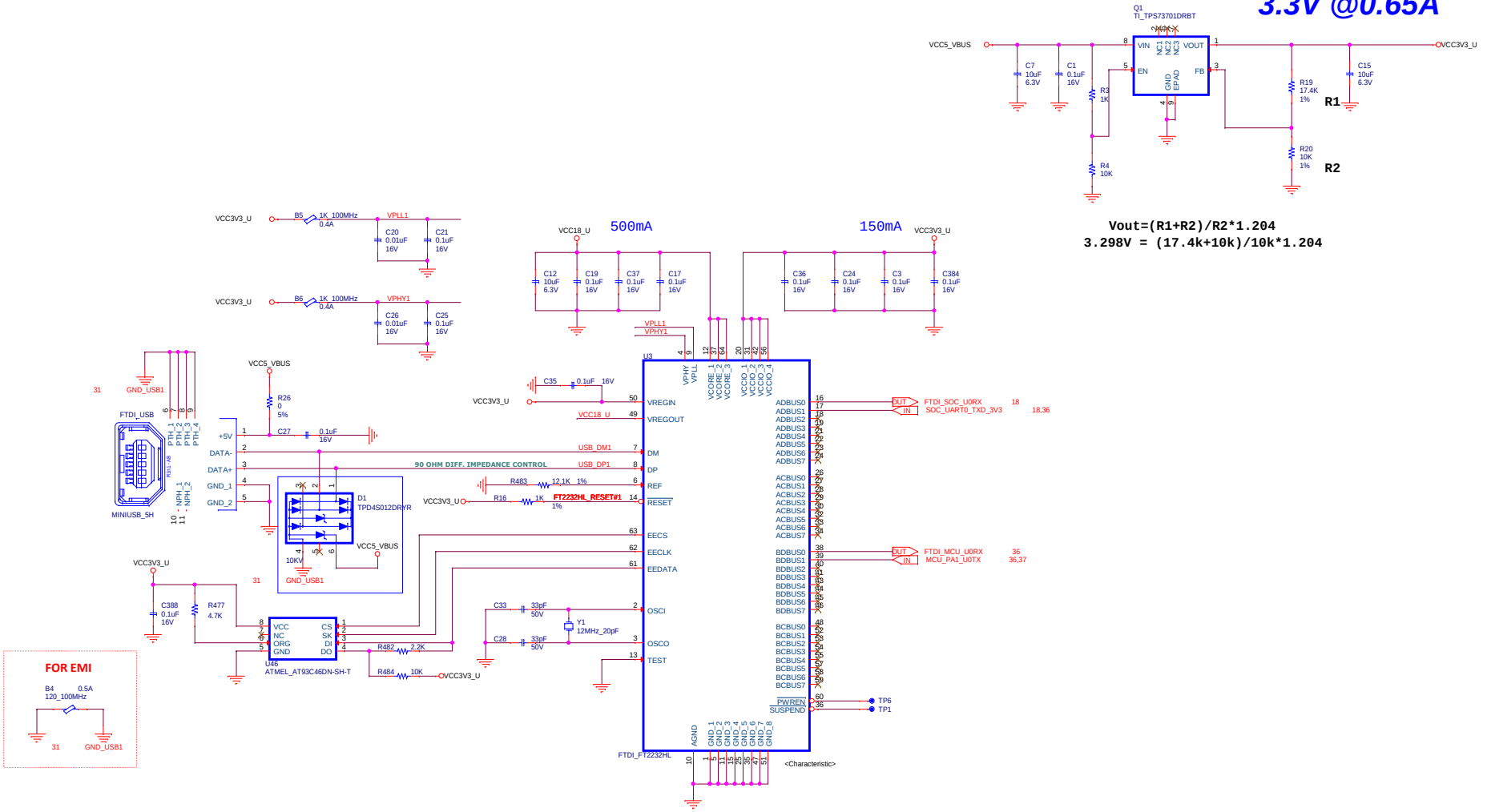


Designed for TI by ADVANTECH

Texas Instruments ADVANTECH

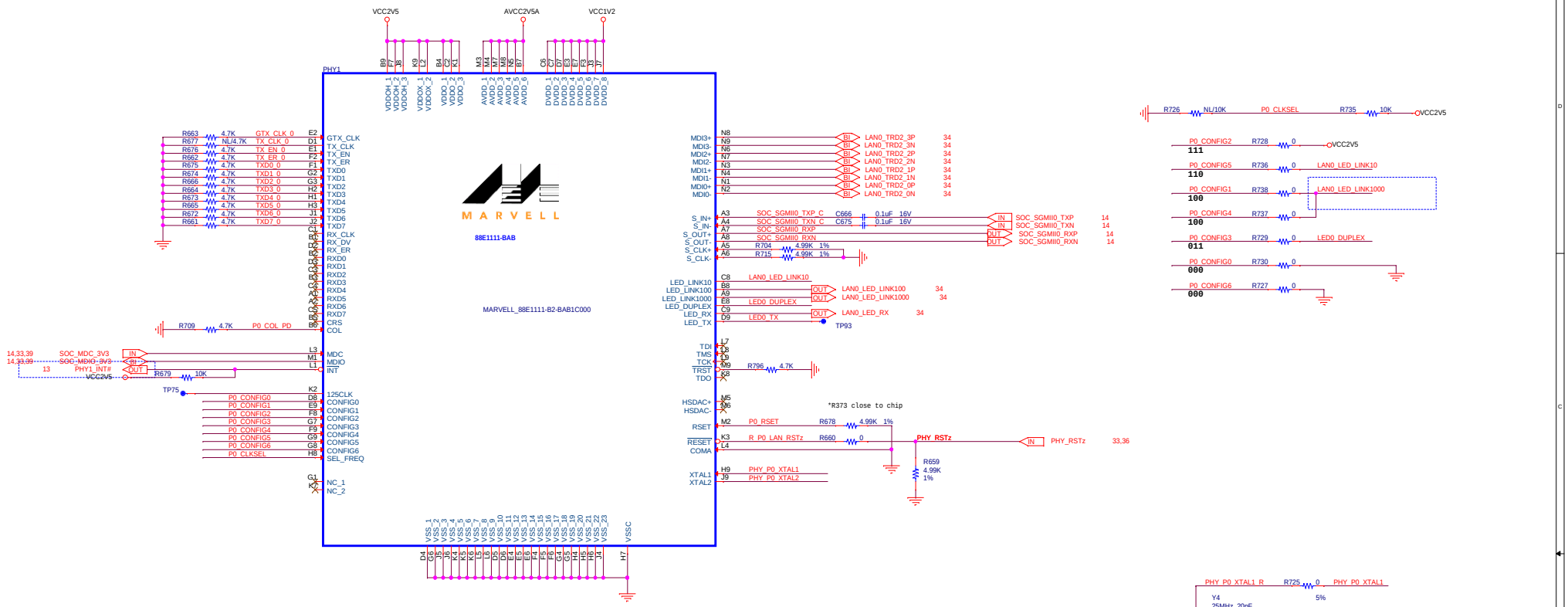
Title	DDR3 SODIMM	
Size C	Document Number K2EVM-HK	Rev A102
Date: Wednesday, March 06, 2013	Sheet 30 of 43	

SoC UART1 TO USB



Designed for TI by ADVANTECH DSPM-8305E

Title	SoC UART1 TO USB	
Size C	Document Number K2EVM-HK	Rev A102
Date: Wednesday, March 06, 2013	Sheet 31 of 43	



88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x00

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	000 [1]	LED_TX	PHY Address bit[2:0] 000
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4			
CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

Designed for TI by ADVANTECH DSPM-8305E

Title: Gigabit Ethernet PHY1

Size: C | Document Number: K2EVM-HK | Rev: A102

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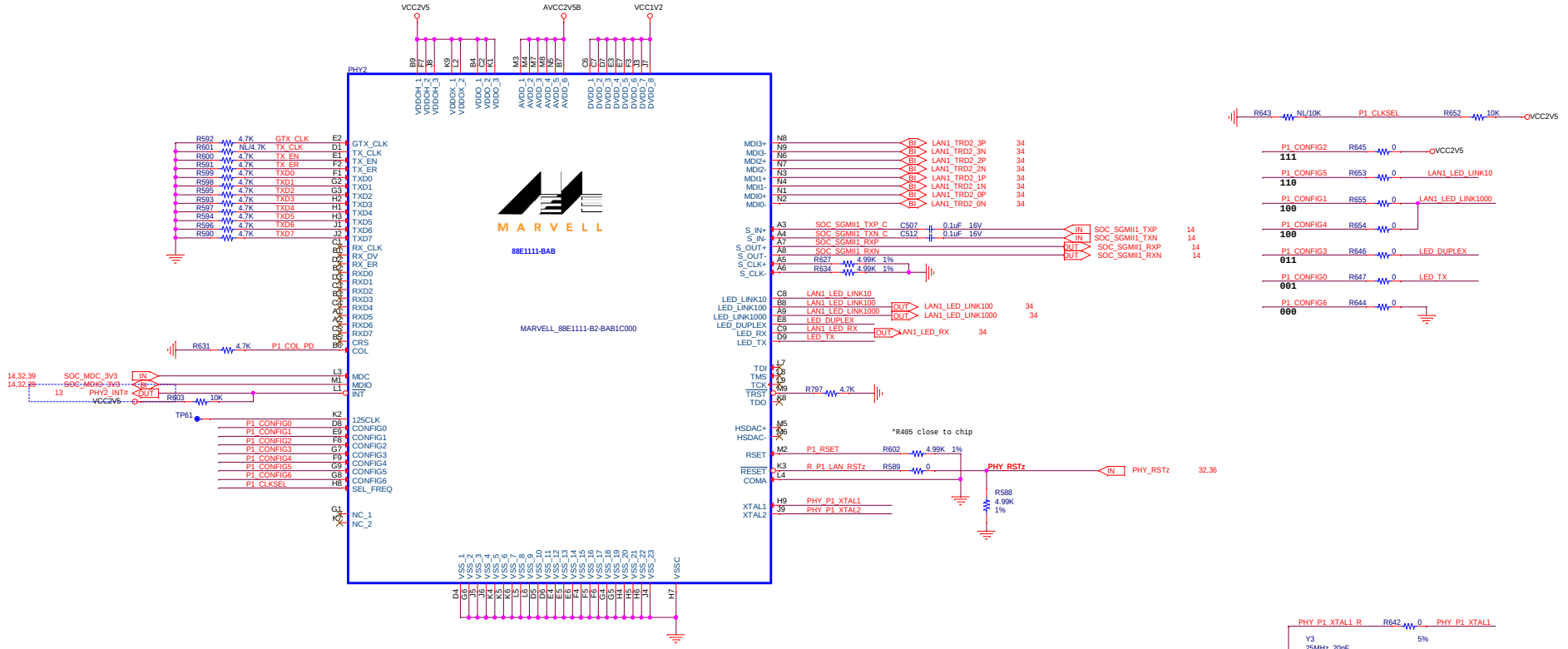

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4			
CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: Gigabit Ethernet PHY2

Size	Document Number	Rev
C	K2EVM-HK	A102

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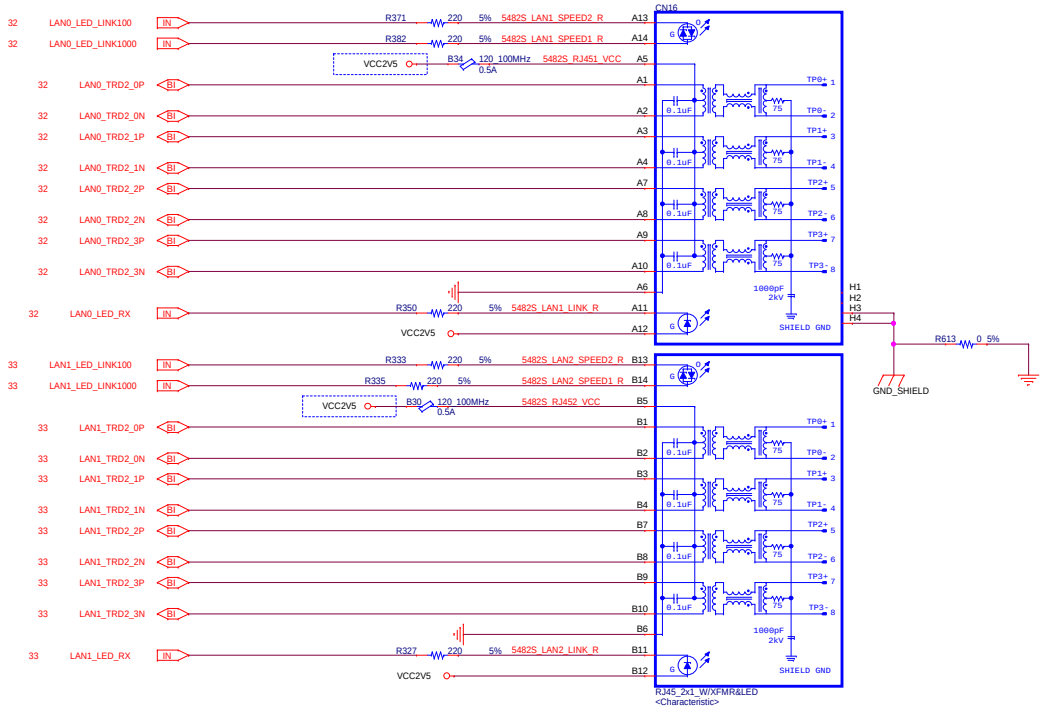
Bi-Color LED's on RJ45 controls from PHY

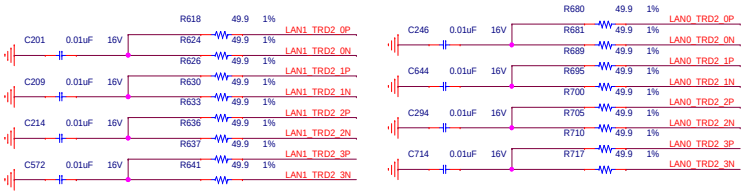
LAN-BI[88E1111 Output Port0]

	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

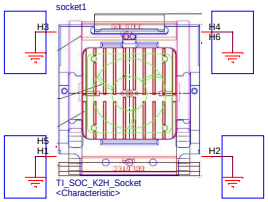
LAN-BI[88E1111 Output Port1]

	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

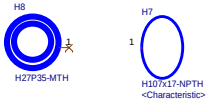




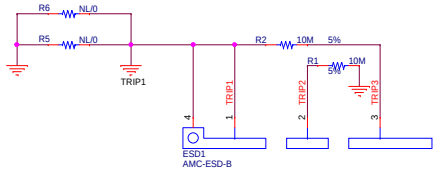
SoC Socket



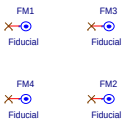
AMC Hole



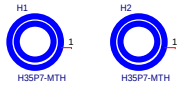
Front panel and ESD Strip



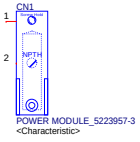
On board



XDS200 Holes



Key Zone



(Bottom Side 3mm) Placed Capacitors

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TEXAS INSTRUMENTS ADVANTECH

Title	88E1111 RJ45	
Size C	Document Number K2EVM-HK	Rev A102
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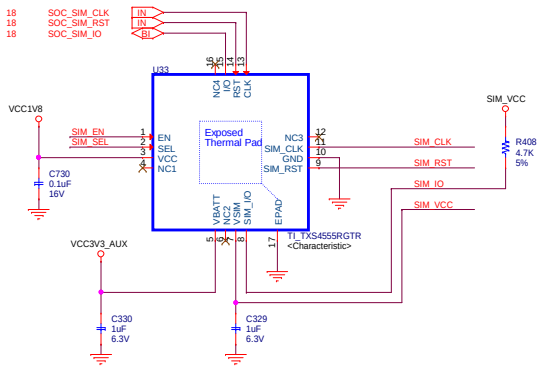
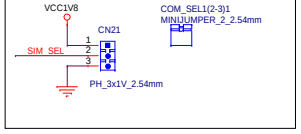
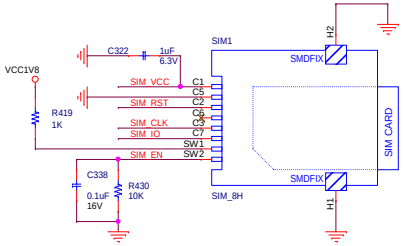
USIM

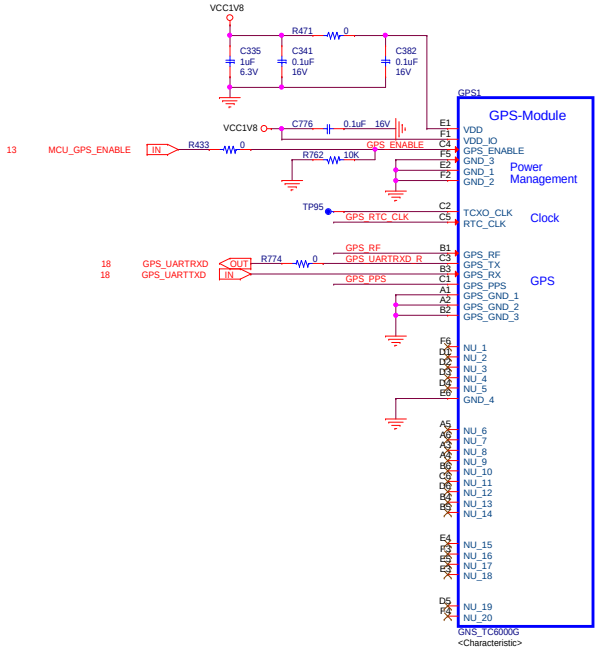


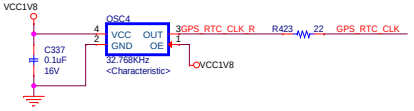
	High	Low (Default)
SIM_SEL	VCC_SIM Value = 2.95V	VCC_SIM Value = 1.8V

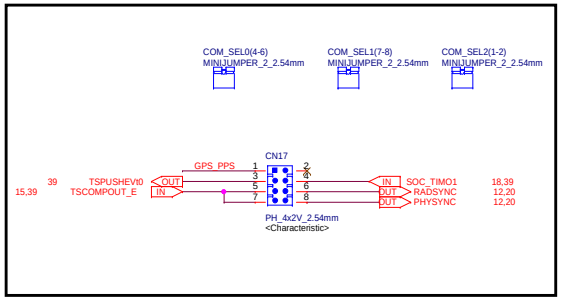




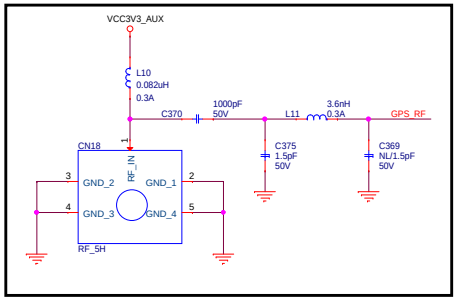
GPS







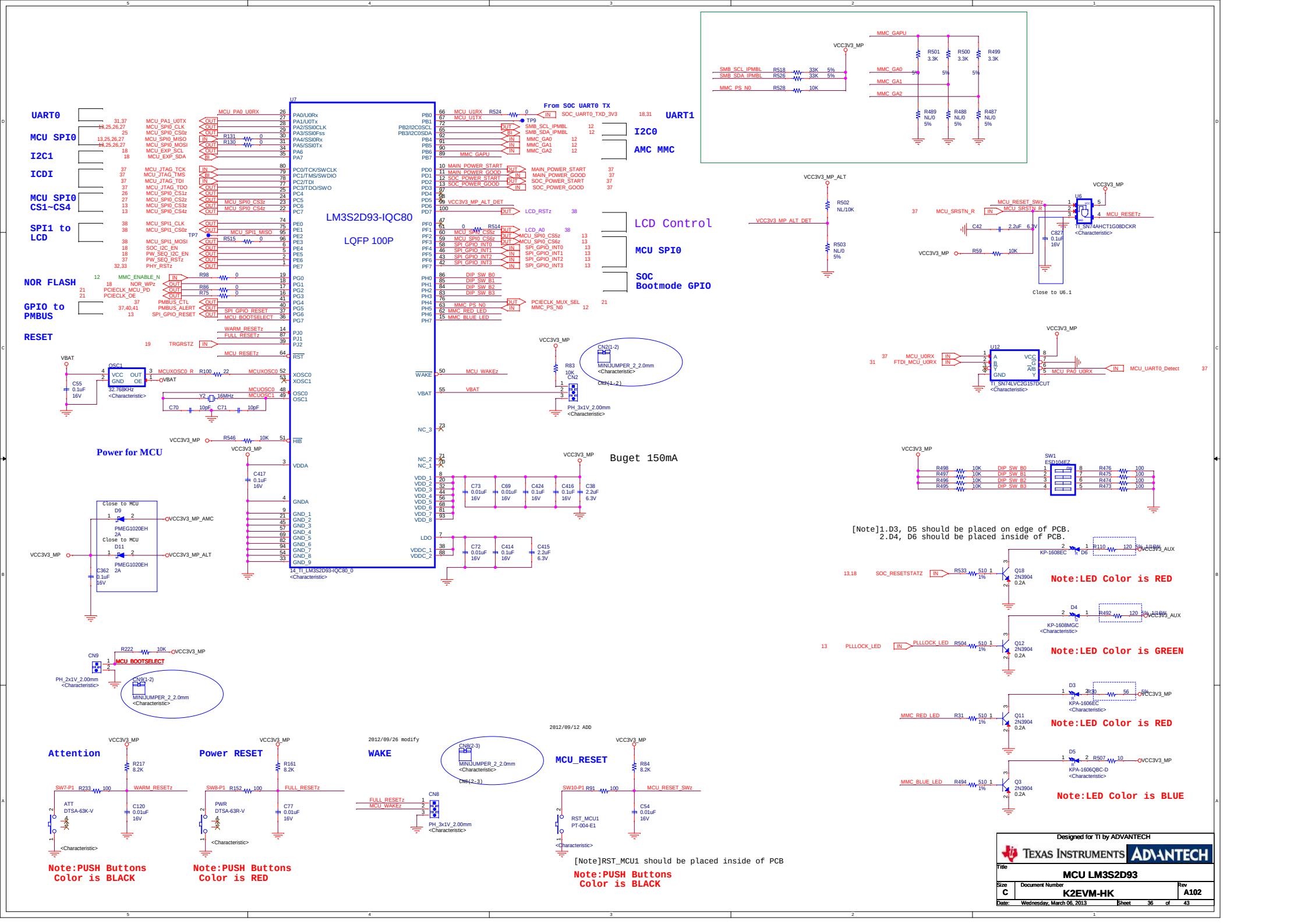
FOR ANTENNA CIRCUIT



Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title	GPS & SIM CARD	
Size C	Document Number K2EVM-HK	Rev A102
Date: Wednesday, March 06, 2013	Sheet 35 of 43	


UART0
MCU SPI0
I2C1
ICDI
MCU SPI0 CS1~CS4
SPI1 to LCD
NOR FLASH
GPIO to PMBUS
RESET
LM3S2D93-IQC80
LQFP 100P
From SOC UART0 TX
UART1
I2C0
AMC MMC
LCD Control
MCU SPI0
SOC Bootmode GPIO
Power for MCU
Buget 150mA
Close to MCU
Close to U6.1
[Note]1.D3, D5 should be placed on edge of PCB.
2.D4, D6 should be placed inside of PCB.
Note:LED Color is RED
Note:LED Color is GREEN
Note:LED Color is BLUE
Attention
Power RESET
WAKE
MCU_RESET
2012/09/26 modify
2012/09/12 ADD
Note:PUSH Buttons Color is BLACK
Note:PUSH Buttons Color is RED
[Note]RST_MCU1 should be placed inside of PCB
Note:PUSH Buttons Color is BLACK
Designed for TI by ADVANTECH
Title
MCU LM3S2D93
Size C
Document Number K2EVM-HK
Rev A102
Date: Wednesday, March 06, 2013
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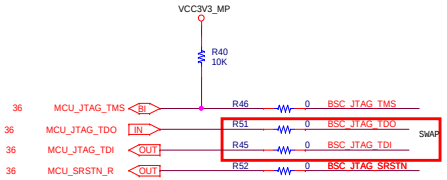
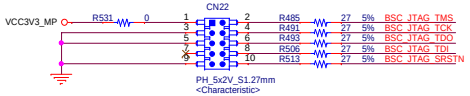
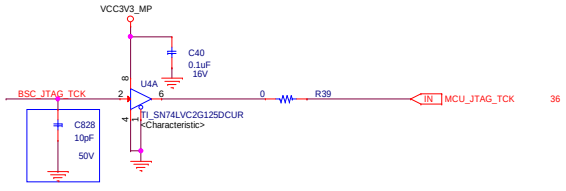
MCU JTAG

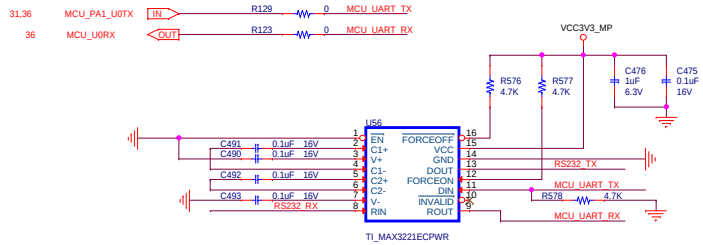


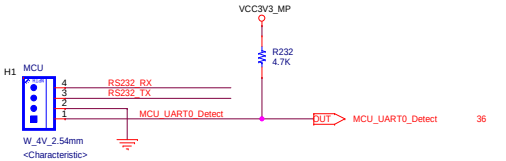


10 pos (50 mil pitch) connector

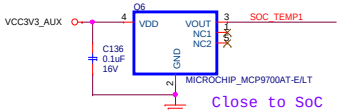


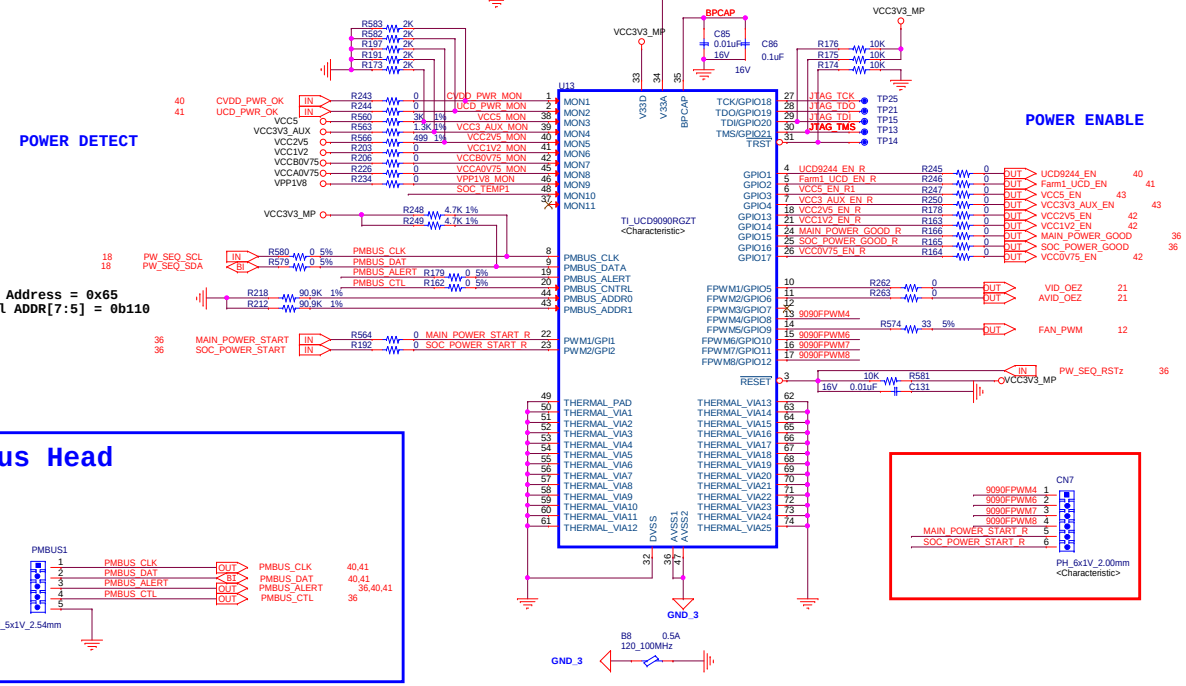
MCU UART





Power Sequencing





Slave I2C Address = 0x65
(Internal ADDR[7:5] = 0b110

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

PMBus Head

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TEXAS INSTRUMENTS ADVANTECH

Title	MCU MISC	
Size C	Document Number K2EVM-HK	Rev A102
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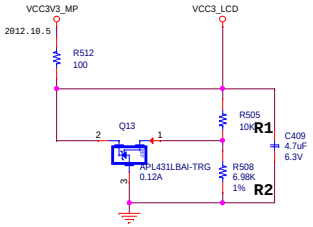
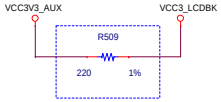
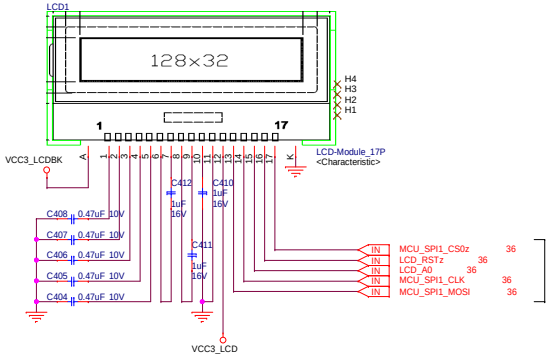


VO = 1.24v(1+R1/R2)+0.15uA*R1

3.018V =1.24 (1+10k/6.98k)+0.15u*10k



NHD-C12832A1Z-FSB-FBW-3V3



SPI1 CS0
LCD control

Designed for TI by ADVANTECH DSPM-8305E

Title: **MCU LCD**

Size	Document Number	Rev
C	K2EVM-HK	A102

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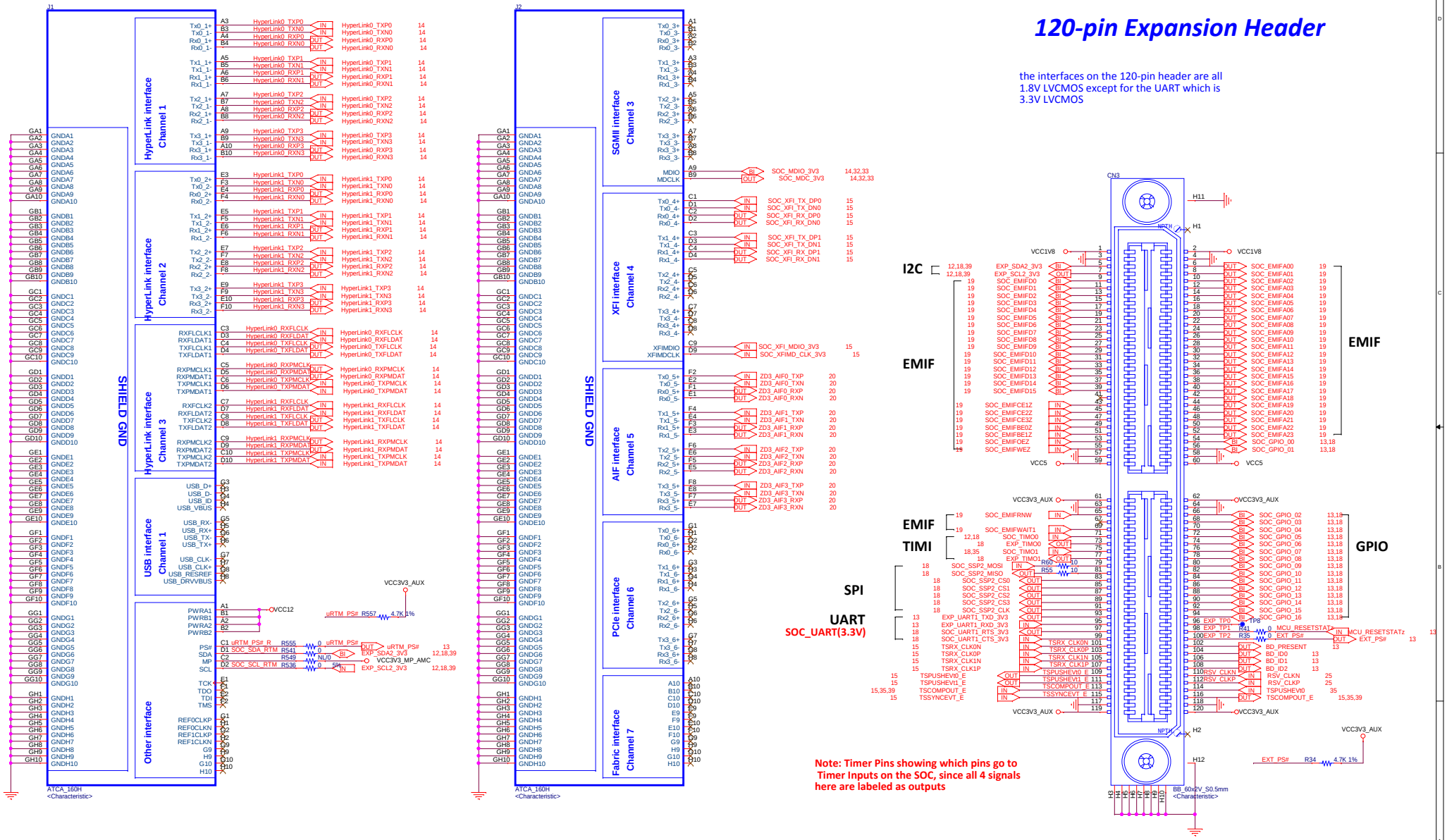
Note : J1 connector close to AMC Interface.

Note : J2 connector close to Key socket.



120-pin Expansion Header

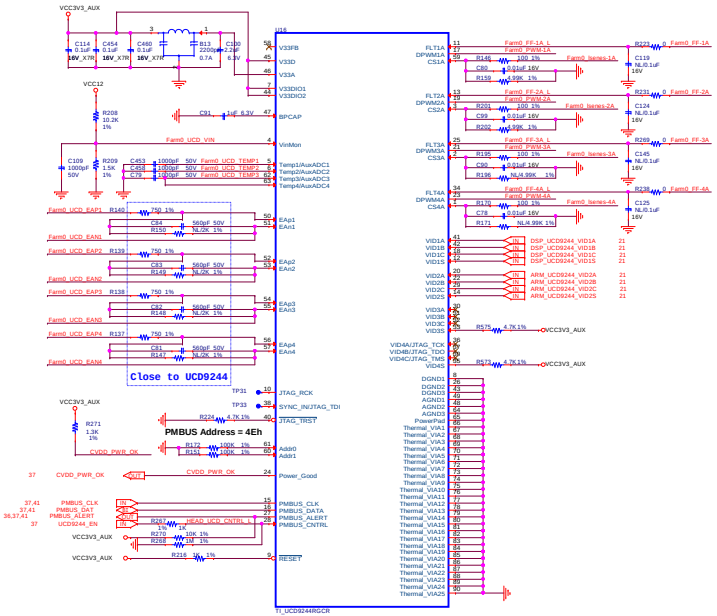
the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS

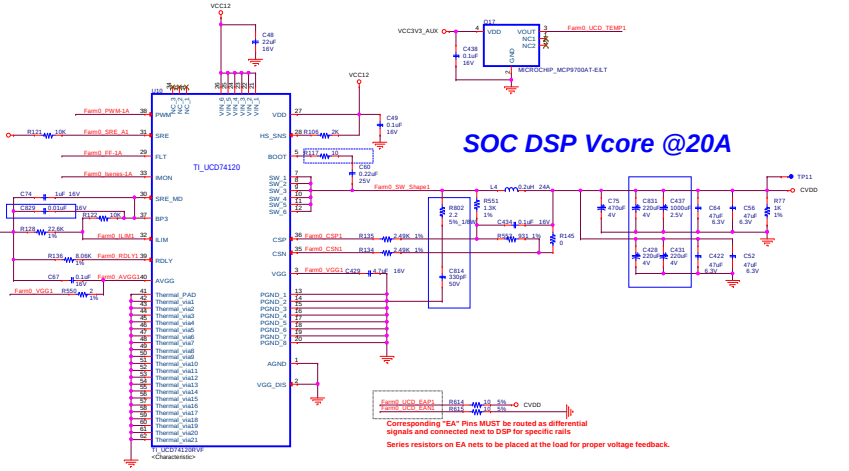
Note: Timer Pins showing which pins go to Timer Inputs on the SOC, since all 4 signals here are labeled as outputs

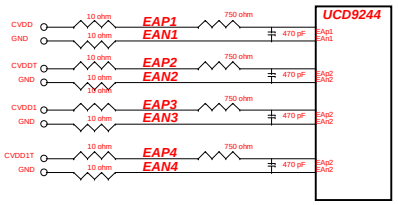
Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

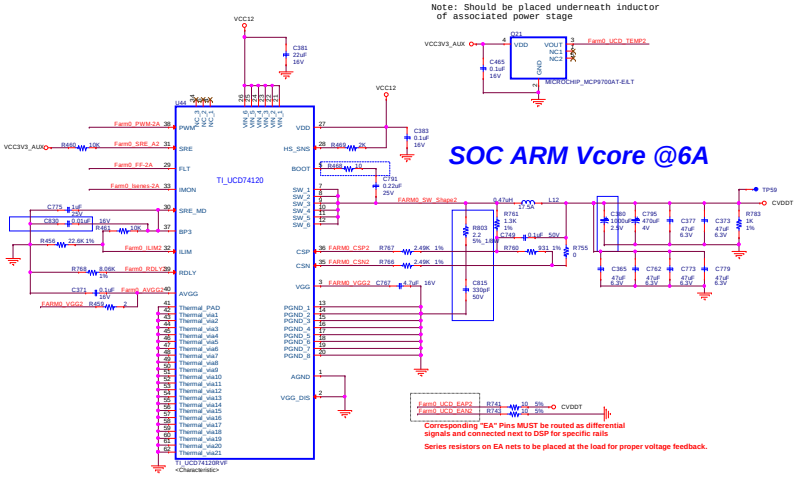
Title	mTCA_ZD3/120-pin Expansion	
Size C	Document Number K2EVM-HK	Rev A102
Date: Wednesday, March 06, 2013	Sheet 39 of 43	





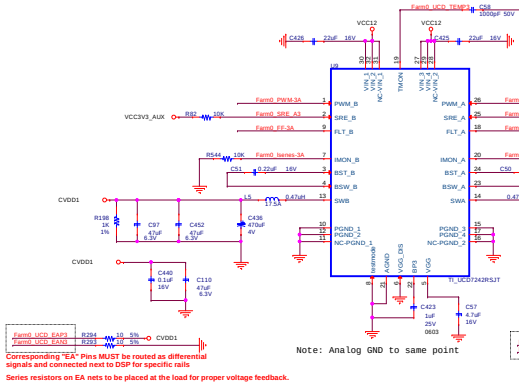


Note: Should be placed underneath inductor of associated power stage



0.95V @5A

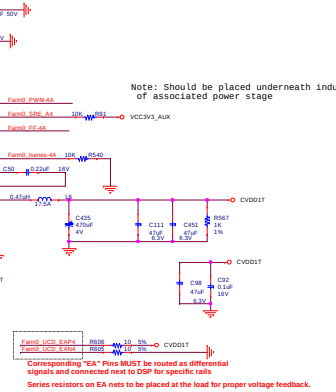
DSP Fixed Core Supply



0.95V @5A

ARM Fixed Core Supply

Note: Should be placed underneath inductor of associated power stage



PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

Designed for TI by ADVANTECH

DSPM-6305E

TEXAS INSTRUMENTS ADVANTECH

Title: Smart_Reflex AVS

Size	Document Number	Rev
D	K2EVM-HK	A102

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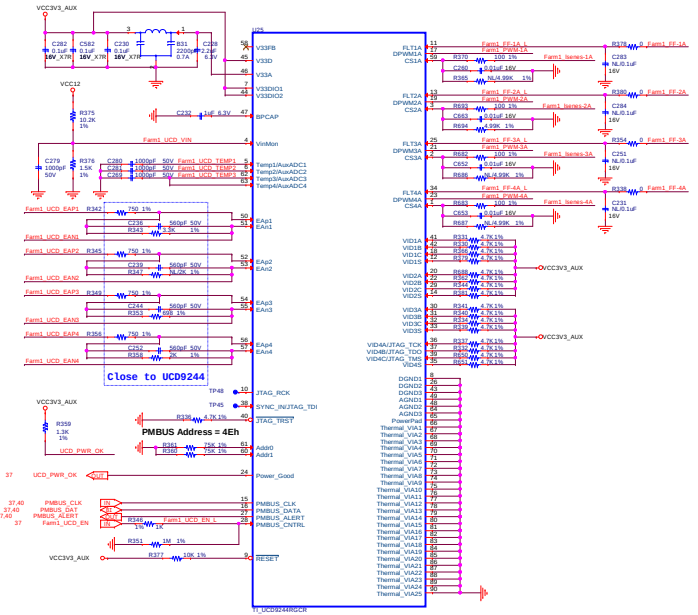
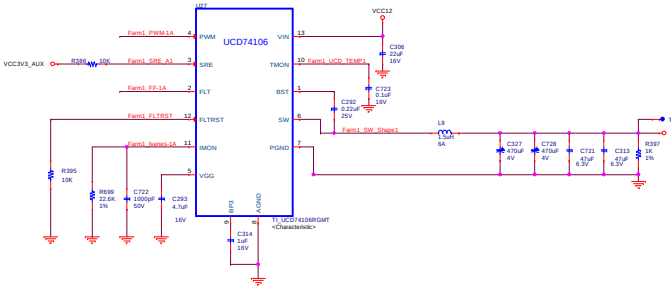
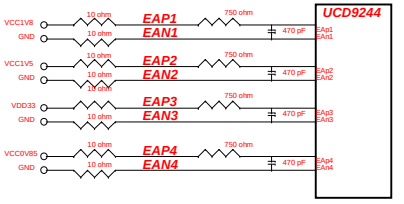


PLL, 1.8V I/O and SERDES @5A



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.



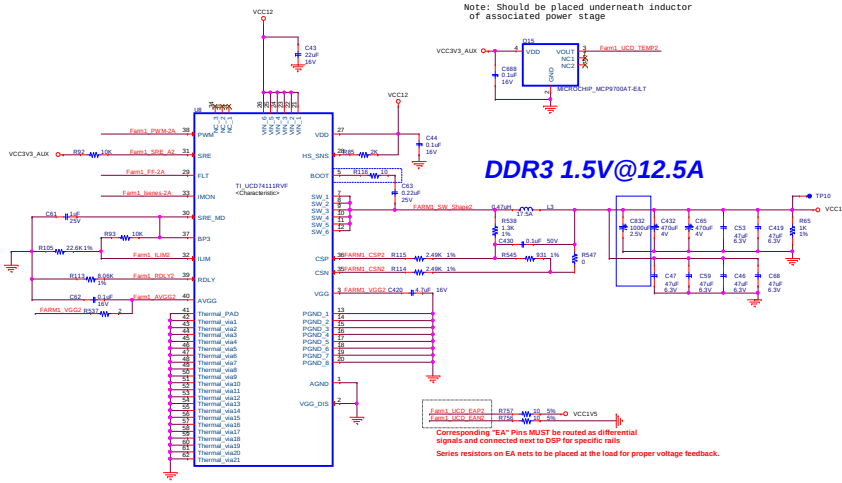
Series resistors on EA nets to be placed at the load for proper voltage feedback.

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

Note: Should be placed underneath inductor of associated power stage

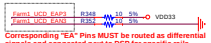
DDR3 1.5V@12.5A



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

SOC VDD33 @TBD



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

SOC USB and SERDES 0.85V @TBD

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Designed for TI by ADVANTECH DSPM-6305E

TEXAS INSTRUMENTS ADVANTECH

Title: Smart_Reflex VDD33/1.8V/1.5V/0.85V

Size	Document Number	Rev
D	K2EVM-HK	A102

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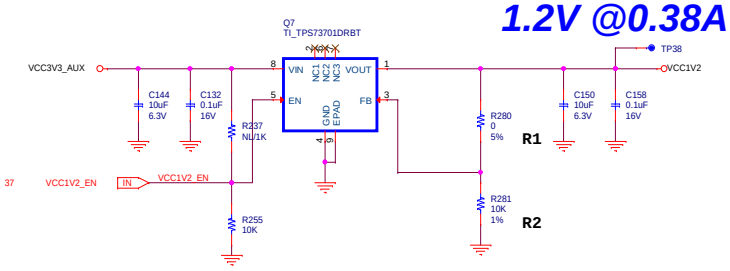
VCC1V2

1.2V @0.38A

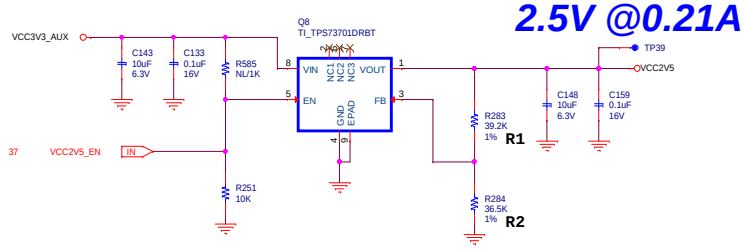


Vout=(R1+R2)/R2*1.204

1.204V = (0+10k)/10k*1.204

VCC2V5

2.5V @0.21A

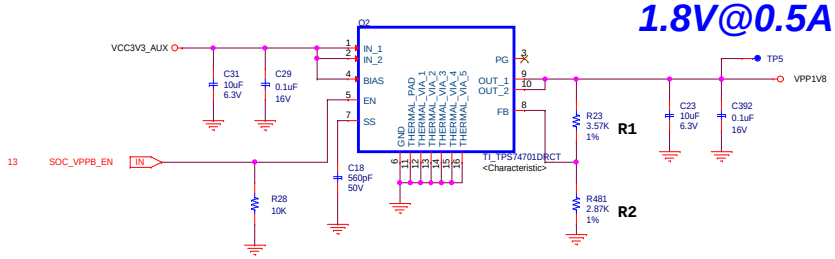


Vout=(R1+R2)/R2*1.204

2.50V =(39.2k+36.5k)/36.5k*1.204

VPP1V8

1.8V@0.5A

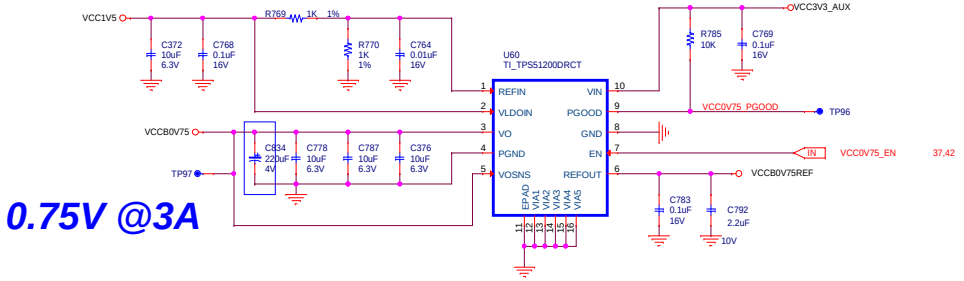


Vout=0.8*(1+R1/R2)

1.79512V =0.8*(1+3.57k/2.87k)

VCCB0V75

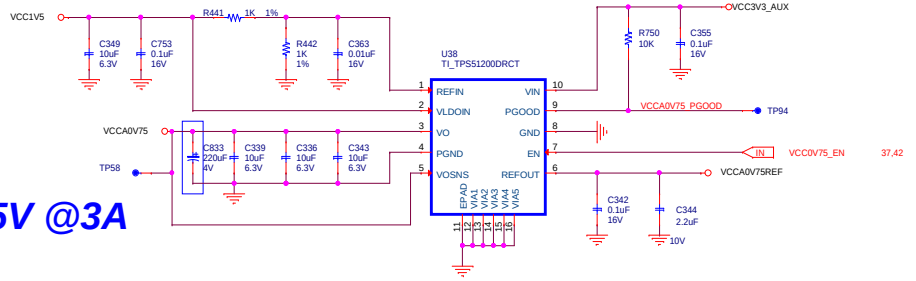
DDR3-1600
DiscreteSDRAM ArrayI



0.75V @3A

VCCA0V75

For DDR3-1600 SO-DIMM



0.75V @3A

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title	Power_1.2V/2.5V/0.75V/1.8V	
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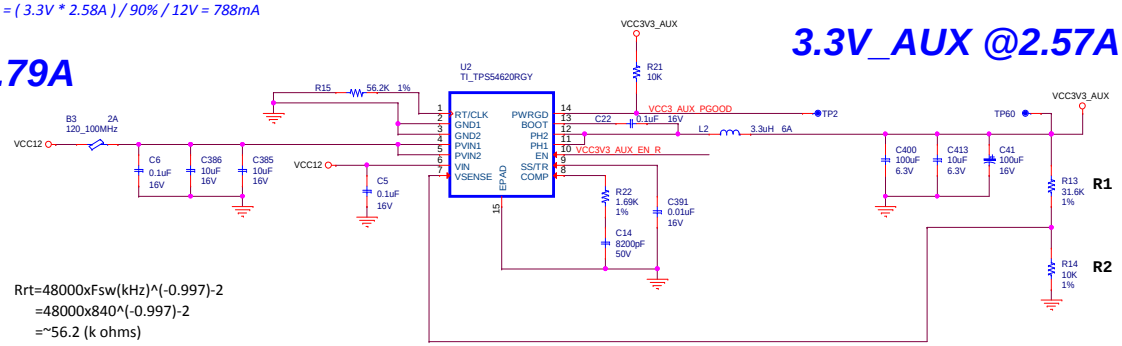
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.57A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x840^(-0.997)-2
=~56.2 (k ohms)

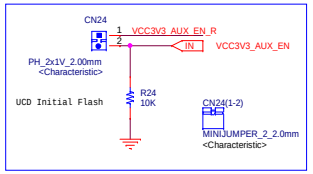
Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*3/(840kHz*0.0825)
Cout=~87uF

Reference Capacitor=100uF

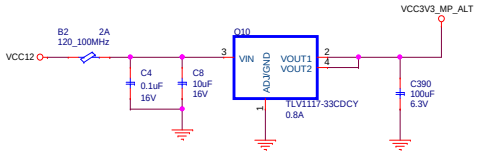
(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3A * 0.3) * (3.3 / (12 * 840kHz))
L = 9.67 * 0.33u
L = ~3.2 uH

Reference Inductor 3.3uH



VCC3V3_MP_ALT

3.3V_MP@150mA



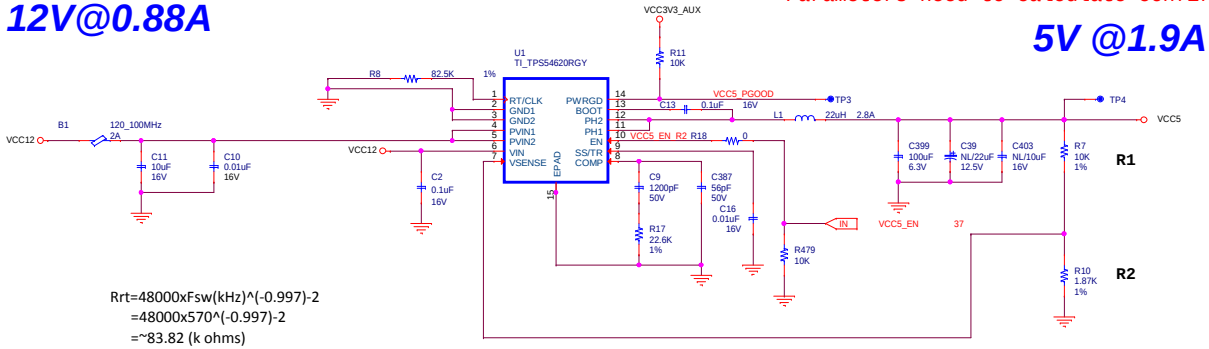
VCC5

Assume 90% Pe,
*Iin = (5V * 1.9A) / 90% / 12V = 880mA*

12V@0.88A

*Parameters need to calculate confirm

5V @1.9A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x570^(-0.997)-2
=~83.82 (k ohms)

Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2/(570kHz*0.125)
Cout=~56.14uF

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 5)/(2.3A * 0.3) * (5 / (12 * 570kHz))
L = 10 * 0.73u
L = ~7.3 uH

Reference Inductor 22uH

Designed for TI by ADVANTECH DSPM-8305E

Title: Power_VCC5 / VCC3V3_AUX/MP_ALT

Size	Document Number	Rev
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