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EVMK2HX Known Issues

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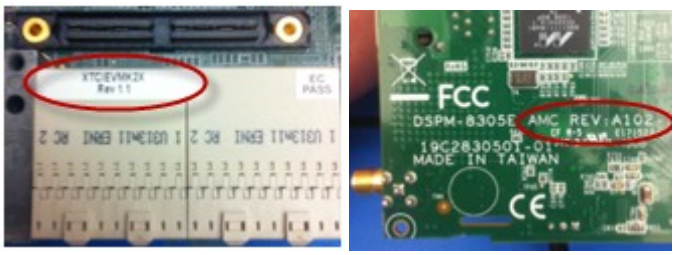
1. Software and Firmware Version List

EVM Revision 1.1 could be identified by sticker on RTM Connector, and the PCB Revision is A102-1 and is located on bottom of board near GPS Antenna Input



The initial firmware versions on Rev 1.1 EVMs are shown as below:

EVM Revision	SN Range	Ship Date	SoC Rev	PCB Rev	BMC Rev	LINUX-MCSDK (NAND)	BIOS-MCSDK (NOR)
Rev1.0	ESE0075202 - 075236	Feb-27	PG 1.0	A102	1.0.1.3a	N/A	Alpha7
Rev1.1	EPD0082118-0082227	May-22 May-24	PG 1.0	A102	1.0.2.5	N/A	Alpha7
Rev2.0		3Q 2013	PG 1.1	A103	1.0.2.5	N/A	Alpha7

Updated firmware/software could be available on Advantech website or TI MCSDK website.

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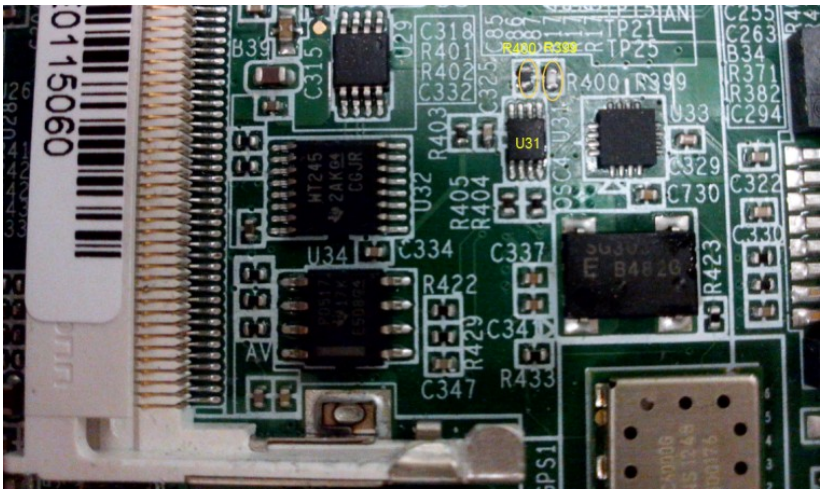
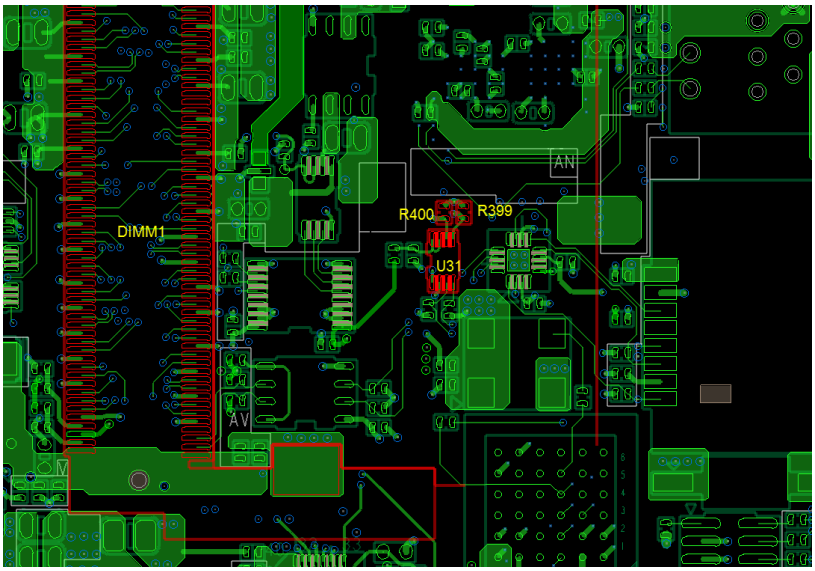
2. EVMK2HX Rev 1.1 Known Issues

2.1 EMAC Link Down Issue

- Description: Noise on MDCLK signal impacts stability of the MDIO link. When Linux kernel sees MDIO link go down it tears down data link as well. Have not seen an issue with using MDIO link to configure external PHY.

- Workaround: Different options under investigation.
  1. Modify code not to depend upon MDIO link remaining active for EMAC communication
  2. Add stronger pull-up resistors on MDCLK and MDIO signal, by replacing R399/R400 from 4.7 kohm with 220 ohm resistors (0402 sized)





- Plans for a fix: Will clean up routing of MDCLK signal on Rev2.0. BOM will also be changed on future builds to incorporate 220ohm resistor pull-up changes.

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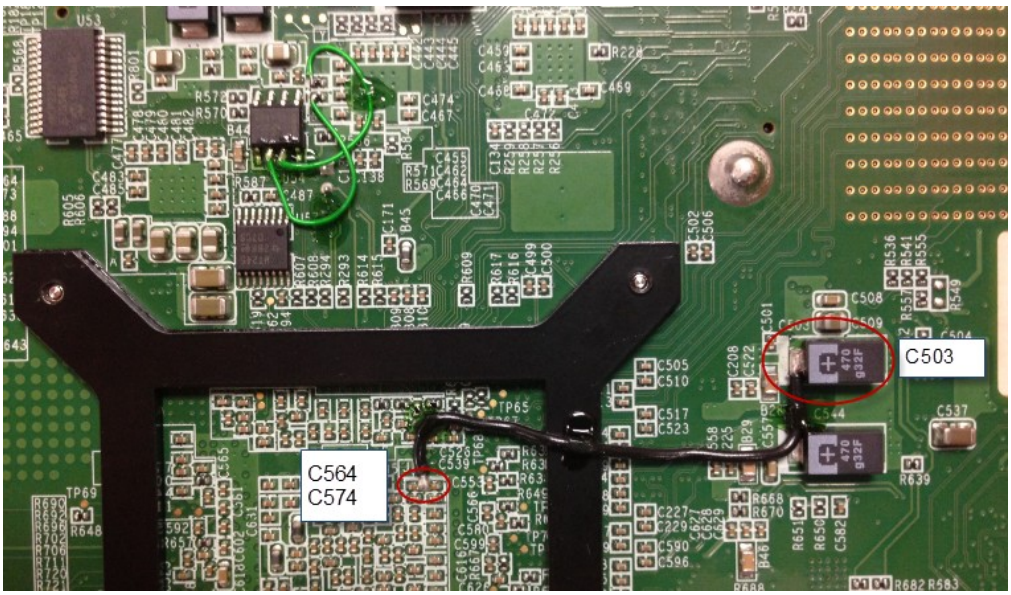
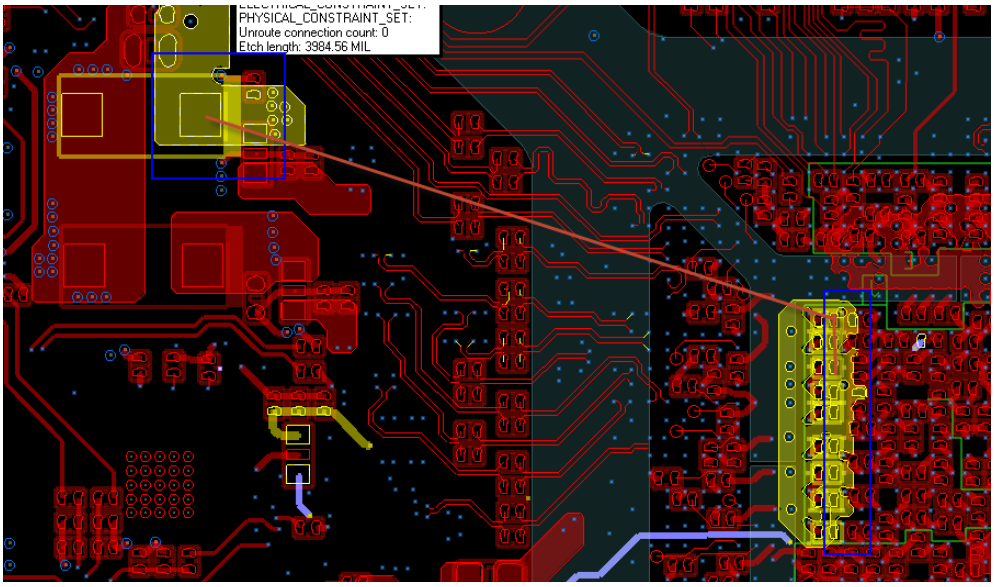
2.2 VCC0V85 Voltage Drop Issue

- Description: The trace width of the VCC085 signal is too narrow and causes a voltage drop at the pin of the SOC. Since this supply is used for SerDes interfaces it could cause SerDes interfaces to lose link. This issue has only been identified and observed on the SGMII.
- Workaround: A couple different options are still under investigation for their effectiveness.
  1. Add external wire to provided adequate patch for expected current from pin 1 of "C503" (net VCC0V85) to pin 1 of "C564, C574" (net VDD0V85). (Wire length = 5 cm)



Note: That the rework should not link to GND and cause short circuit.



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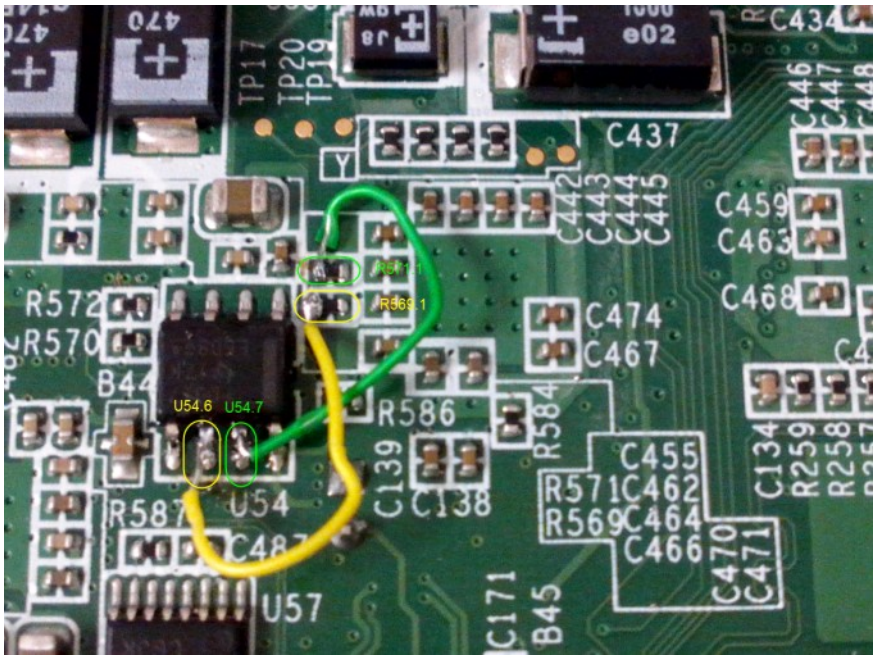
- Plans for a fix: The trace width will be fixed on Rev2.0. The filter element on AVDDALV requires an increased current capacity (suggest up to 4A) to allow for margin on worse-case power as per latest Snowbush power estimates when all SERDES are active. Increase of current capacity on filtering elements for AVDDAHV also recommended (suggest up to 3A). Please see latest estimates below. CVDD power budgeted already on the DSP AVS supply. Both of these nets shall be implemented as copper pours up to the filters and as a plane afterwards to minimize resistance and inductance and maximize plane capacitance.

	AVDDAS (0.85V)	AVDDHVS (1.8V)	CVDD (AVS)	Unit
Total per Kepler	2.951016043	1.274949495	0.005754011	A

2.3 I2C SDA/SCL Reserve Issue

- Description: SCL and SDA are swapped on U54 bus repeater. Impacts I2C going to 120p Expansion Connector and Zone 3 RTM connector.

- Workaround: Cut the jumper wire (30AWG) to swapped signal of EXP_SDA2_3V3 and EXP_SCL2_3V3. Two wire each to similar yellow and green to link from U54.6 to R569.1 and U54.7 to R571.1 .



- Plans for a fix: This will be corrected on Rev2.0.

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2.4 Incorrect UCD Setting

- Description: An invalid 'over current' setting in one of the UCD power management devices can cause the EVM to shut down when the SOC is heavily loaded.
- Workaround: Follow instructions on MCSDK wiki to perform a field update to get your UCD settings to the proper value. (http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update)
- Plans for fix: The correct configuration will be programmed in future builds of EVMs.

2.5 SOC Power Fail

- Description: During power on of the board the UCD controller will detect a fault and will abort the power on sequence
- Workaround:
  1. Occasionally a successful "power on" will occur if multiple power cycles are performed.
  2. A script is in development to enable a field update to correct the UCD settings. (http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update)
- Plans for a fix: Correct configuration will be programmed in future builds of EVMs

2.6 USB3.0 Performance

- Description: Lack of AC coupling and in-signal shunts for ESD protection can impact functionality by causing the link to intermittently go down or never come up.
- Workaround:
  1. Remove choke B26 , and add AC capacitors C839, C840 (0.1uf)
  2. Connect the EN pin of the USB power switch (U59) to USBDRVVBUS pin of SoC (U24) through R809 (10ohm). (USBDRVVBUS pin on U59 is used by the USB state-machine to control the VBUS supplied to the Type A connector)
- Plans for a fix: Expected to be fixed in future builds of EVMs

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3. EVMK2HX Rev 1.1 Hardware Modifications

Rev 1.1 EVM keeps the schematics and PCB layout same as Rev 1.0 EVM, but following BOM change and reworks are made in Rev 1.1 EVMs for better stability.

3.1 EMAC Link Down Issue

- Workaround: R399 and R400 are changed from 4.7 kohm to 220 ohm resistors (0402 sized) in Rev 1.1 EVM.

3.2 VCC0V85 Voltage Drop Issue

- Workaround: An external wire is added to provided adequate patch for expected current from pin 1 of “C503” (net VCC0V85) to pin 1 “C564, C574” (net VDD0V85). (Wire length = 5 cm). Also, the wire is glued on heat sink back plate for stability.

3.3 I2C SDA/SCL Reserve Issue

- Workaround: External rework wires (30AWG) are added to swapped signal of EXP_SDA2_3V3 and EXP_SCL2_3V3.

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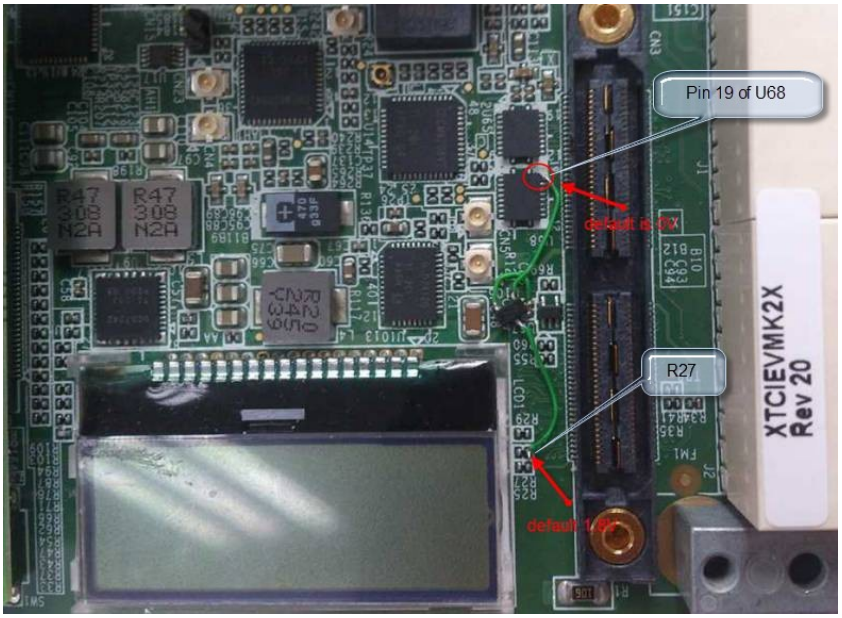
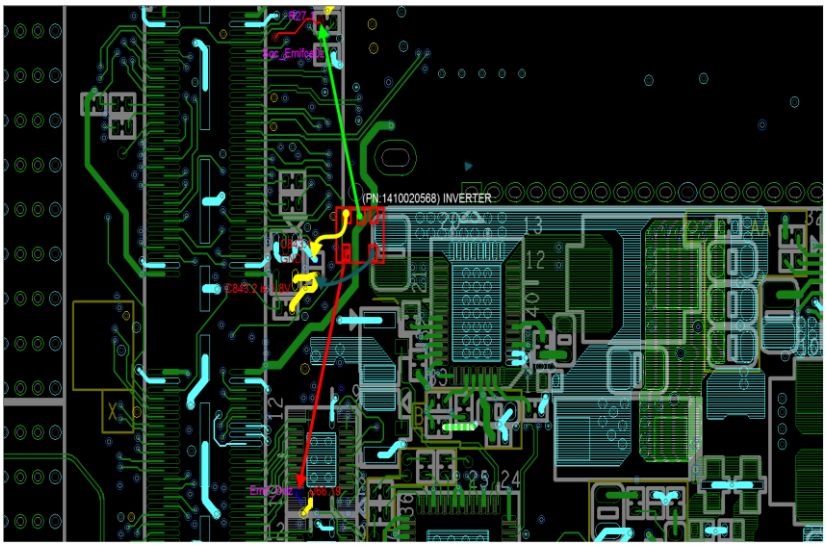
4. EVMK2HX Rev 2.0 Known Issues

4.1 EMIF and NAND Test cannot be synchronized

- Description: SoC could not access NAND flash through EMIF interface, and there will be one cause data transmission errors.
- Workaround:
  1. Add inverter (SN74LVC1G04DVR).
  2. Add wire (30AWG) from inverter PIN 3 to C843.1 (GND),
  3. Add wire (30AWG) from inverter PIN 5 to C843.2 (VCC1V8)
  4. Add wire (30AWG) from inverter PIN 2 to R27.1 (SOC_EMIFCE0Z)
  5. Add wire (30AWG) from inverter PIN 4 to U66.19 (EMIF_OEz).





- Plans for a fix: The rework is installed on all Rev 2.0 board before shipping.

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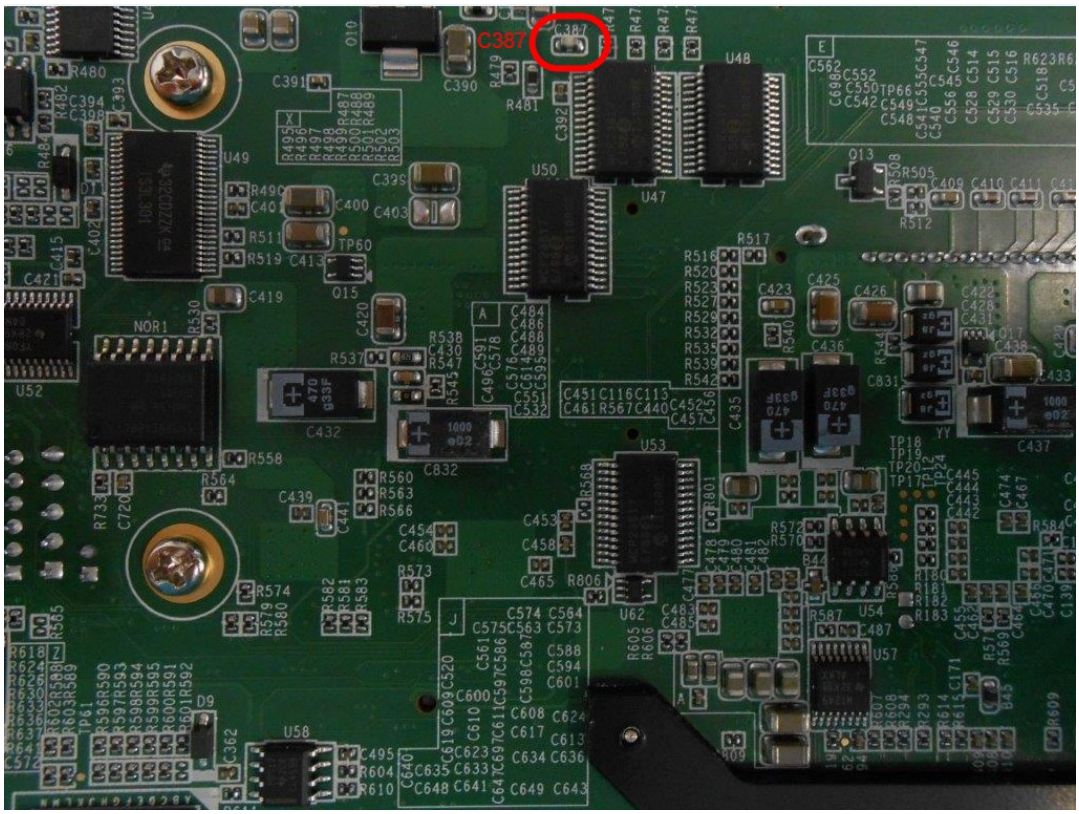
4.2 USB Device not work

- Description: USB 3.0 port could not work even Linux kernel loaded. The cause is 5V rail turned off due to overshoot/undershoot protection.
- Workaround: A couple different options are still under investigation for their effectiveness.
  1. Increase 5V overshoot/undershoot margin in with UCD9090 XML File (UCD9090_104_A04.XML) in TI Fusion Power Manager Tool so 5V rail would not be turned off.
  2. Remove C387 (56pf) extra capacitor on 5V rail to solve overshoot/undershoot symptom.



- Plans for a fix: C387 will be removed in next revision EVM. User could remove C387 or apply updated xml file to solve the symptom.

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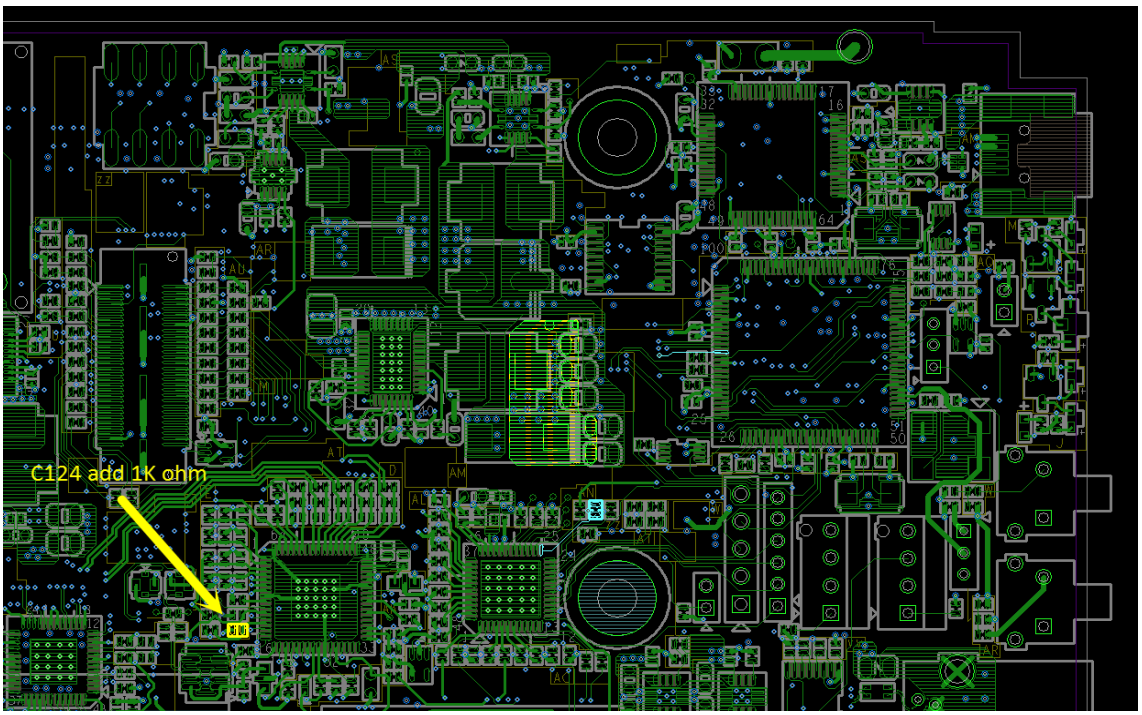
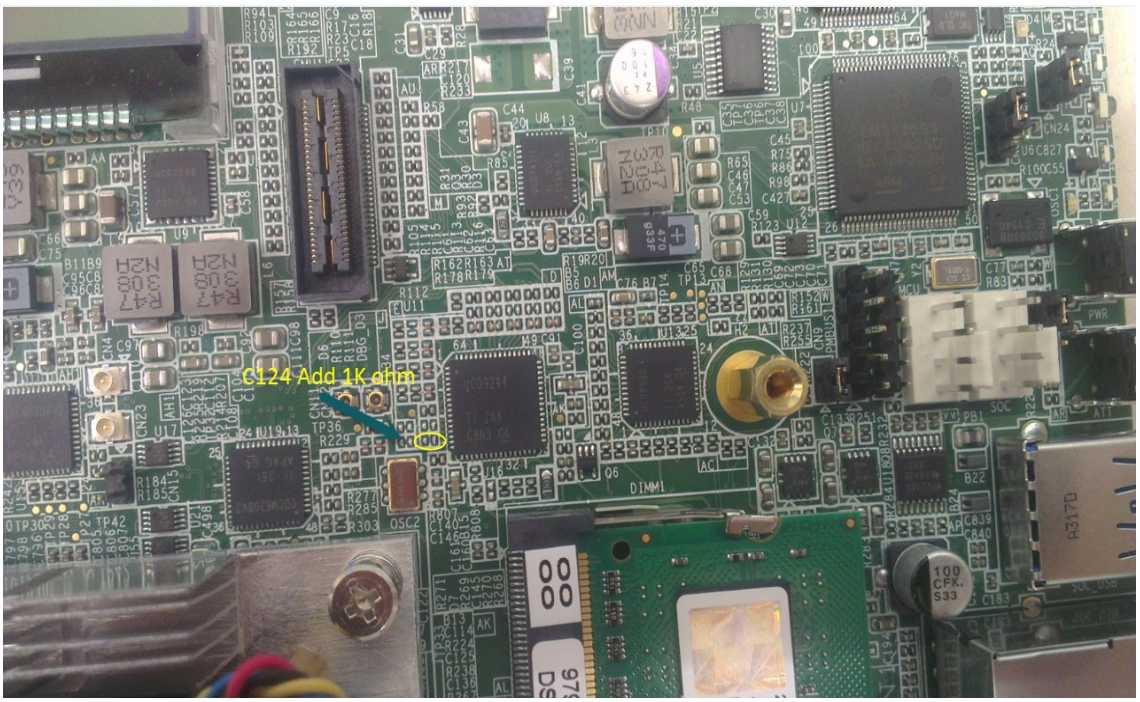
4.3 Power up will happen SoC PWR stop

- Description: UCD controller detects a fault during power-on and aborts the power-on sequence.
- Workaround: The fault comes from un-used CVDDT rail and FLT pin is floating. Adding a 1K ohm resistor on location C124 will pull-down the un-used FLT pin and avoid false fault signal.





- Plans for a fix: The 1Kohm resistor is added before Rev 2.0 EVM shipping.

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5. EVMK2HX Rev 2.0 Hardware Modifications

The schematics and layout design are modified for Rev 2.0 EVM, and major items are described as below:

5.1 Design Changes:

1. Combine CVDD and CVDDT power rail
2. Change Boot resistor R116, R117, R468 from 10 ohm back to 0 ohm
3. Swap nets EXP_SCL2_3V3 and EXP_SDA2_3V3 on U54
4. Change on-board RAM (U39, U40, U41, U42, U43) from 128Mbit x16 to 256Mbit x16
5. Change EMIF termination resistor to EMIF buffers (U63, U64, U65, U68) for solving signal reflection issue
6. Connect enable pin of USB VBUS switch (U59) to SoC instead of enable directly
7. Rename “VDDAHV” rail to “AVDDAHV”
8. Rename “VDD0V85” rail to “AVDDALV”
9. Modify PCB stack-up so Top/Bottom layers are 1.2 oz (0.5 oz originally) and the inner Power/GND layers are 1.0 oz (0.5 oz originally) in thickness for sustaining larger AC ripple current.

Also, following reworks are installed on Rev 2.0 EVM before shipping:

5.2 EMIF and NAND Test cannot be synchronized

- Workaround:
  1. Add inverter (SN74LVC1G04DVR).
  2. Add wire (30AWG) from inverter PIN 3 to C843.1 (GND),
  3. Add wire (30AWG) from inverter PIN 5 to C843.2 (VCC1V8)
  4. Add wire (30AWG) from inverter PIN 2 to R27.1 (SOC_EMIFCE0Z)
  5. Add wire (30AWG) from inverter PIN 4 to U66.19 (EMIF_OEz).

5.3 Power up will happen SoC PWR stop

- Workaround: Add a 1K ohm resistor on to GND.