A Keystone 2 EVM Board for TI

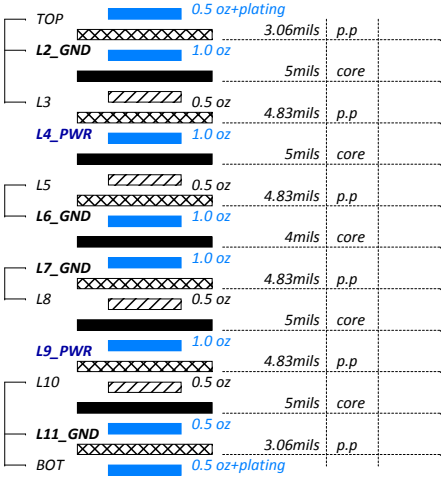
Product name : K2EVM-HK

Rev. 4.0

PCB PN :

Project Code :

PCB Thickness : 63 mils(1.6mm)
12 Layers



DISCLAIMER: THIS CIRCUIT DESIGN IS PROVIDED AS REFERENCE ONLY, WITHOUT WARRANTY EXPRESSED OR IMPLIED. THE USER IS ENCOURAGED TO PERFORM ALL DUE DILIGENCE WITH RESPECT TO DESIGN AND ANALYSIS. FOR COMMITTED PERFORMANCE AND FUNCTIONALITY , PLEASE REFER TO THE DEVICE DATA MANUAL.

NOTE: TI Information – Selective Disclosure

NOTE: EVM design supports multiple devices. Check your device datasheet to determine if a given functionality is supported.

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K2EVM-HK Revision Table

K2EVM-HK (Rev 104-1 / PCB- 19C2830503-01)

Item	Description	Page
1	Update Blockdiagram for EMIF Feature	Page. 05
2	Rserve R812 for Buffer OE control	Page. 13
3	Added Inverter U69 to solve EMIF and NAND read/write issue	Page. 19
4	Adding SN74LVC1G07 Buffer for USBDRVVBUS net	Page. 15
5	Remove C387 for VCC5 feedback compensation optimization	Page. 43
6	Adding R815,R816,R817 Pull down resistance for CLK PDN	Page.25,26,27
7	Change R310 3K to 200ohm for USB PHY PVT sense path	Page.15
8	Change R25 1K to 470ohm for EMIFWAIT0 PU	Page.19
9	Change R116,R117,R468 0ohm to 10ohm for PWR Solution	Page.40,41
10	U39 to U43 DDR SDRAM Change to Samsung K4B4G1646D-BCK0	Page.28, 29

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Title: K2EVM-HK Revision Table I

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Item	Description	Page

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Title: K2EVM-HK Revision Table II

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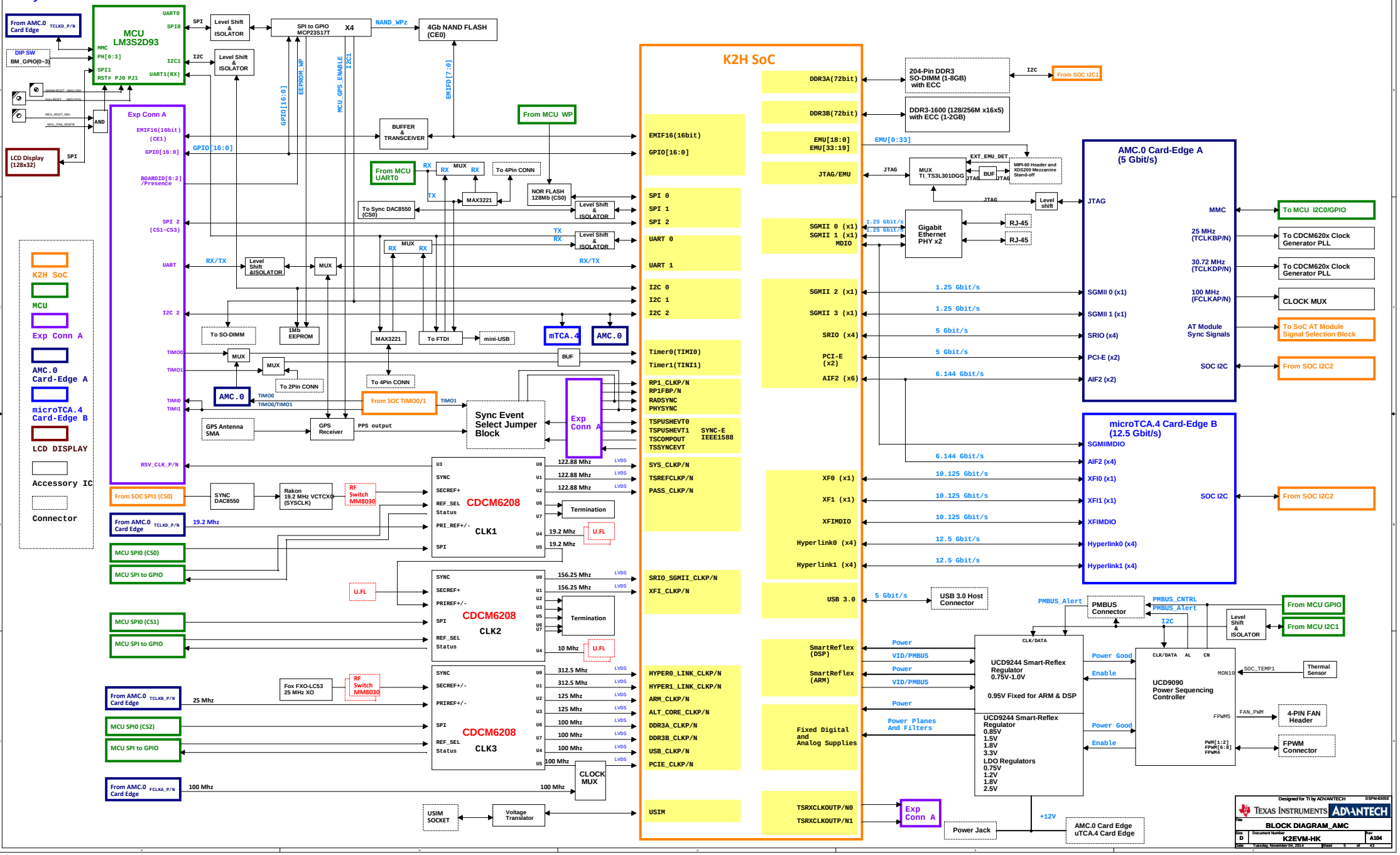
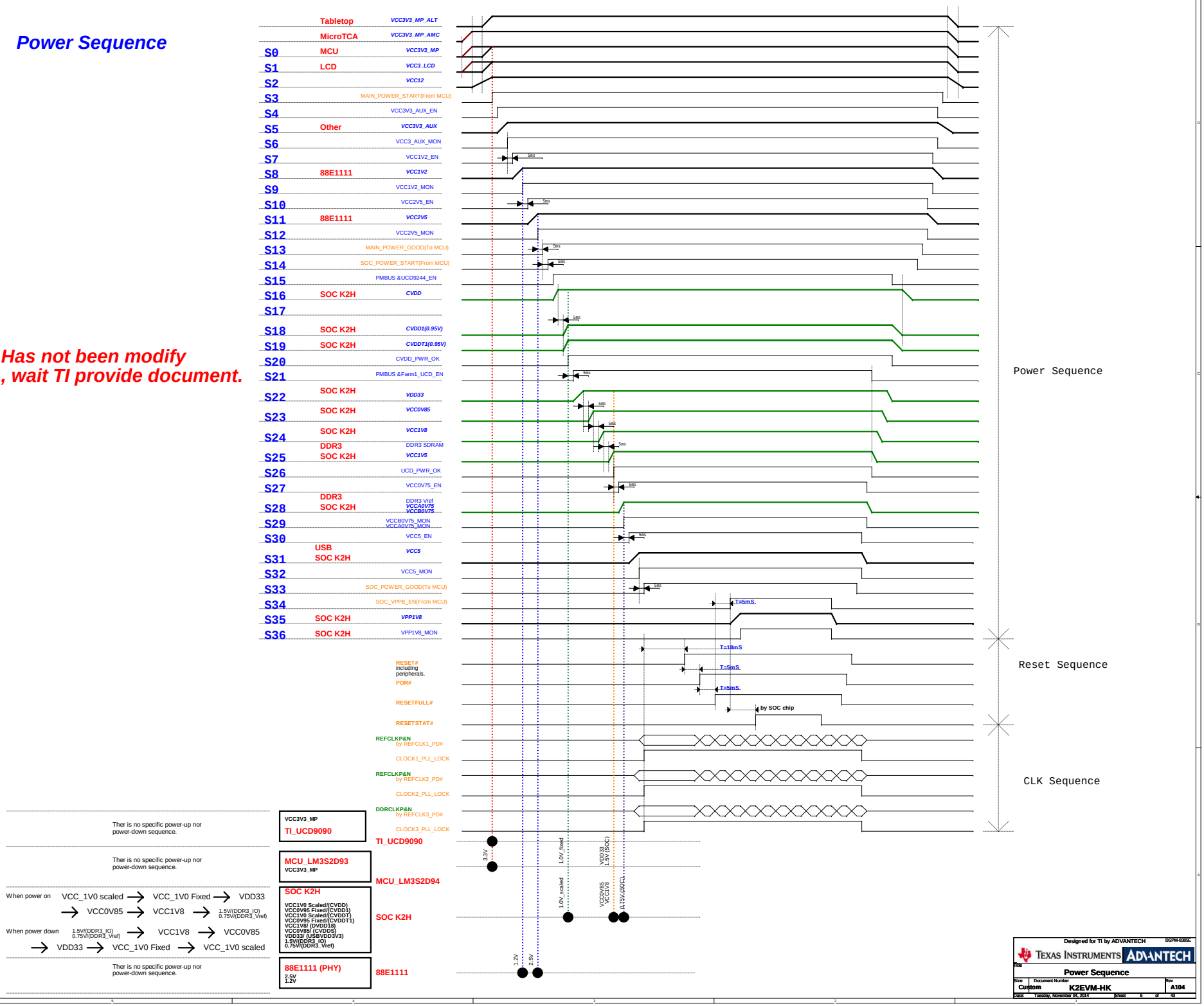
Keystone-2 EVM BLOCK DIAGRAM



Power Sequence

Has not been modify , wait TI provide document.



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DSPM-8355E

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Title: Power Sequence

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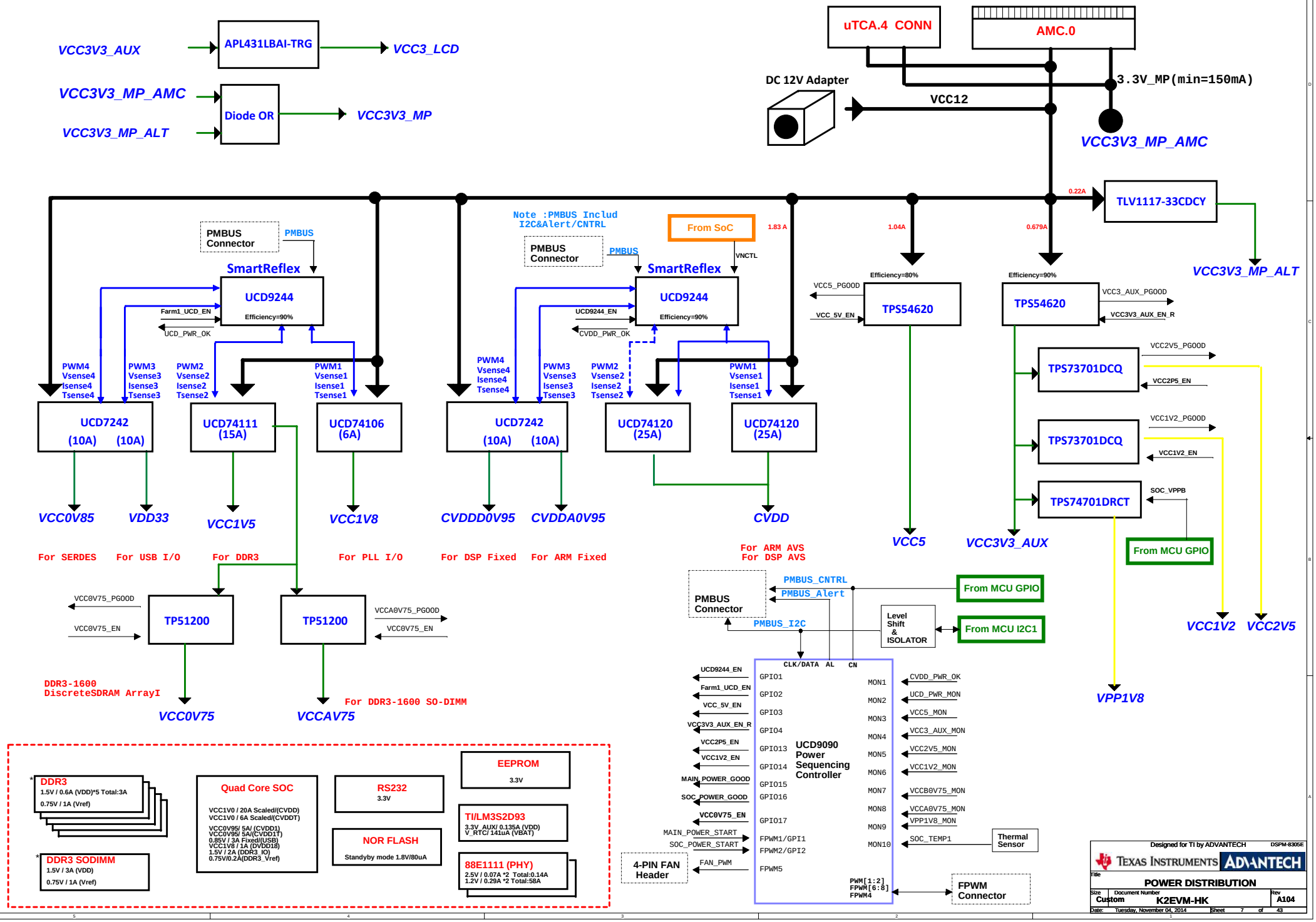
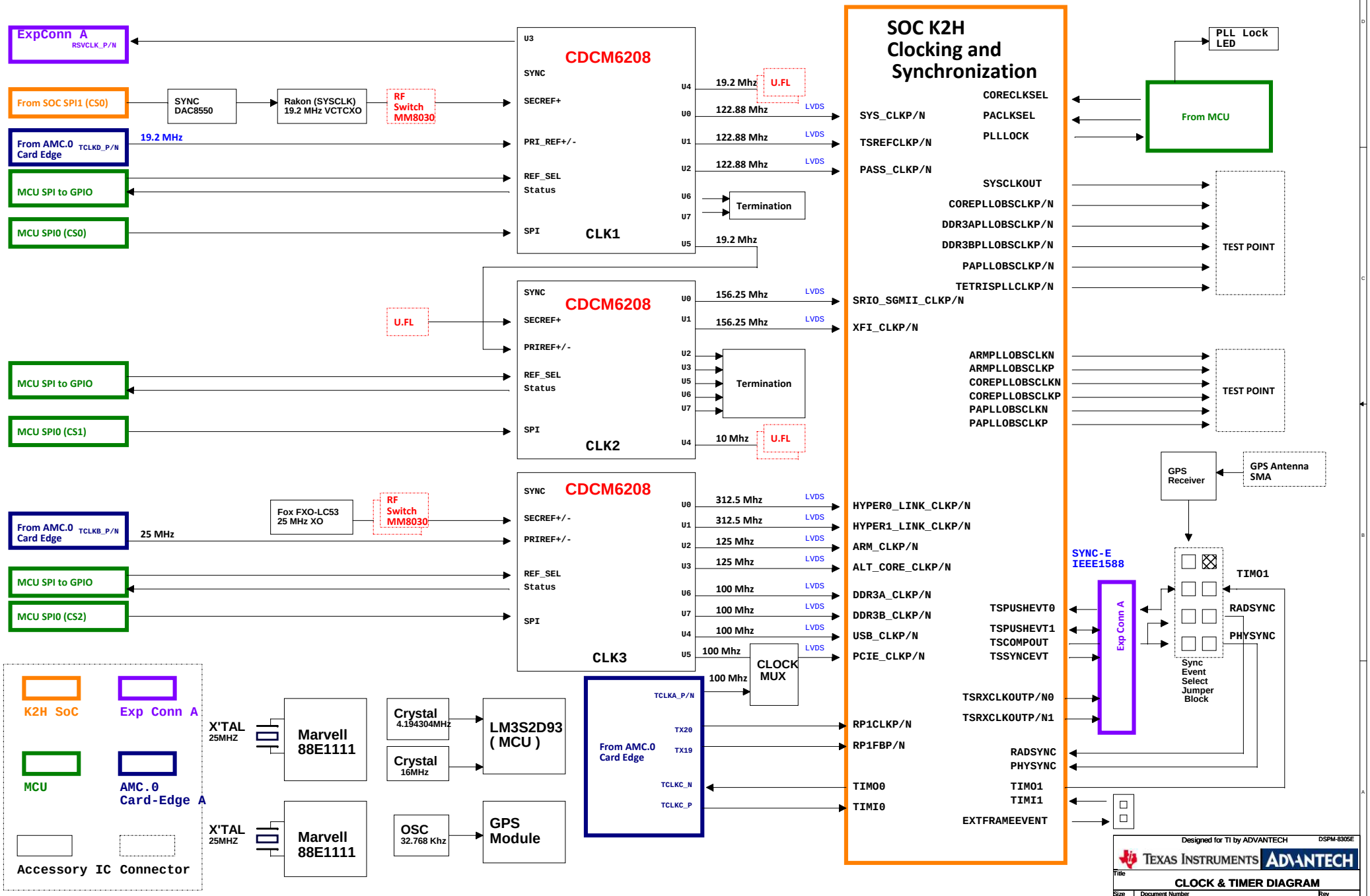
POWER DISTRIBUTION



CLOCK & TIMER DIAGRAM



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TEXAS INSTRUMENTS ADVANTECH

Title	CLOCK & TIMER DIAGRAM	
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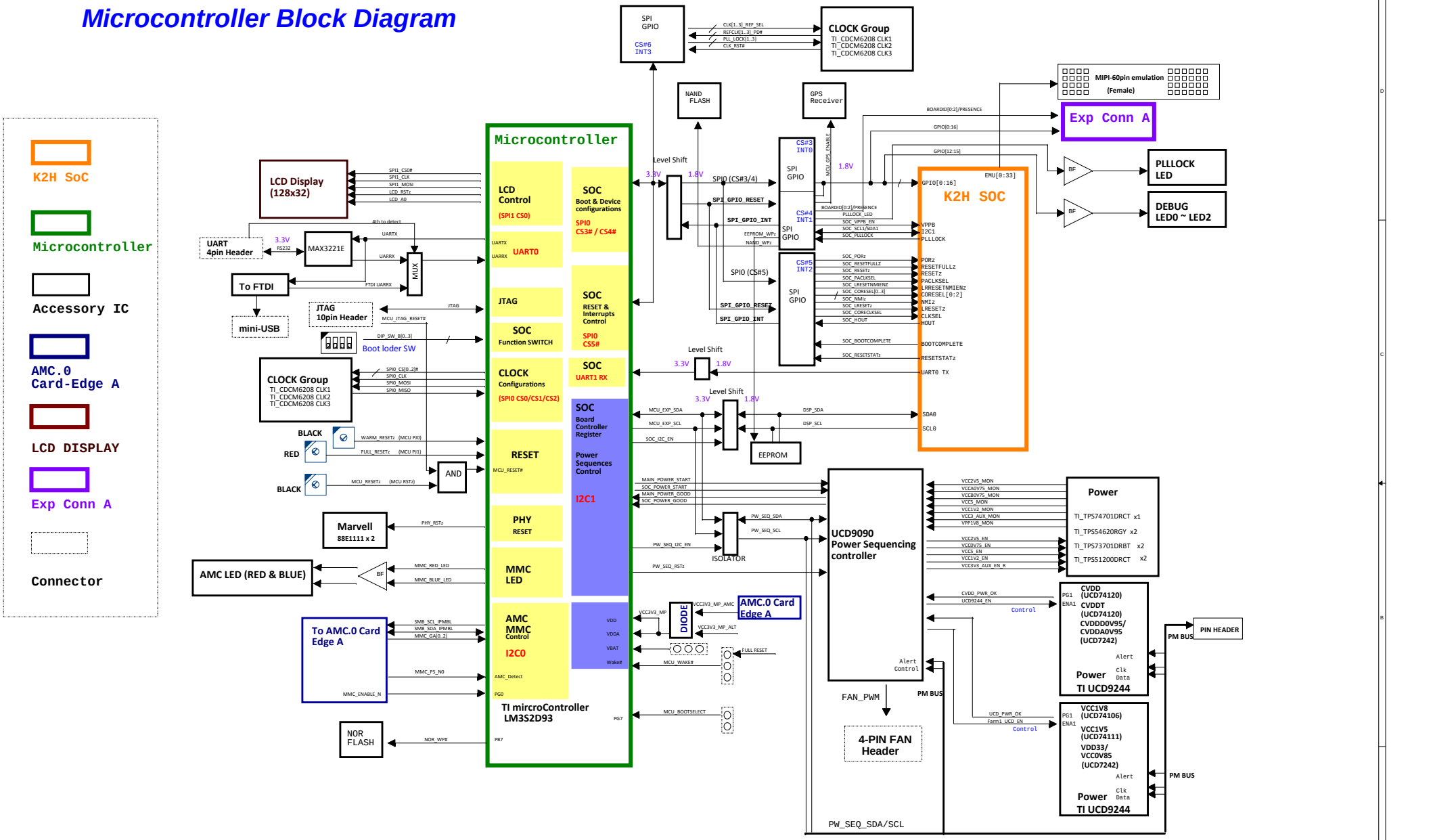
Microcontroller Block Diagram



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Title	Microcontroller Block Diagram	
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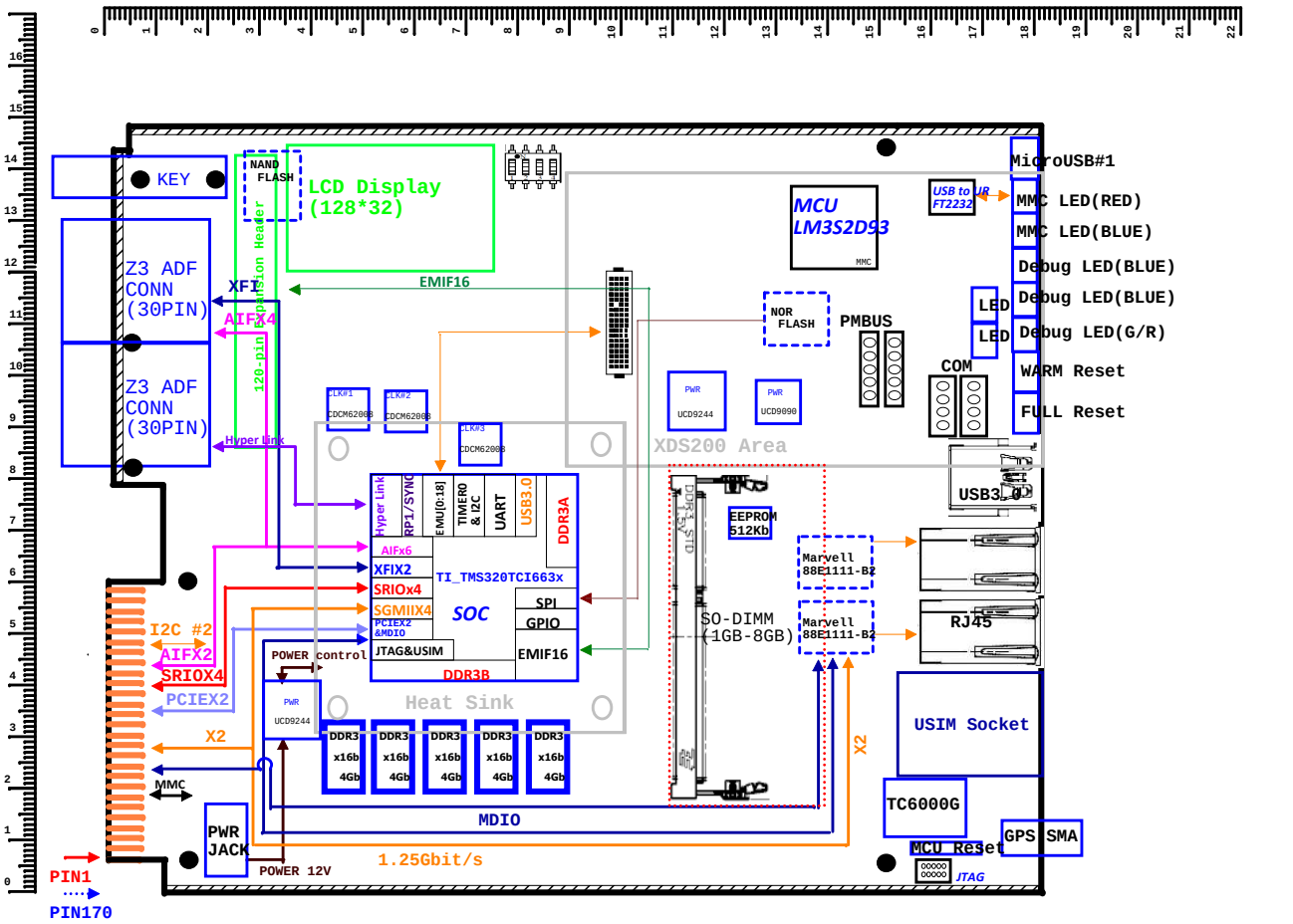
K2EVM-HK EVM PLACEMENT (TOP SIDE)



PCB Half Length = 181.5x148.5mm

Note: Dotted line is Bottom SIDE Component

Note: EVM with K2H device does not support XGMII

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K2EVM-HK Placement			
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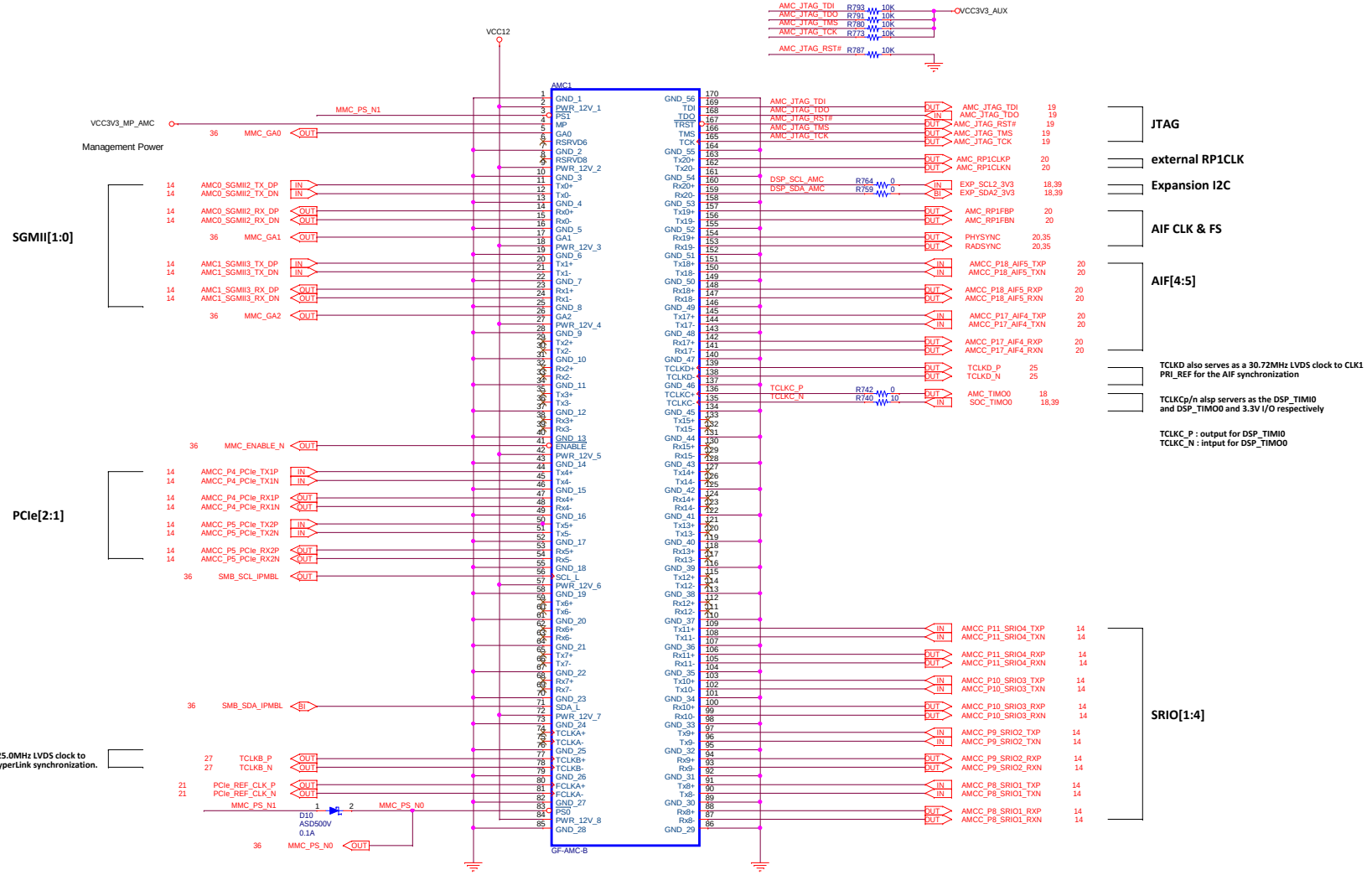

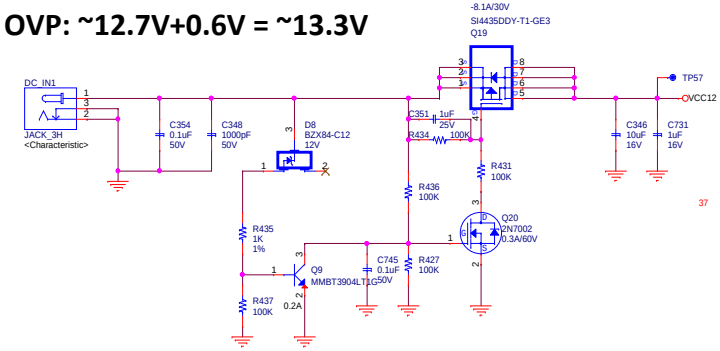

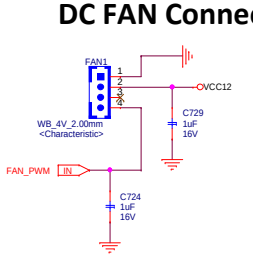

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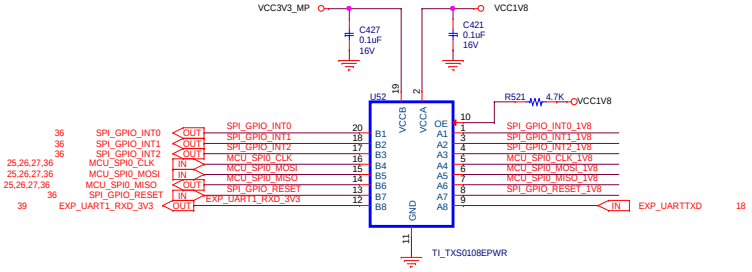
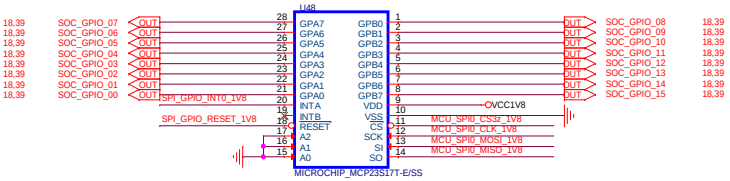
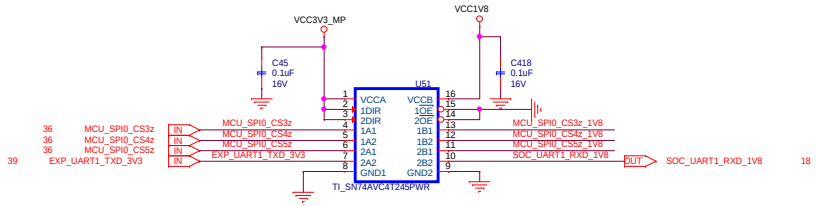
SPI level shift 3.3V <=> 1.8V



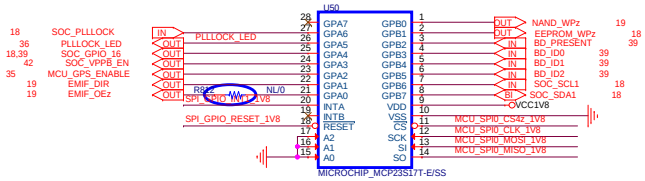
1.8V Level



MicroChip SPI to GPIO

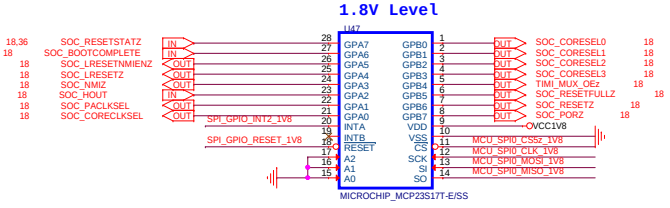


1.8V Level



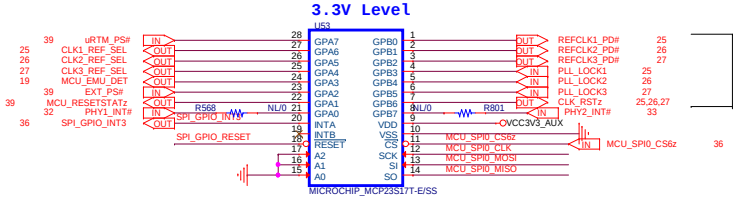
MicroChip SPI to GPIO

1.8V Level



MicroChip SPI to GPIO

3.3V Level



MicroChip SPI to GPIO

CDCM-620X Control

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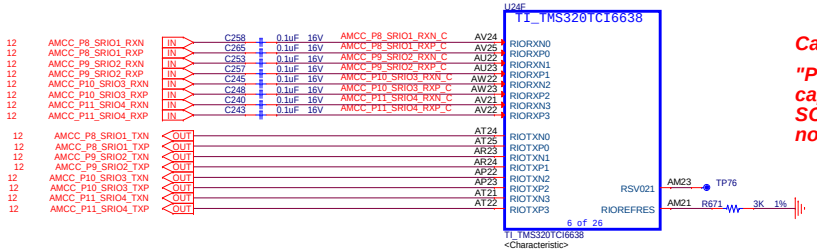
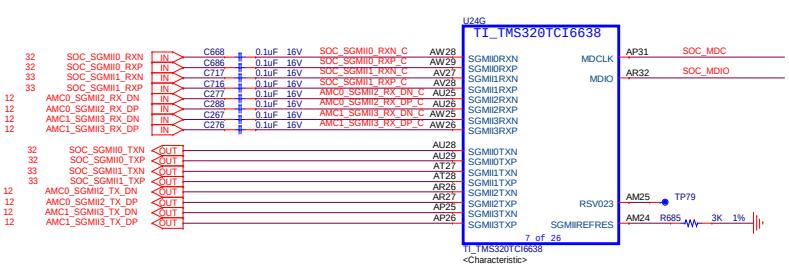
SRIO X4

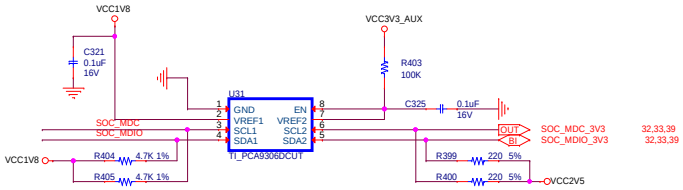


Caution!

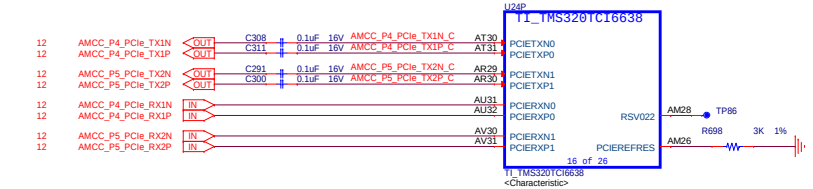
"Place ALL SRIO DC-blocking caps on top layer adjacent to the SOC's RX pins so that there are no additional vias"

SGMII X4





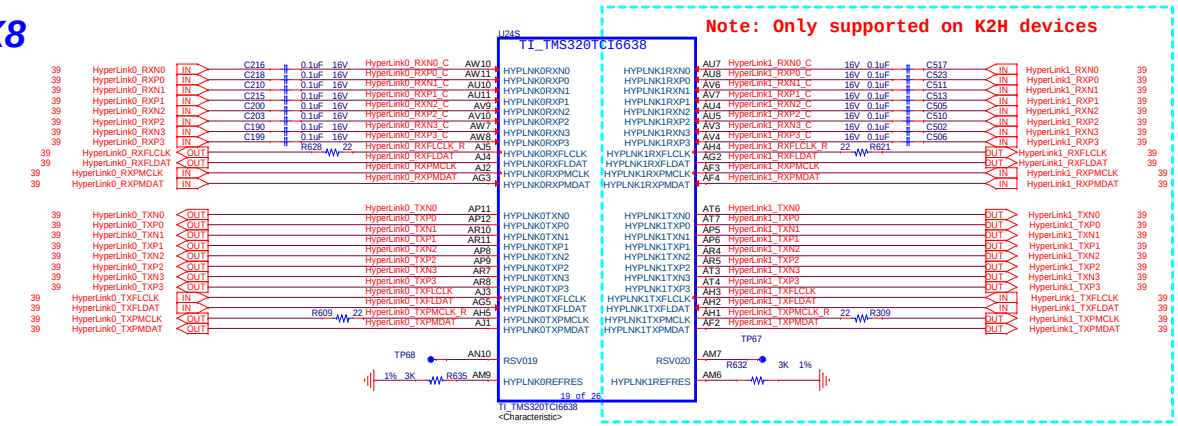
PCIE X2



Caution!

"Place ALL PCIe DC-blocking caps close to the TX pins"

HyperLink X8



"The HyperLink routes should have a maximum of 2 vias and no via stubs – All routes should be on the outer layer of the board."

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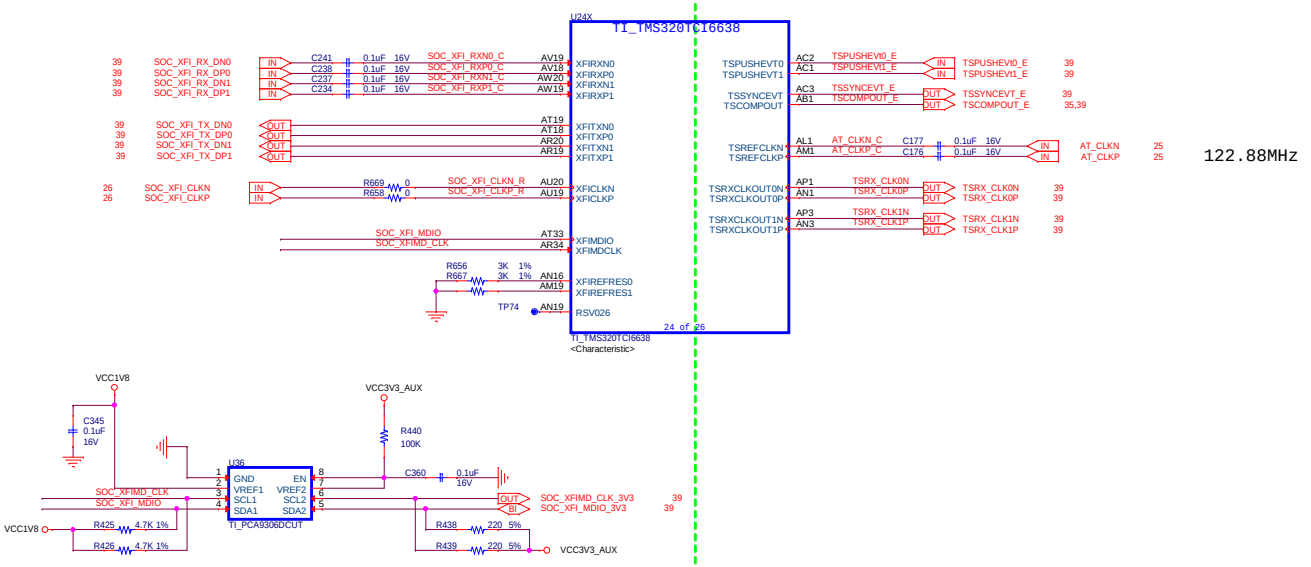
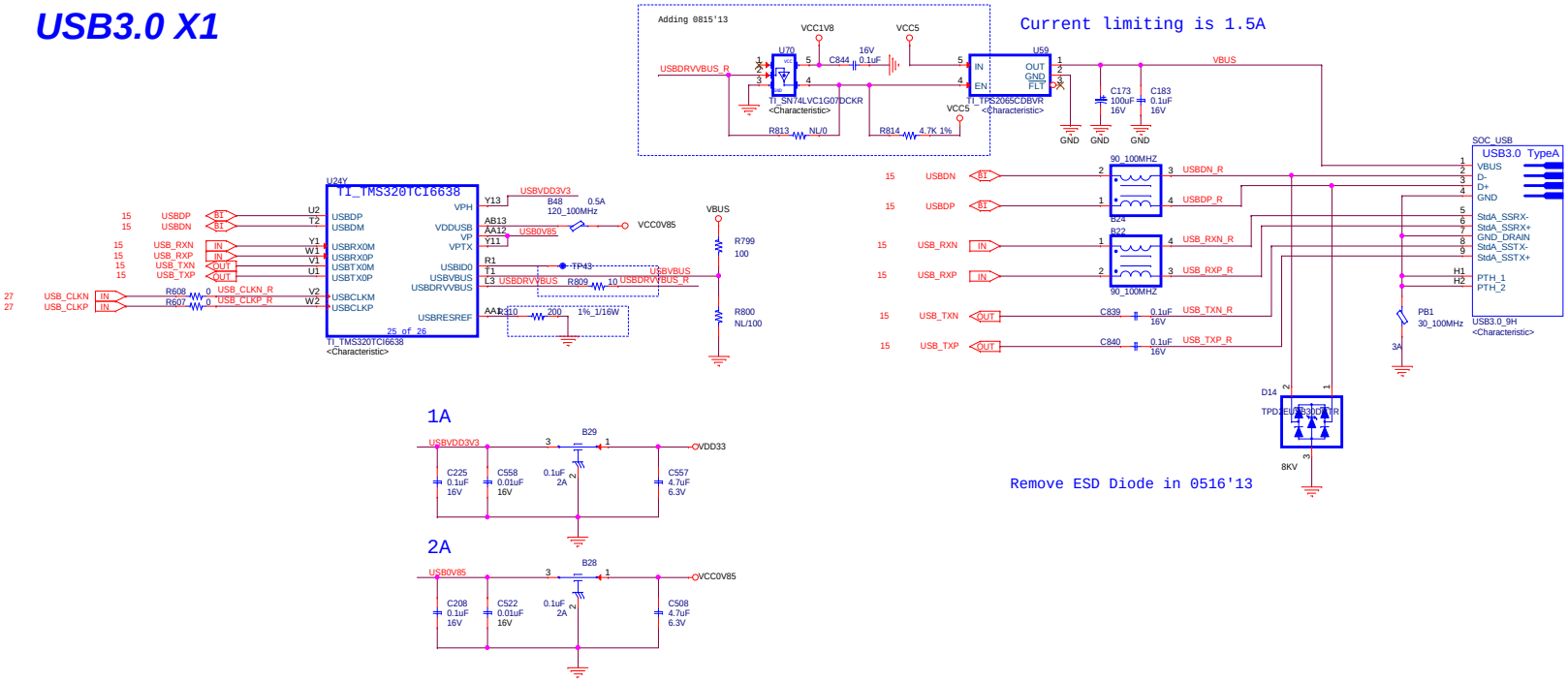
XFI X2

Note: Only supported on K2K devices



USB3.0 X1



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Title: **SOC_XFI_USB**

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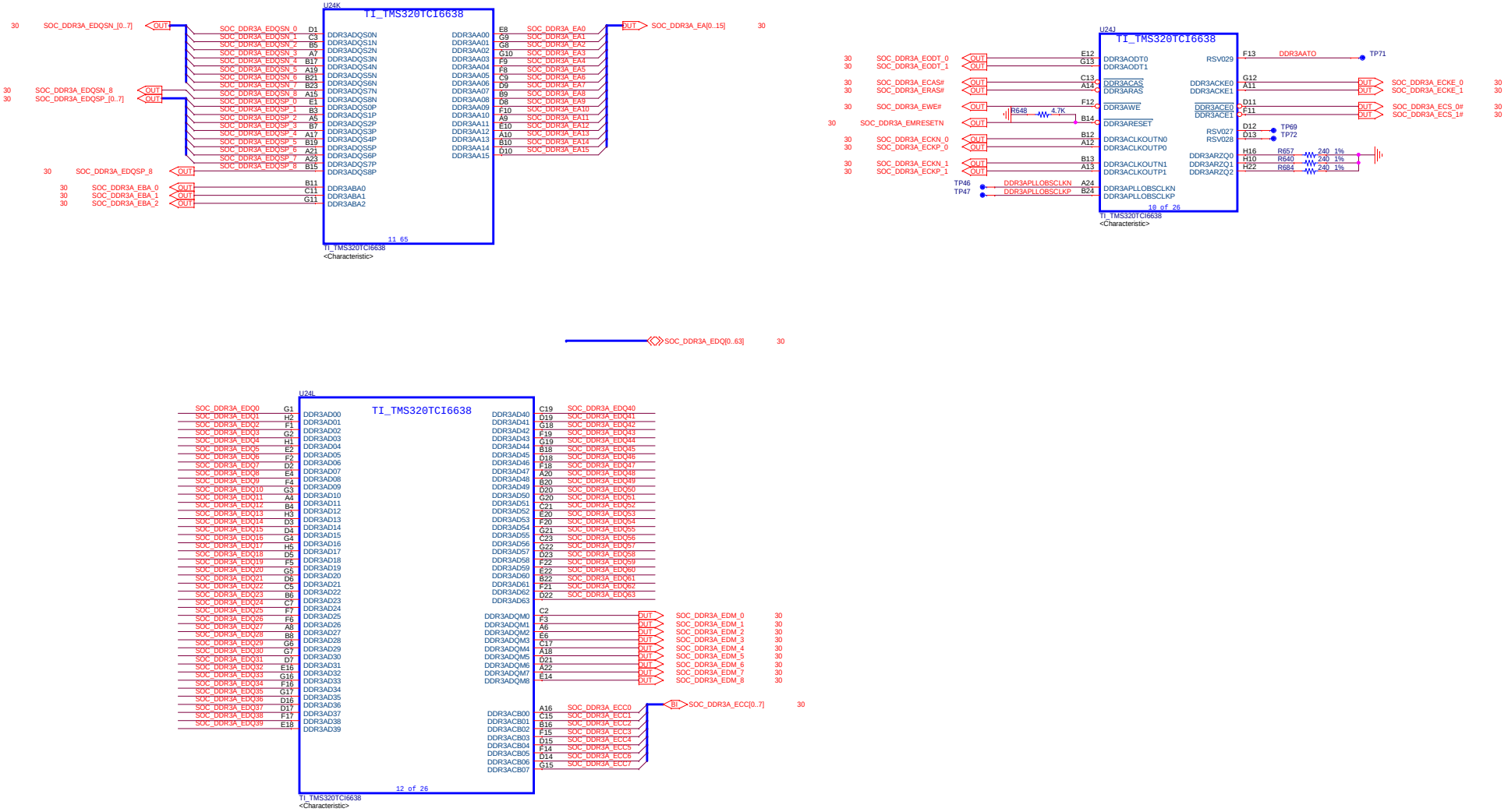
U24K
TI_TMS320TCI6638
SOC_DDR3A_EDQSN_[0..7]
SOC_DDR3A_EDQSP_[0..7]
SOC_DDR3A_EDQSN_8
SOC_DDR3A_EDQSP_8
SOC_DDR3A_EBA_0
SOC_DDR3A_EBA_1
SOC_DDR3A_EBA_2
SOC_DDR3A_EA[0..15]
11 65
TI_TMS320TCI6638
<Characteristic>
U24J
TI_TMS320TCI6638
SOC_DDR3A_EODT_0
SOC_DDR3A_EODT_1
SOC_DDR3A_ECAS#
SOC_DDR3A_ERAS#
SOC_DDR3A_EWE#
SOC_DDR3A_EMRESETN
SOC_DDR3A_ECKN_0
SOC_DDR3A_ECKP_0
SOC_DDR3A_ECKN_1
SOC_DDR3A_ECKP_1
R648
4.7K
DDR3APLLOBSCLKN
DDR3APLLOBSCLKP
DDR3AATO
TP71
SOC_DDR3A_ECKE_0
SOC_DDR3A_ECKE_1
SOC_DDR3A_ECS_0#
SOC_DDR3A_ECS_1#
TP69
TP72
R657
R640
R684
240 1%
10 of 26
TI_TMS320TCI6638
<Characteristic>
SOC_DDR3A_EDQ[0..63]
U24L
TI_TMS320TCI6638
SOC_DDR3A_EDM_0
SOC_DDR3A_EDM_1
SOC_DDR3A_EDM_2
SOC_DDR3A_EDM_3
SOC_DDR3A_EDM_4
SOC_DDR3A_EDM_5
SOC_DDR3A_EDM_6
SOC_DDR3A_EDM_7
SOC_DDR3A_EDM_8
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12 of 26
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SOC_DDR3A
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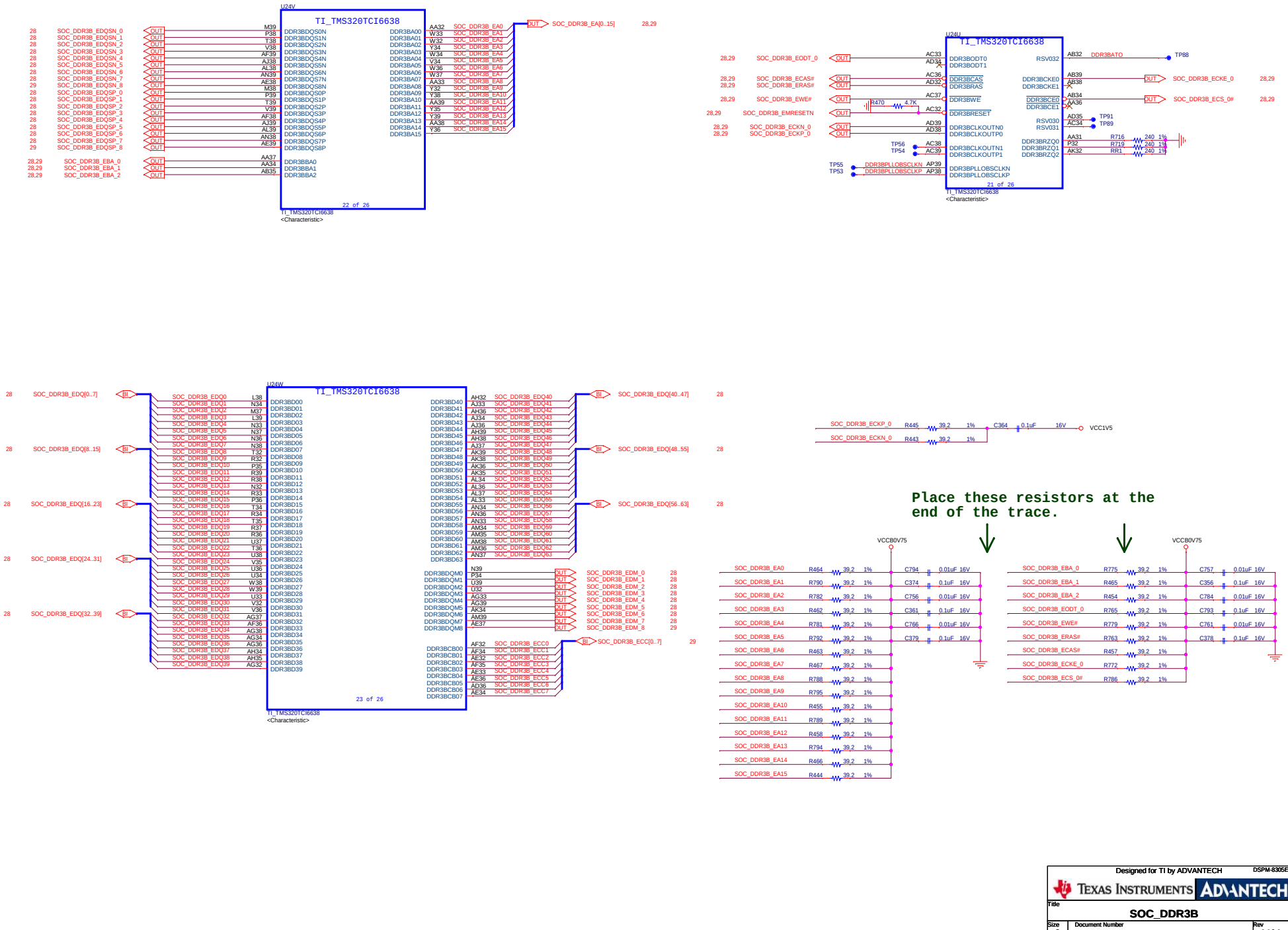

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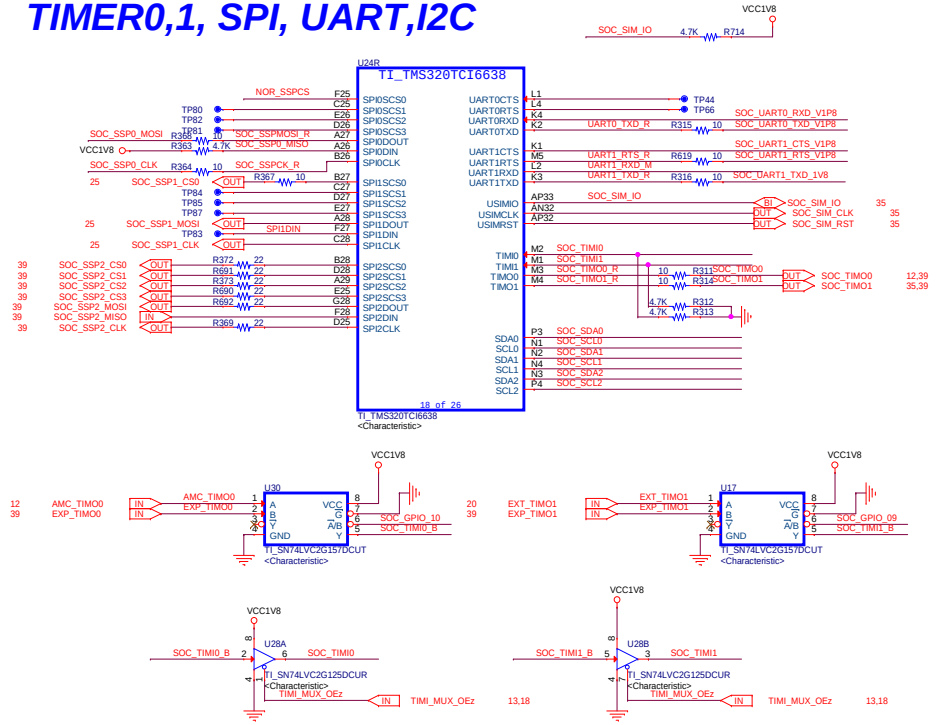
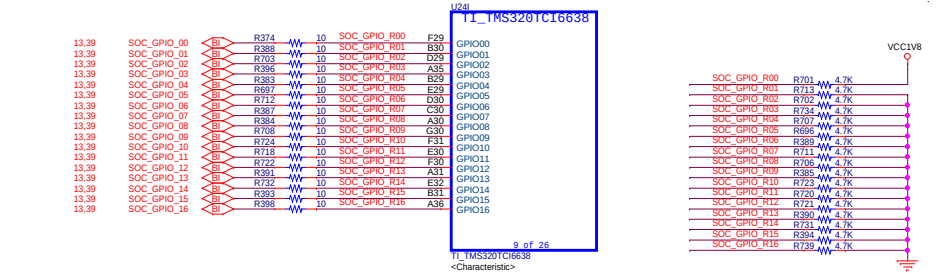
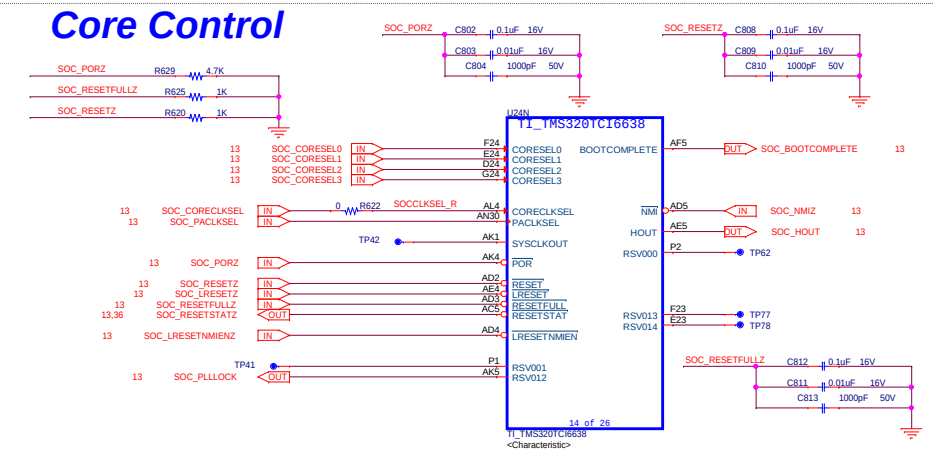
TIMER0,1, SPI, UART,I2C

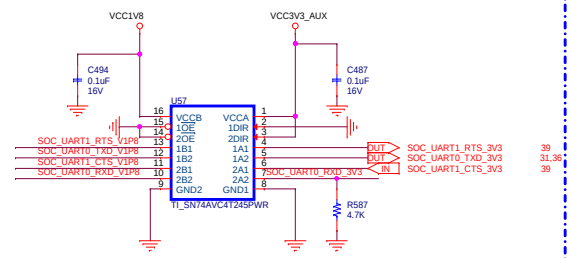


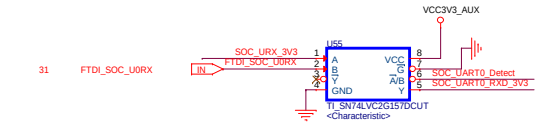
GPIO

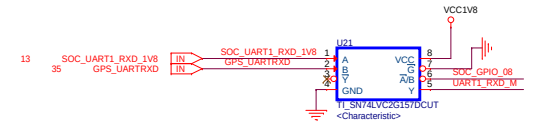


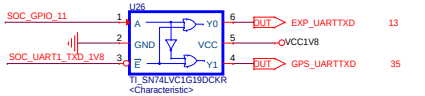
Core Control

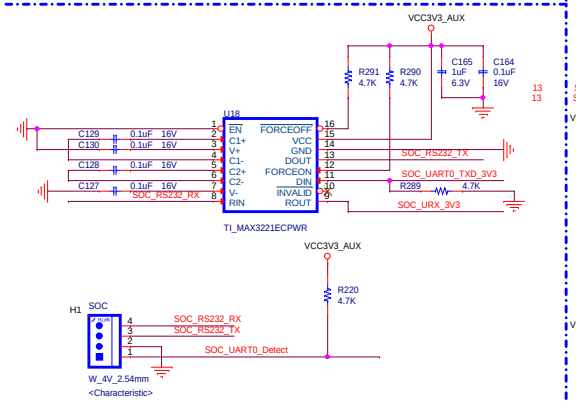


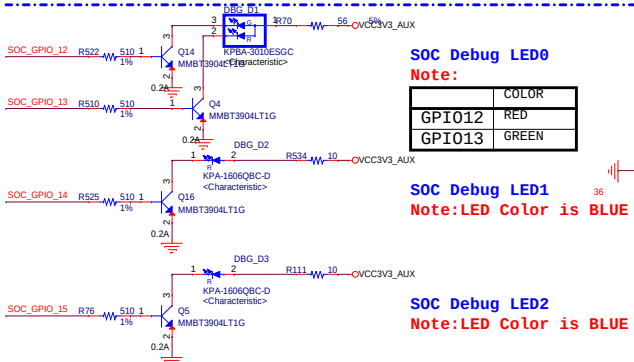


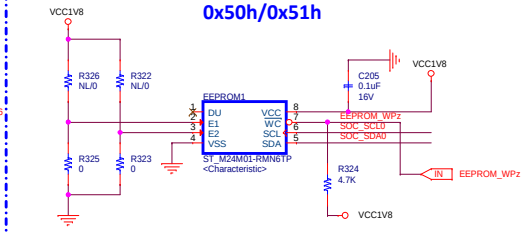


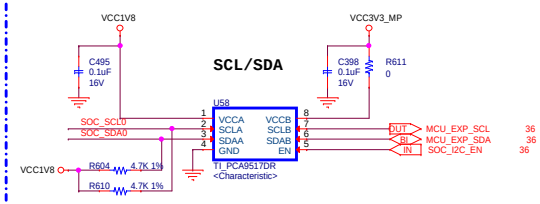


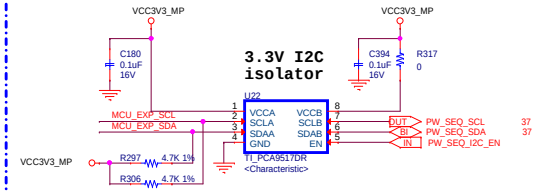


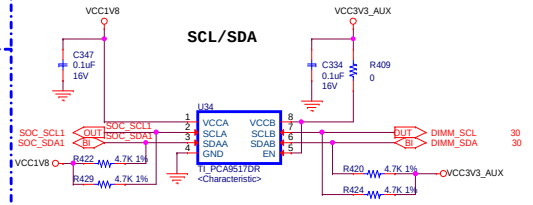


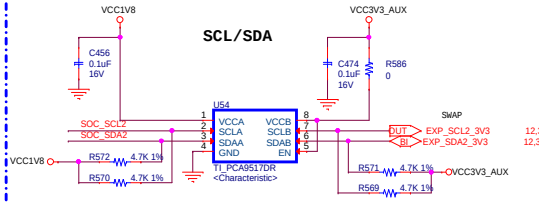


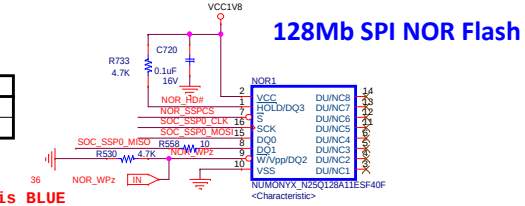












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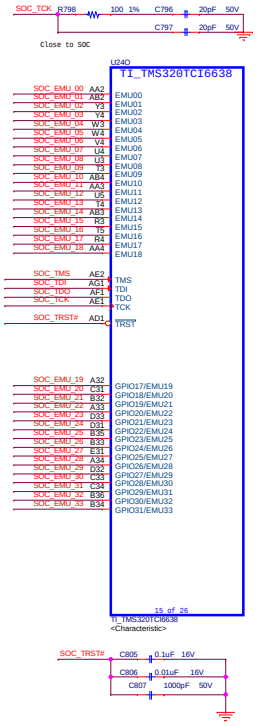
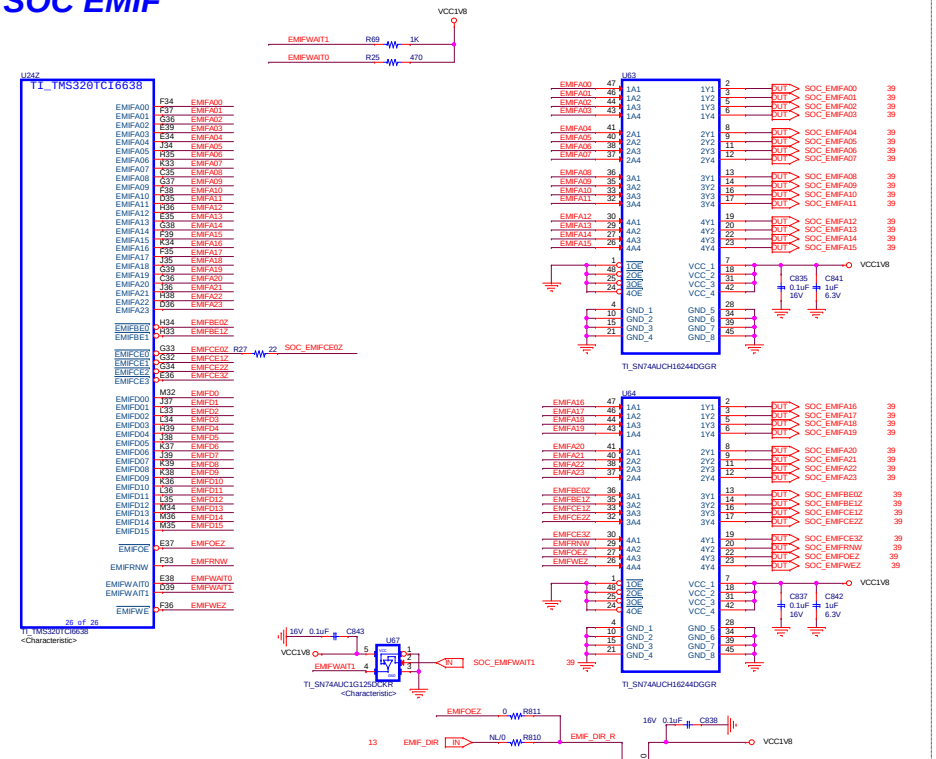
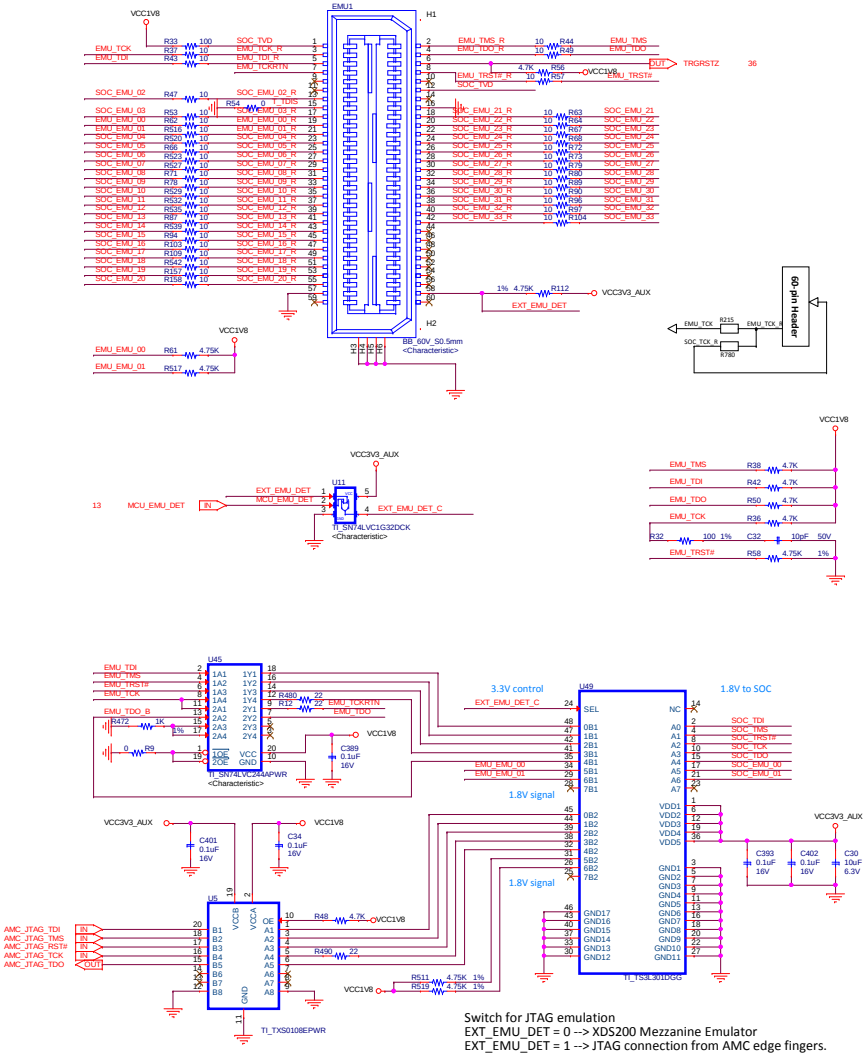
EMU & JTAG



SOC EMIF

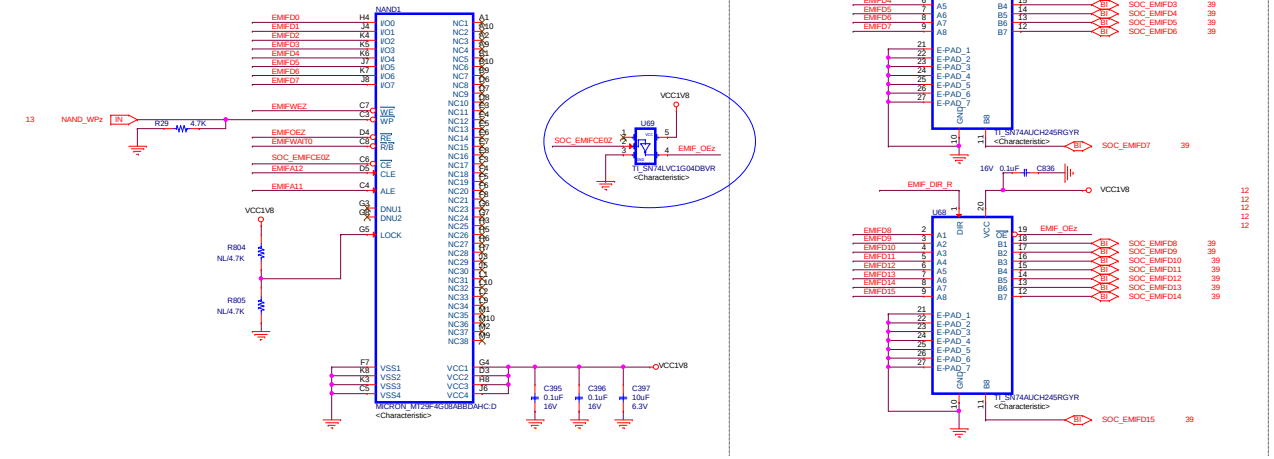


EMU CONN.



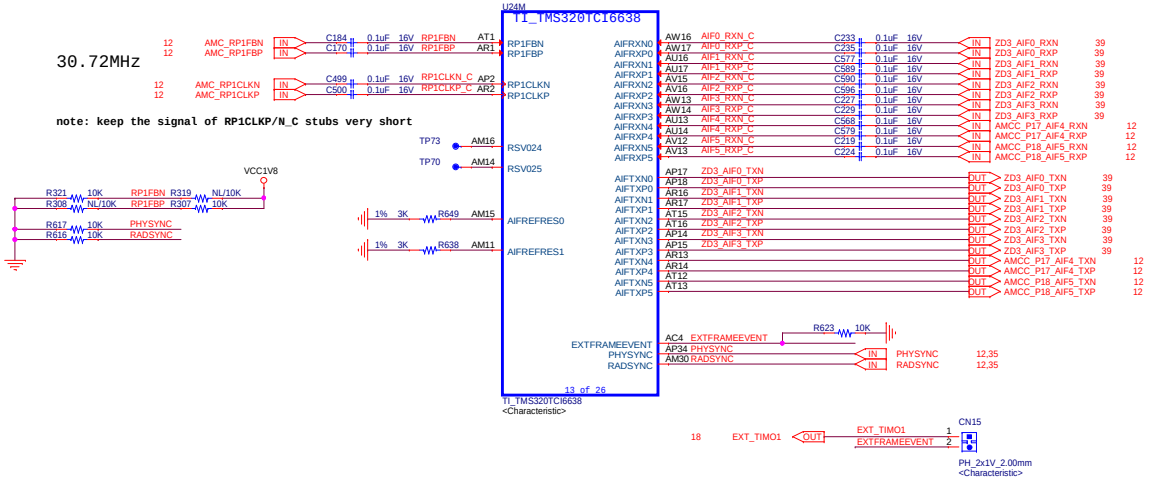
NAND FLASH

Note: NAND FLASH Device size is 4Gb.



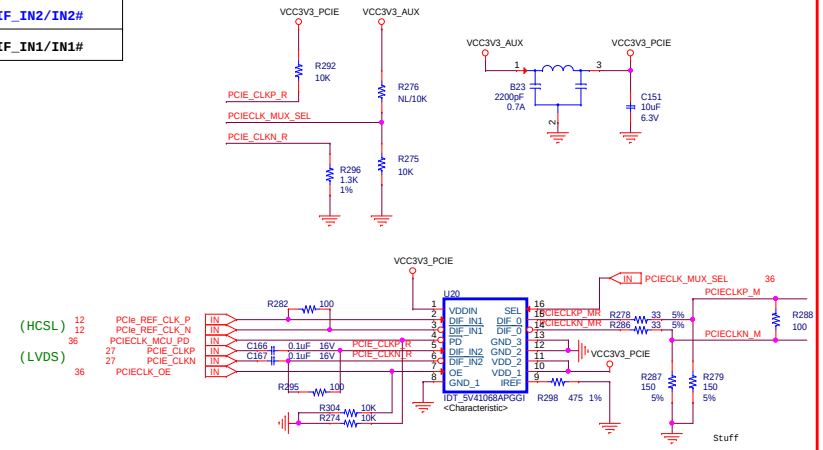
SOC AIF

Note: AIF is only supported on K2H devices

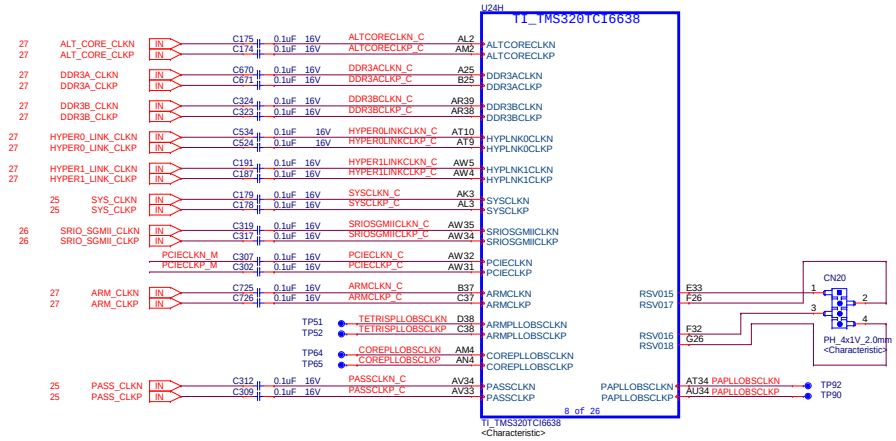


SOC CLOCK / RESET

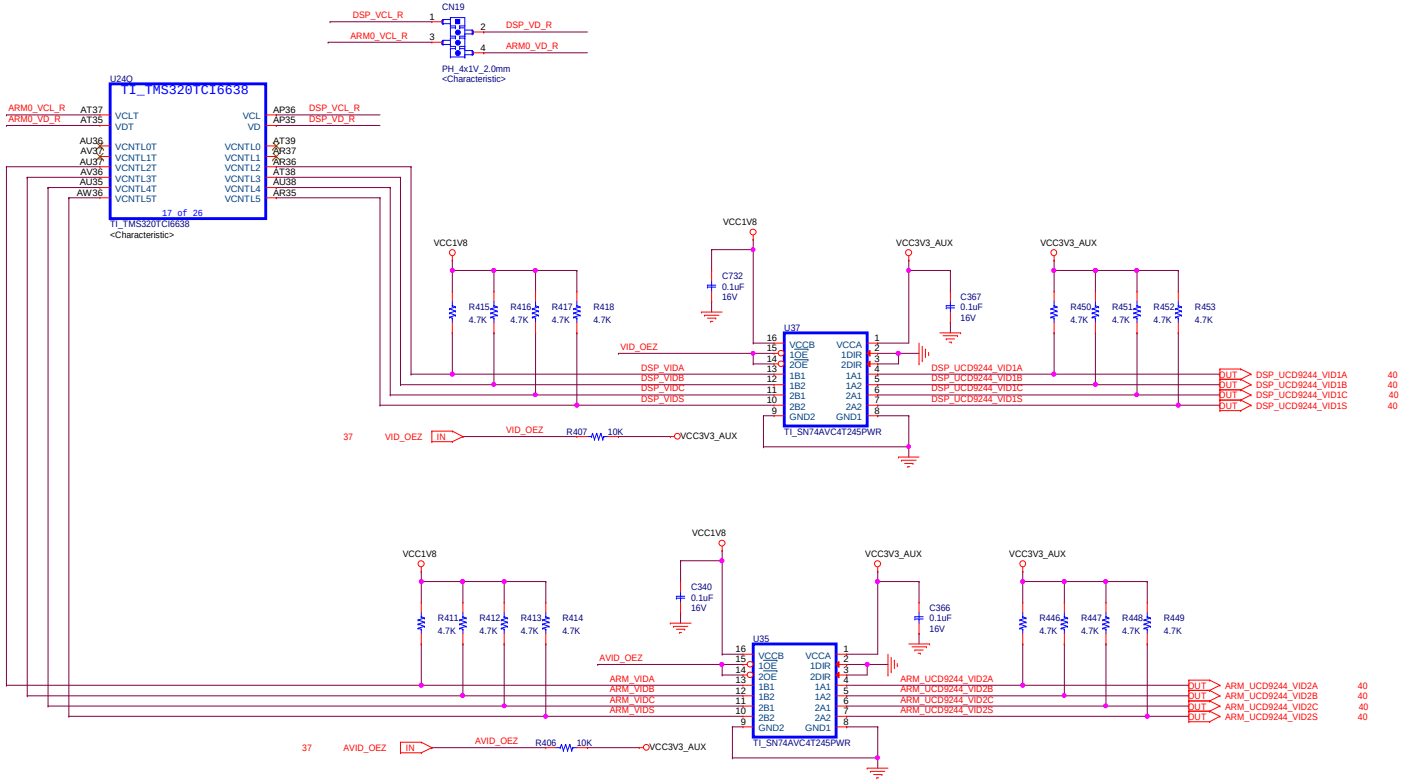
SEL	I/P PAIR SEL
LOW	DIF_IN2/IN2#
HIGH	DIF_IN1/IN1#



All blocking capacitors should be placed near SOC to keep connecting routes short and minimize vias



Smart Reflex



Designed for TI by ADVANTECH			DSPM-8305E
Title	SOC_CLOCK & Smart-Reflex VID		
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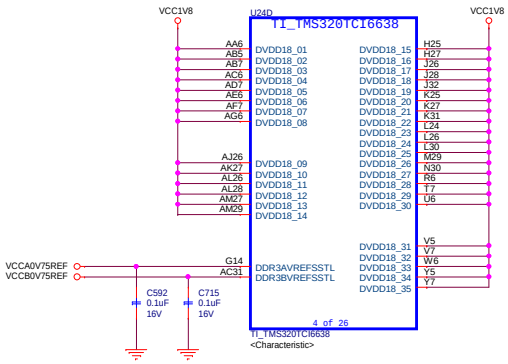
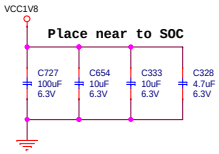
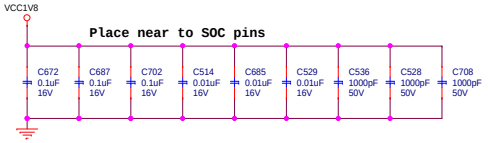
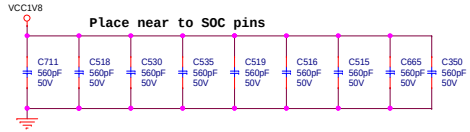
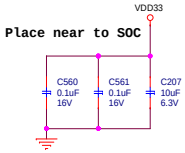
1.8V_1A

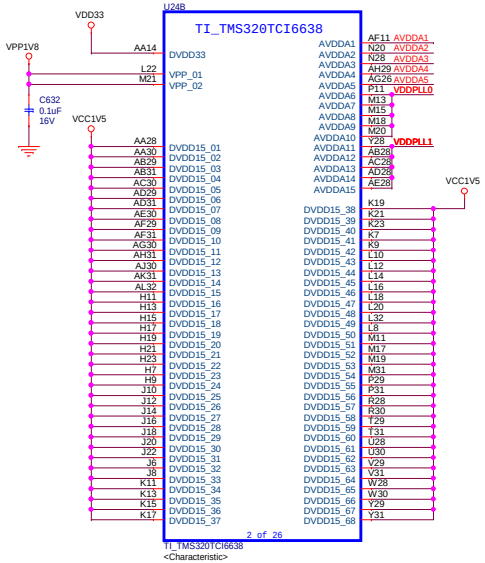


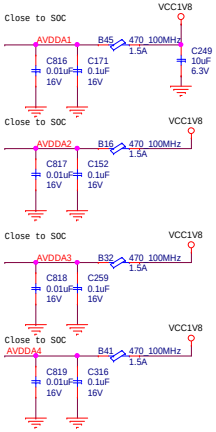


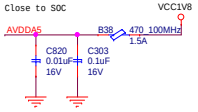


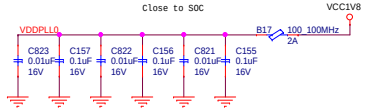


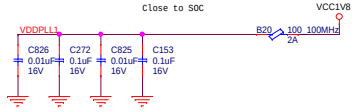


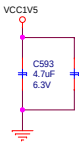


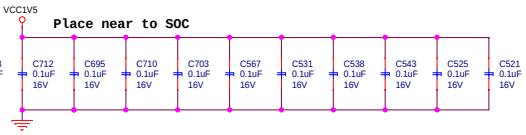


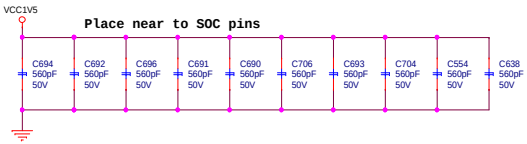


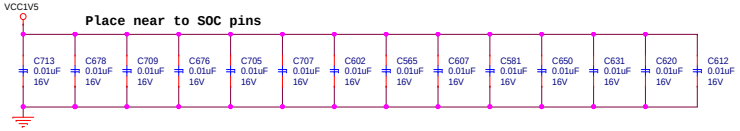












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TEXAS INSTRUMENTS ADVANTECH

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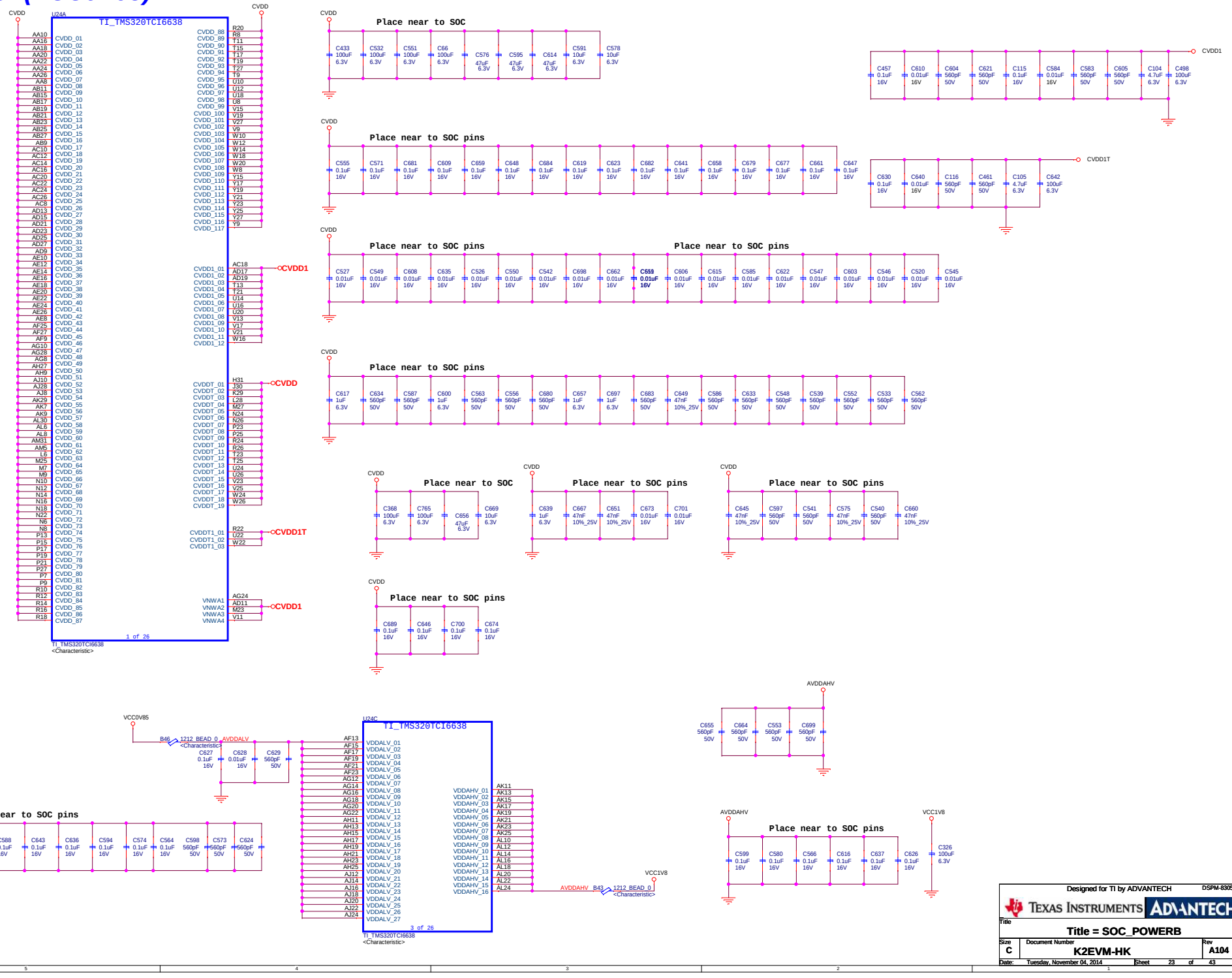
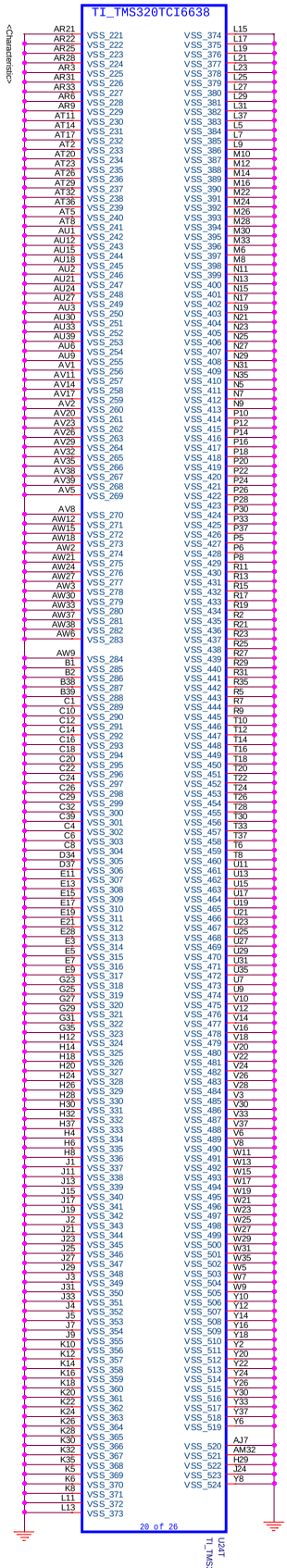
0.85V - 1.05V (CVDD) (Smart Reflex)
Fix_0.95V(VCC0V95)





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TEXAS INSTRUMENTS ADVANTECH

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DSPM-8806E

CLOCK GEN1

from AMC.0 care
30.72MHz

STATUS0 outputs the PLL_LOCK signal
STATUS1 the LOSS OF REFERENCE.

from VCTCXO19.2Mhz

From MCU connect to this signal

R227//R221=530.303

Synthesizer mode (high loop bandwidth)
CDCM6208V1:
With C1=100pF, R2=500Ω, C2=22nF and
Internal components R3=100Ω, C3=242.5pF,
fPFD=25MHz, and ICP=2.5mA:
Loop bandwidth ~ (300kHz)
CDCM6208V2:
With C1=470pF, R2=560Ω, C2=100nF and
Internal components R3=100Ω, C3=242.5pF,
fPFD=30.72MHz, and ICP=2.5mA:
Loop bandwidth ~ (300kHz)

[Note]layout would place R213and C113 close to U14.

Serial Interface Mode or Pin Mode Selection

MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

pull-up resister

122.88MHz Output
122.88MHz Output
122.88MHz Output
19.2MHz Output

SPI0 From SOC

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Title	CLOCK GEN1
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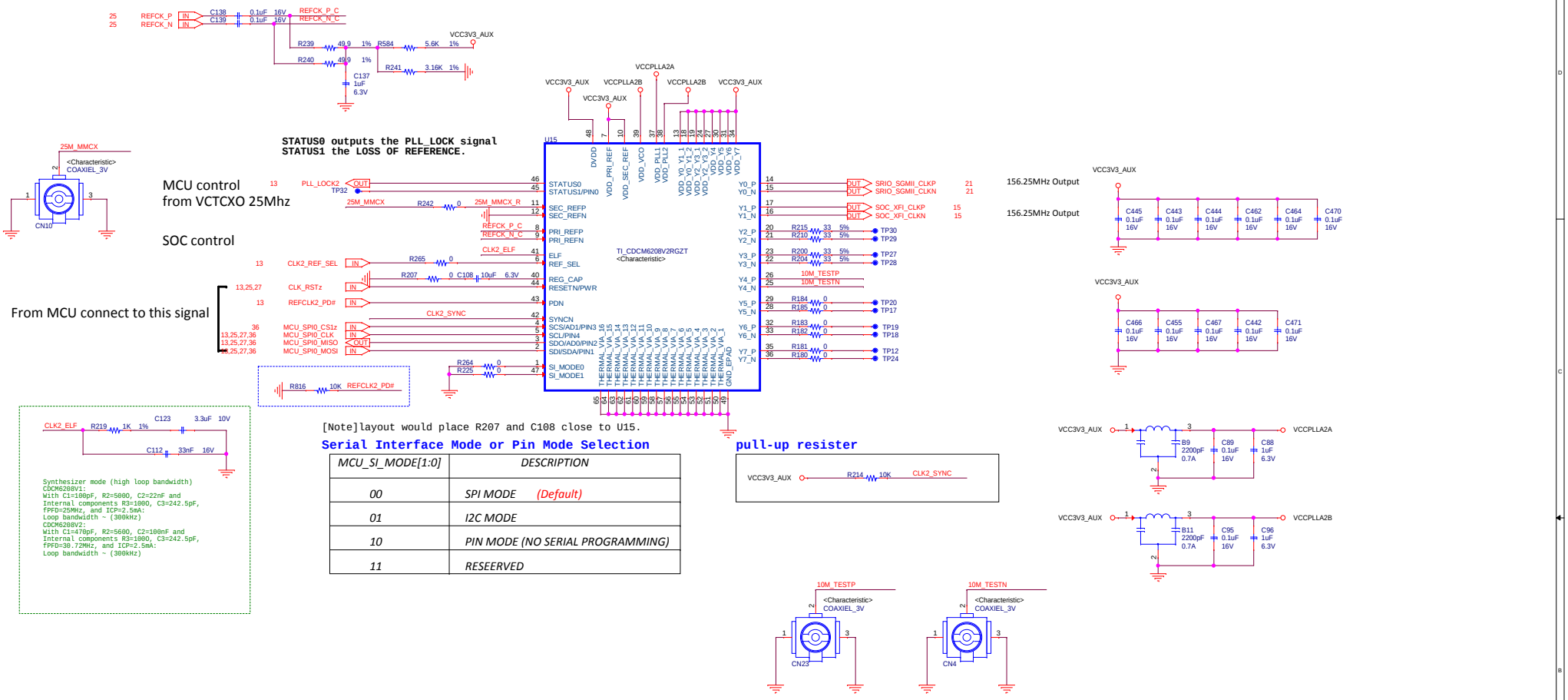
CLOCK GEN2



MCU_SI_MODE[1:0]	DESCRIPTION
00	SPI MODE (Default)
01	I2C MODE
10	PIN MODE (NO SERIAL PROGRAMMING)
11	RESEERVED

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Title: CLOCK GEN2		
Size: C	Document Number: K2EVM-HK	Rev: A104
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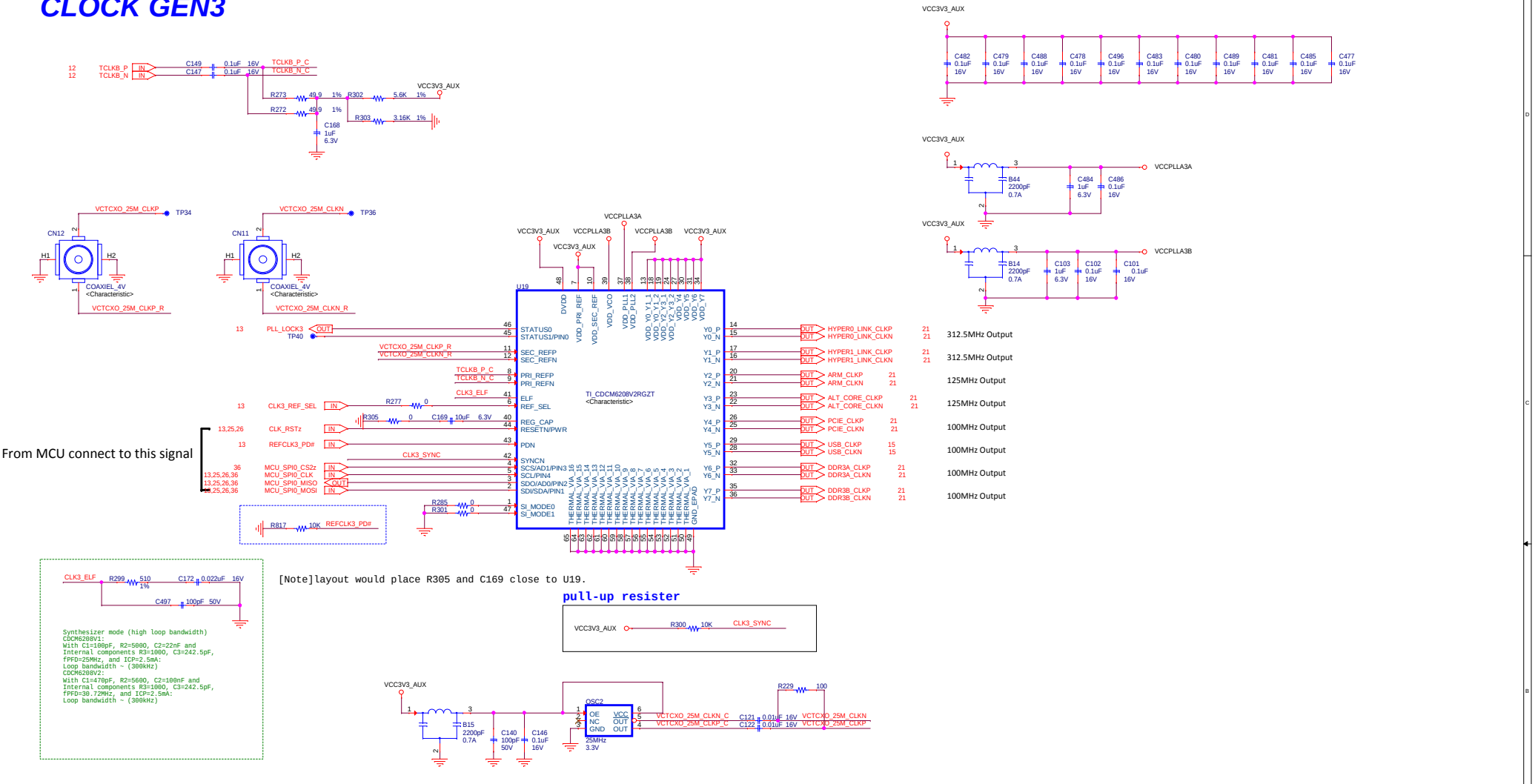
CLOCK GEN3



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Title	CLOCK GEN3
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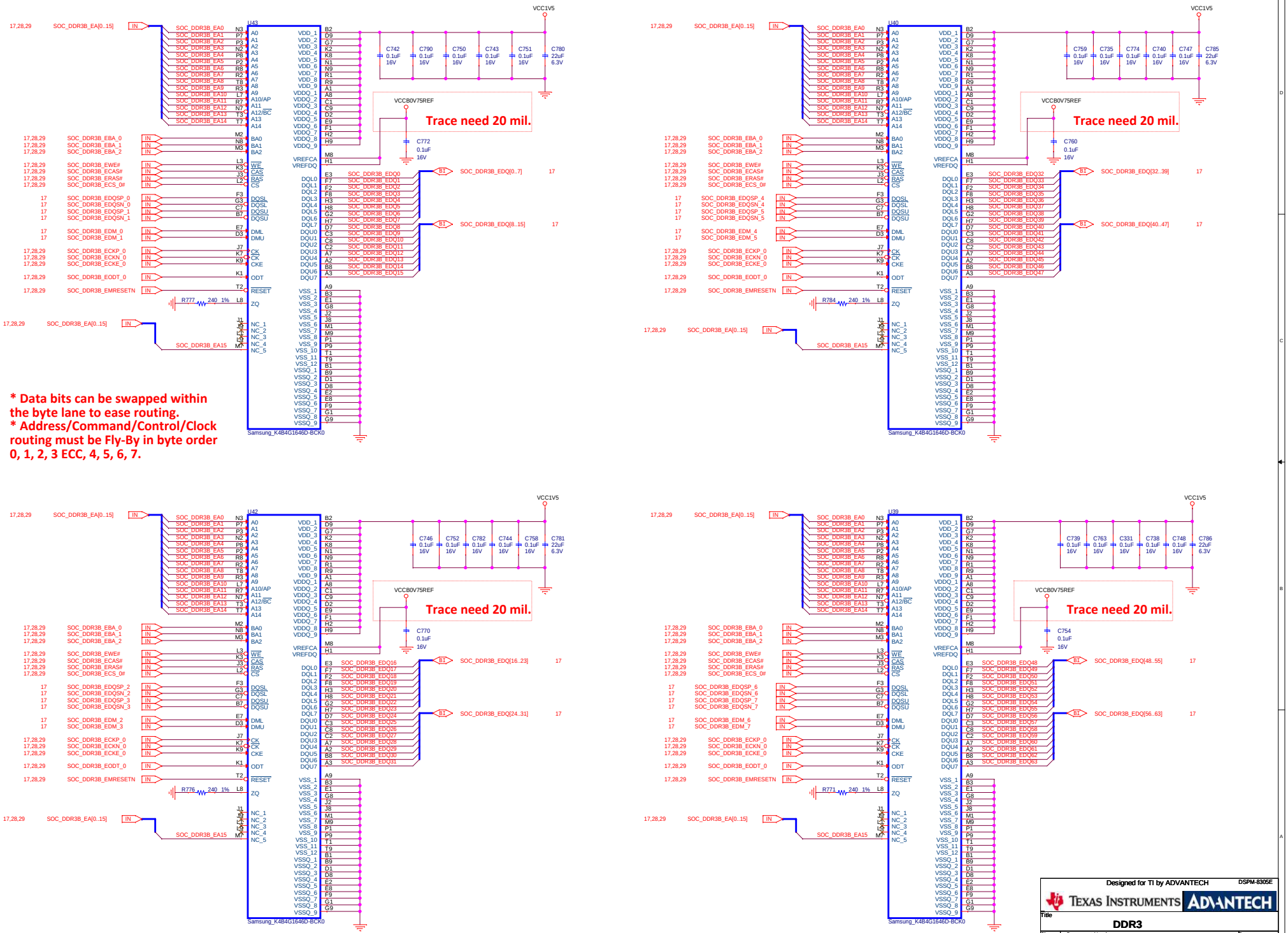

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DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title			
DDR3			
Size: C	Document Number: K2EVM-HK		Rev: A104
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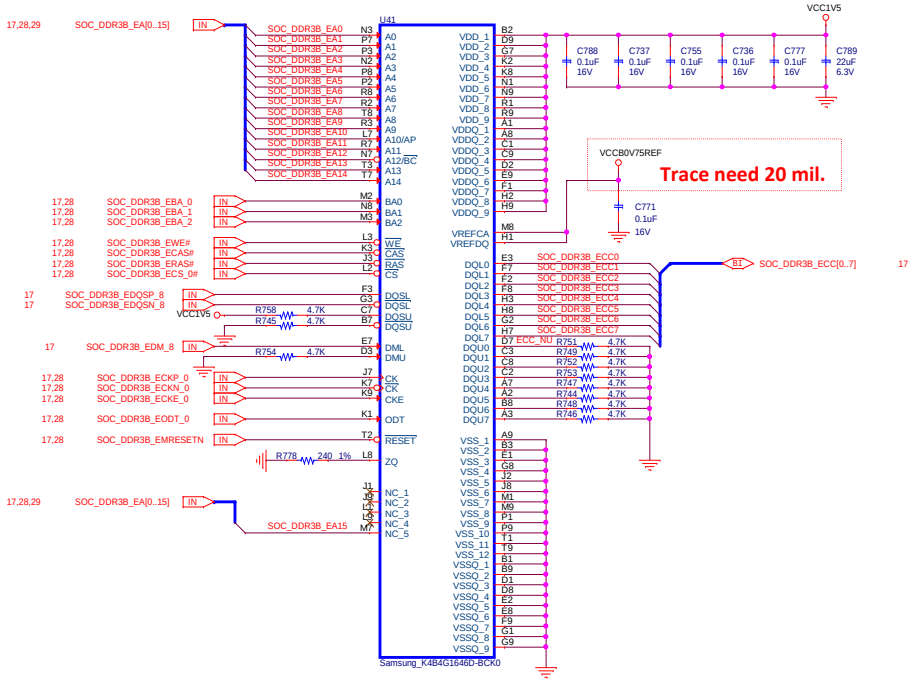
FOR ECC USE



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TEXAS INSTRUMENTS ADVANTECH

Title			
DDR3_ECC			
Size: C	Document Number: K2EVM-HK		Rev: A104
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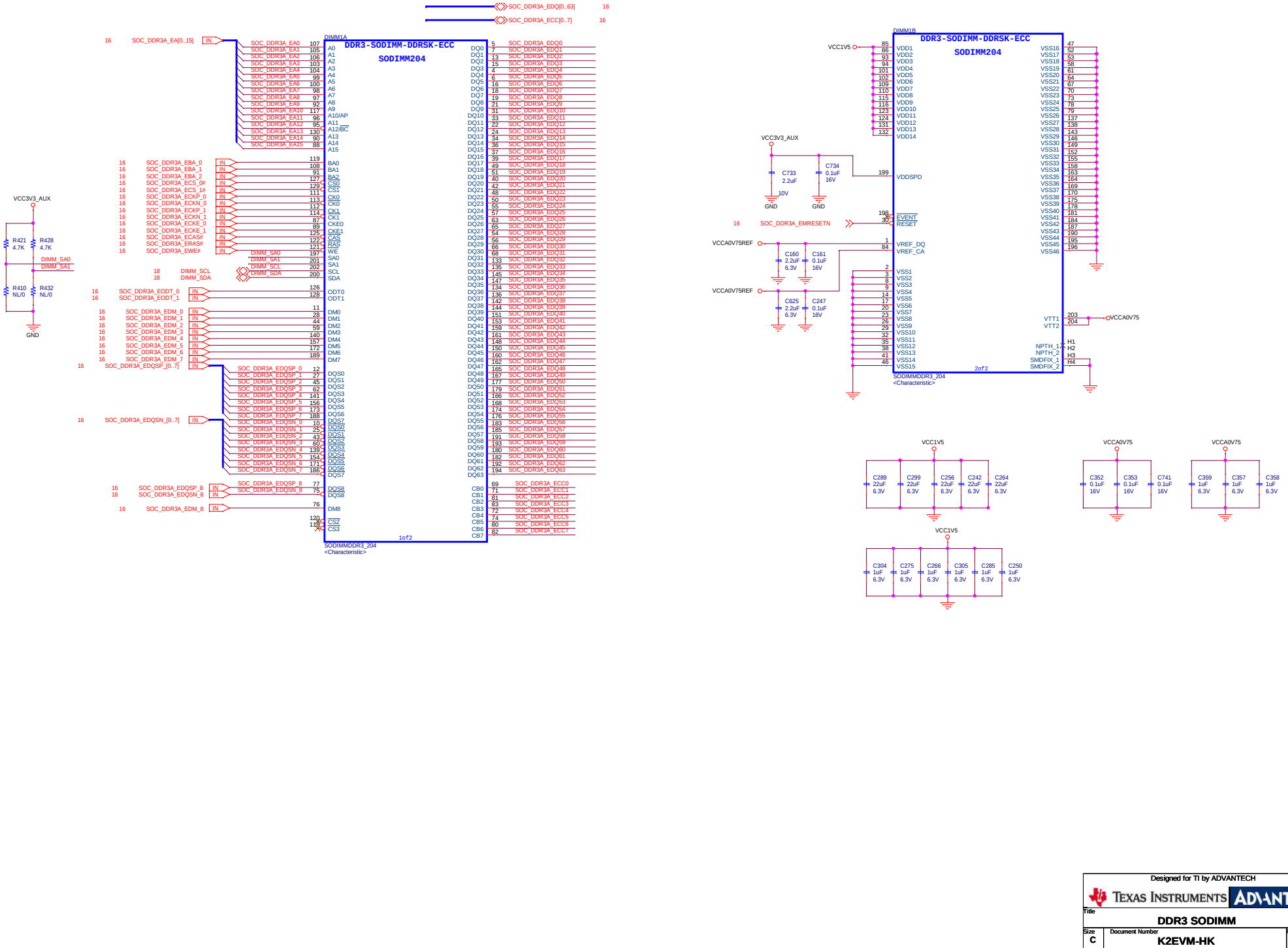

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TEXAS INSTRUMENTS ADVANTECH

Title	DDR3 SODIMM	
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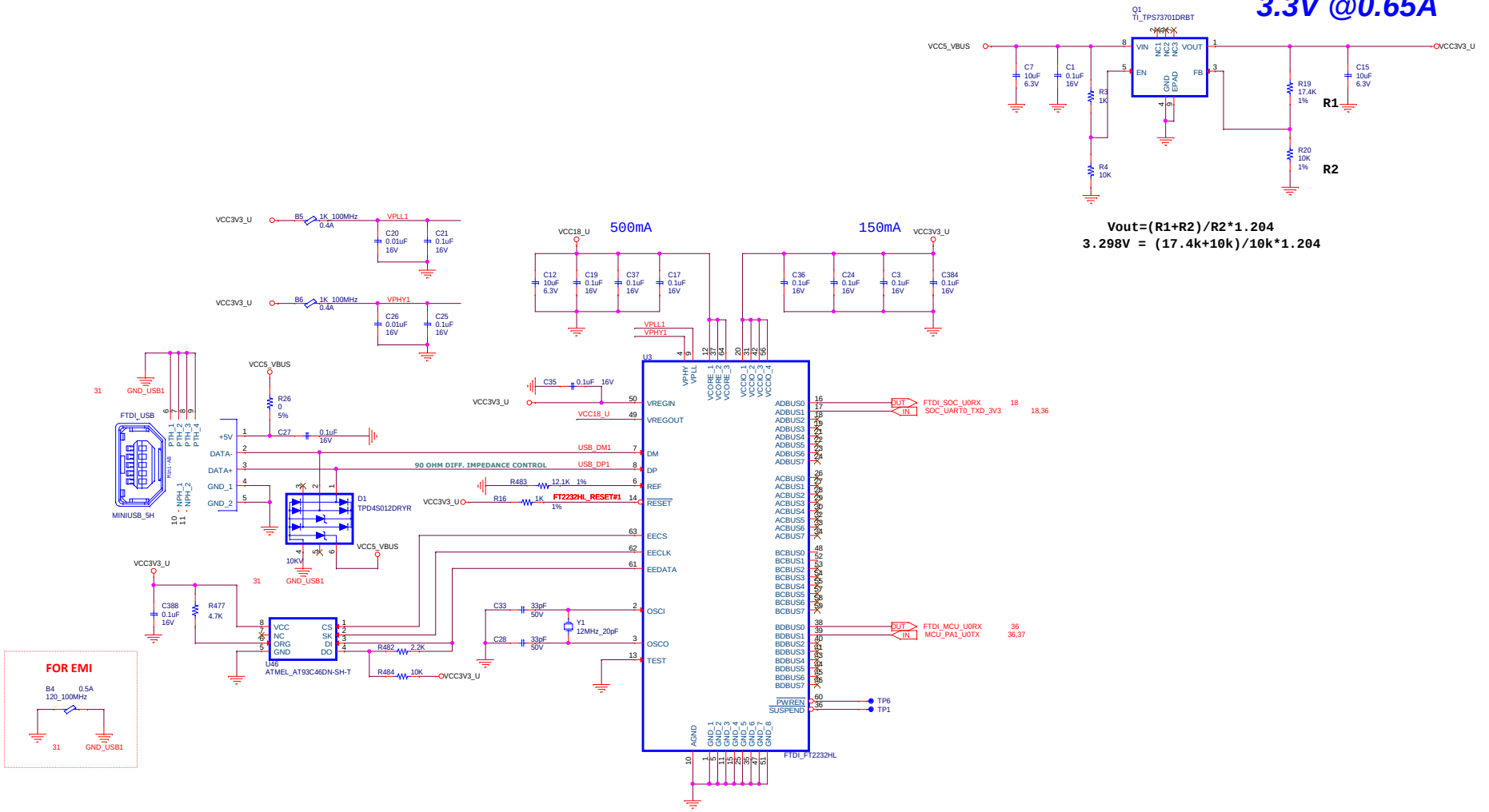
SoC UART1 TO USB



Designed for TI by ADVANTECH DSPM-8305E

Title	SoC UART1 TO USB	
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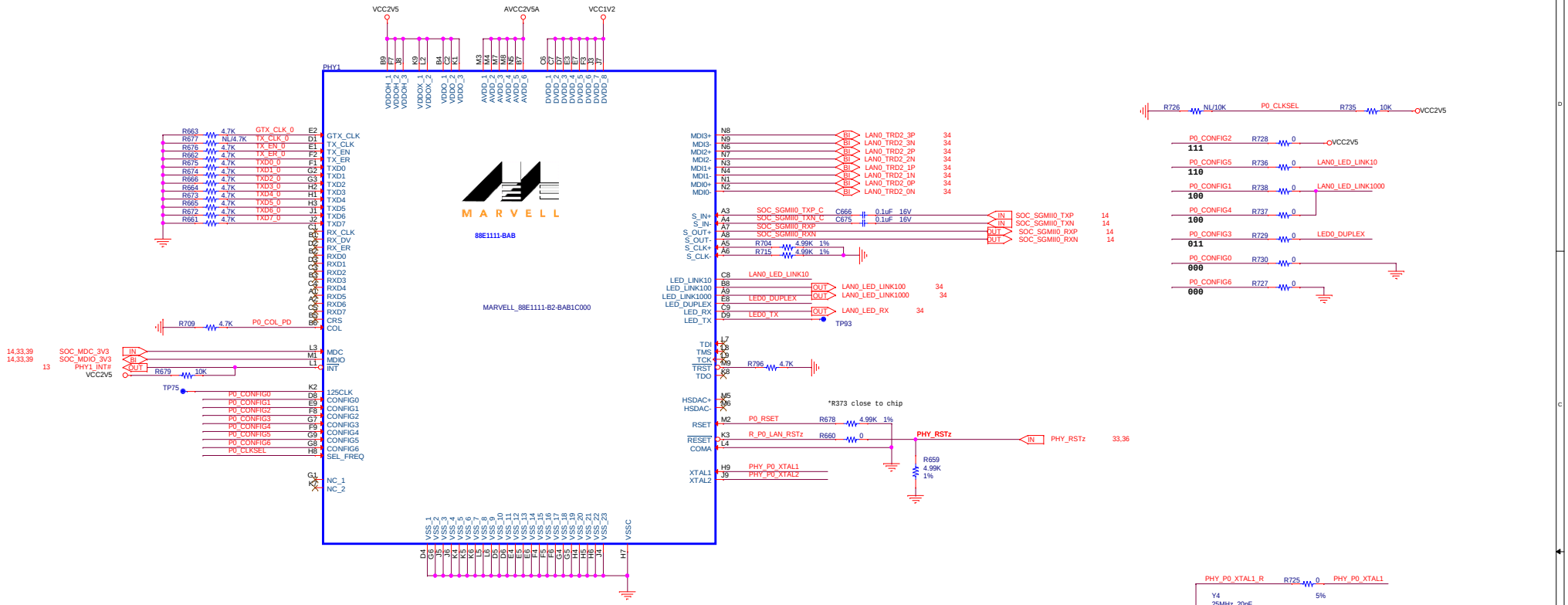

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x00

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	000	LED_TX	PHY Address bit[2:0] 000
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4			
CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

Designed for TI by ADVANTECH DSPM-8305E

Title: Gigabit Ethernet PHY1

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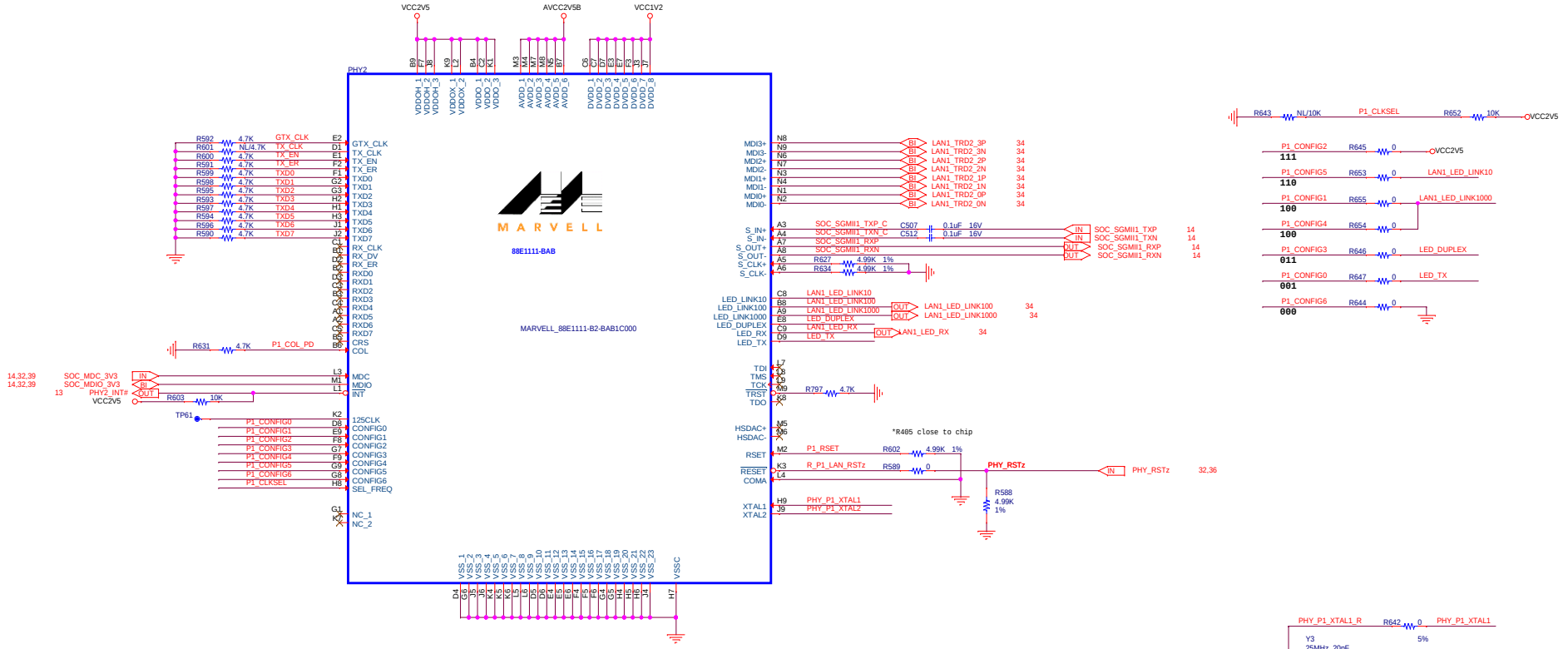

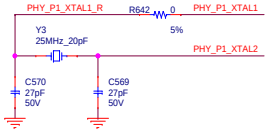

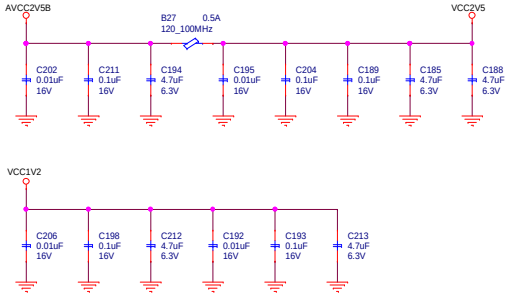

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4			
CONFIG5	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG6	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

Designed for TI by ADVANTECH DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: Gigabit Ethernet PHY2

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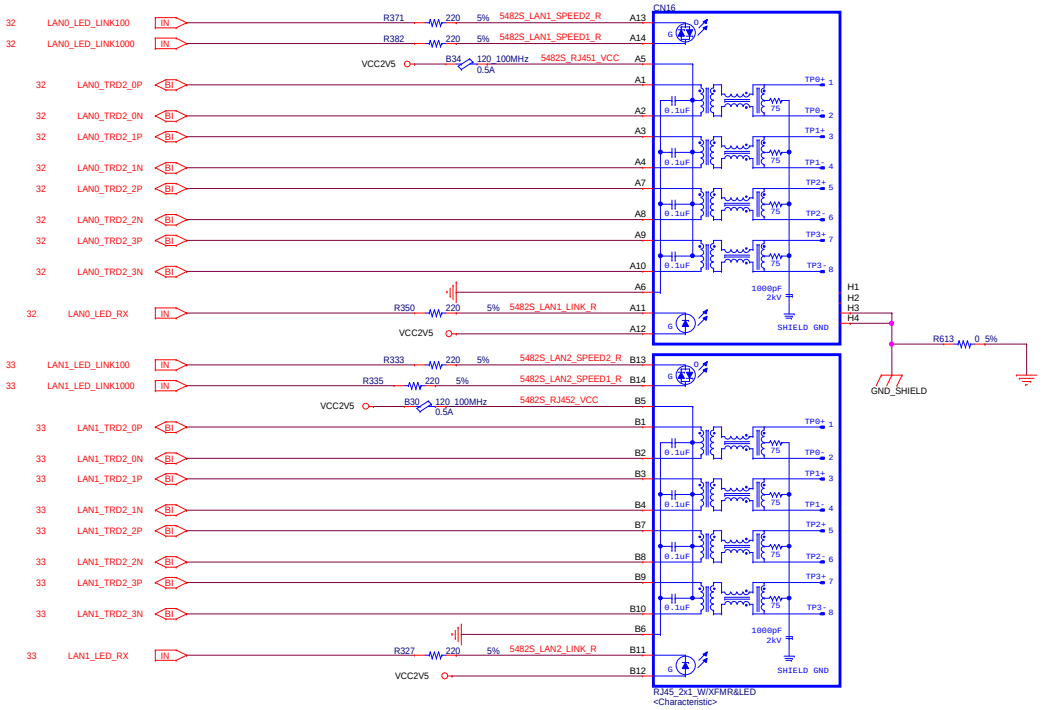
LAN-BI[88E1111 Output Port0]

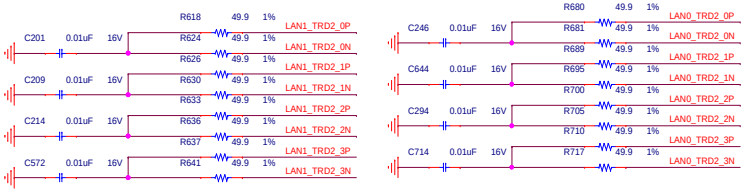
	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

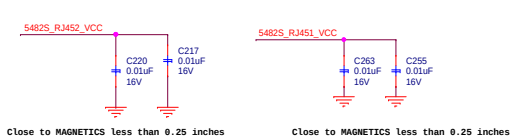
LAN-BI[88E1111 Output Port1]

	LED2 (GREEN)	LED1 (ORANGE)	LED3 (GREEN)
1G	0	1	BLINKING
100M	1	0	BLINKING
10M	0	0	BLINKING
NO LINK	1	1	0

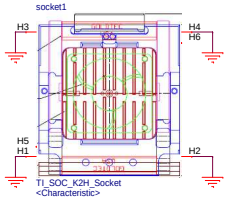
Bi-Color LED's on RJ45 controls from PHY



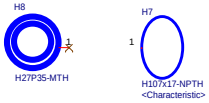




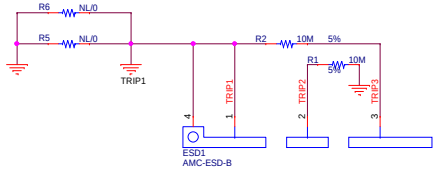
SoC Socket



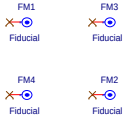
AMC Hole



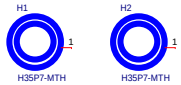
Front panel and ESD Strip



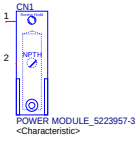
On board



XDS200 Holes



Key Zone



(Bottom Side 3mm) Placed Capacitors

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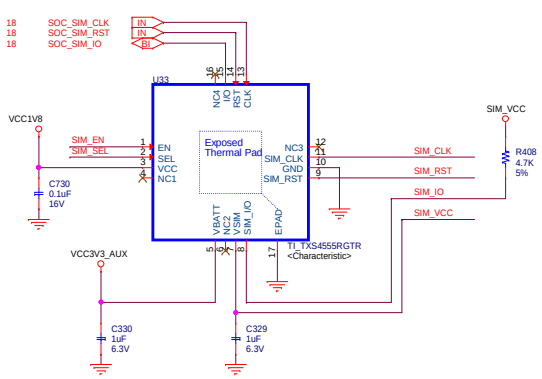
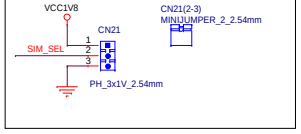
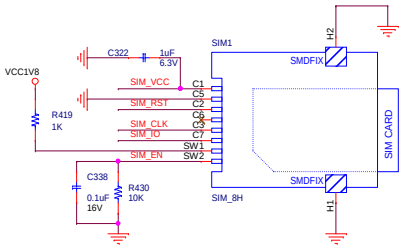
USIM

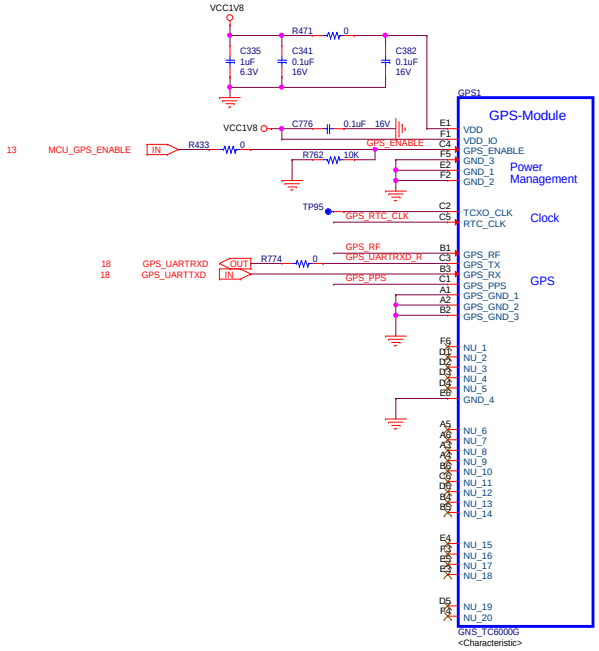


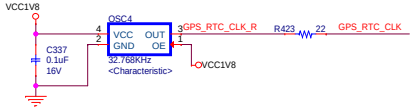
	High	Low (Default)
SIM_SEL	VCC_SIM Value = 2.95V	VCC_SIM Value = 1.8V

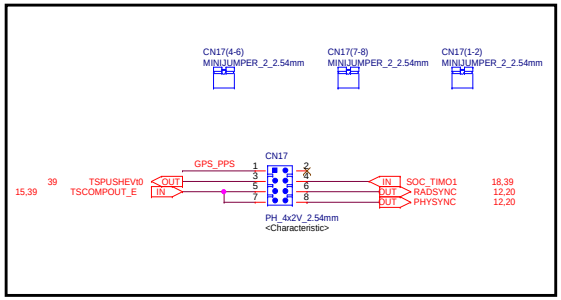




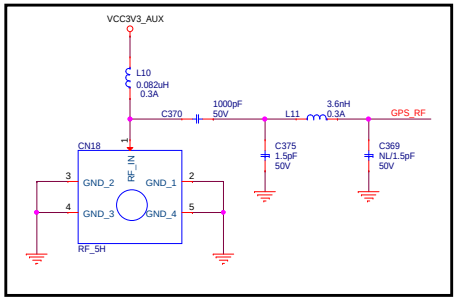
GPS







FOR ANTENNA CIRCUIT



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Title	GPS & SIM CARD	
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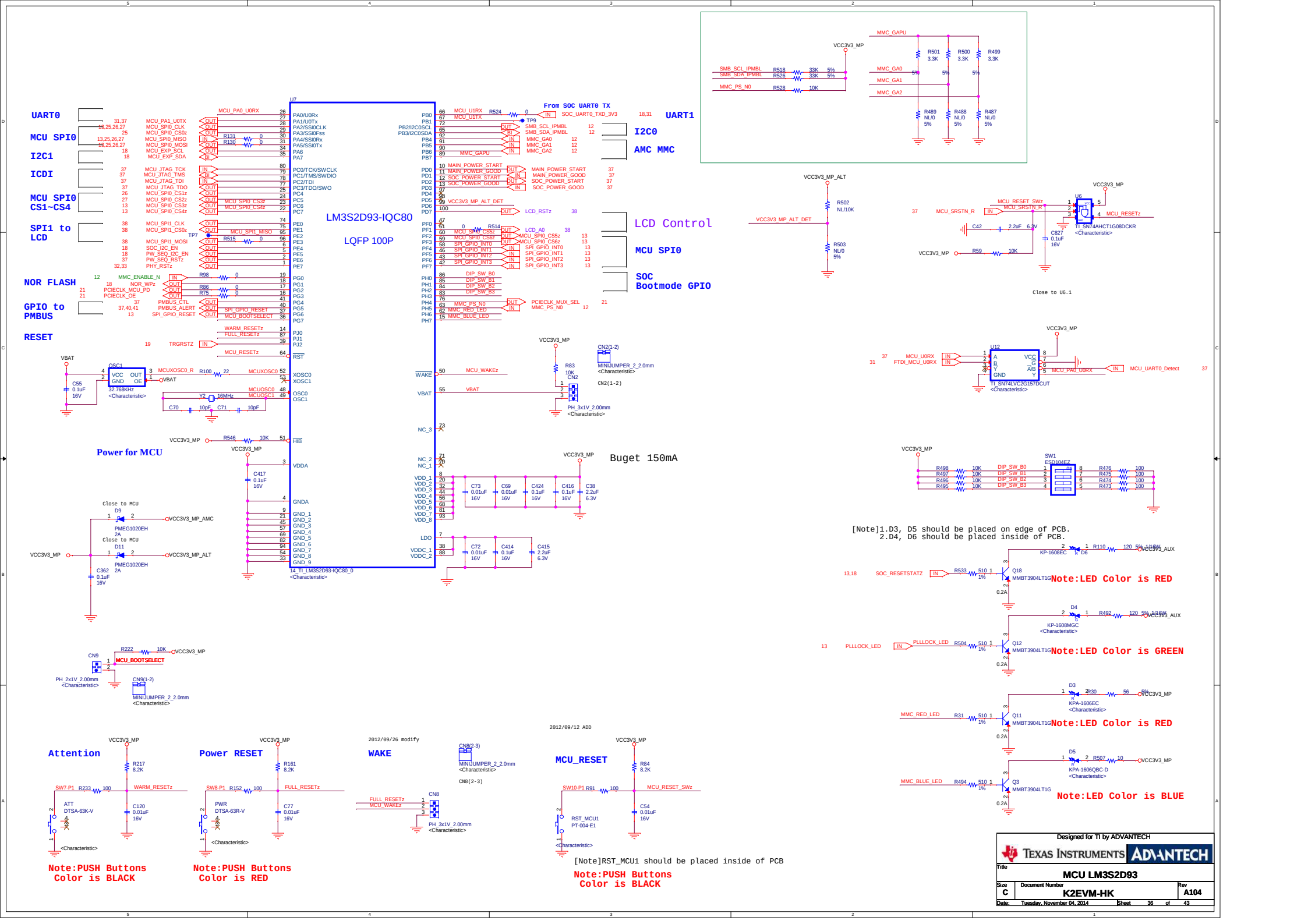
UART0
MCU SPI0
I2C1
ICDI
MCU SPI0 CS1~CS4
SPI1 to LCD
NOR FLASH
GPIO to PMBUS
RESET
LM3S2D93-IQC80
LQFP 100P
From SOC UART0 TX
UART1
I2C0
AMC MMC
LCD Control
MCU SPI0
SOC Bootmode GPIO
Power for MCU
Buget 150mA
Close to U6.1
Close to MCU
[Note]1.D3, D5 should be placed on edge of PCB.
2.D4, D6 should be placed inside of PCB.
Note:LED Color is RED
Note:LED Color is GREEN
Note:LED Color is BLUE
Attention
Power RESET
WAKE
MCU_RESET
2012/09/26 modify
2012/09/12 ADD
Note:PUSH Buttons Color is BLACK
Note:PUSH Buttons Color is RED
[Note]RST_MCU1 should be placed inside of PCB
Note:PUSH Buttons Color is BLACK
Designed for TI by ADVANTECH
TEXAS INSTRUMENTS
ADVANTECH
Title
MCU LM3S2D93
Size C
Document Number K2EVM-HK
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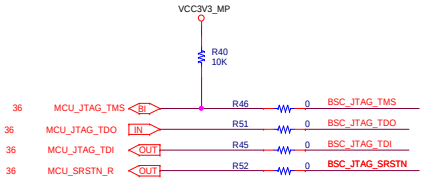
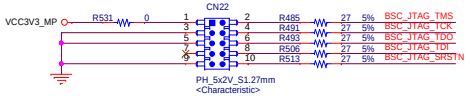
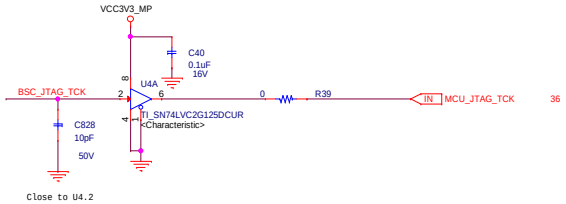
MCU JTAG

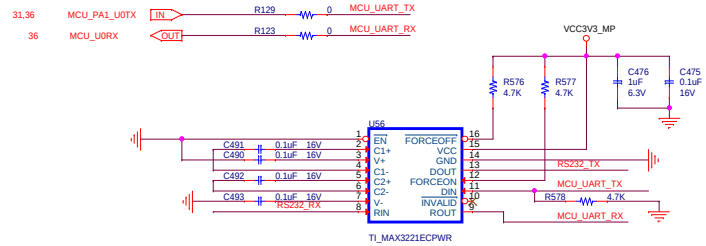


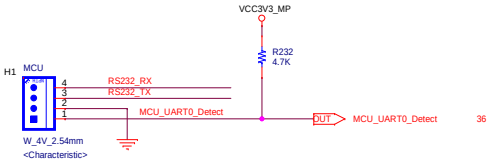


10 pos (50 mil pitch) connector

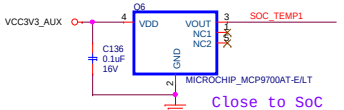


MCU UART

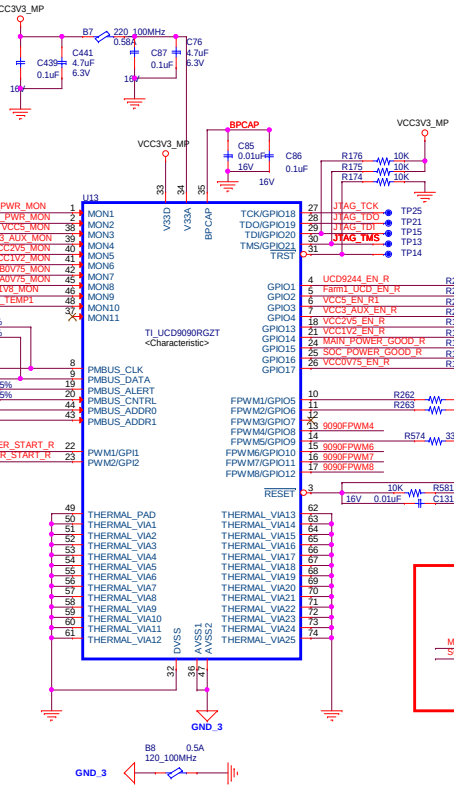




Power Sequencing



Close to SoC

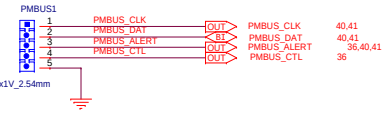


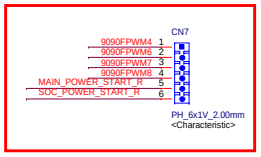
Slave I2C Address = 0x65
(Internal ADDR[7:5] = 0b110

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
SHORT	--

PMBus Head





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Title	MCU MISC	
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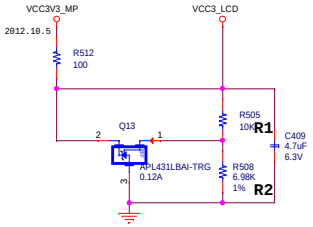
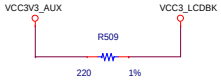
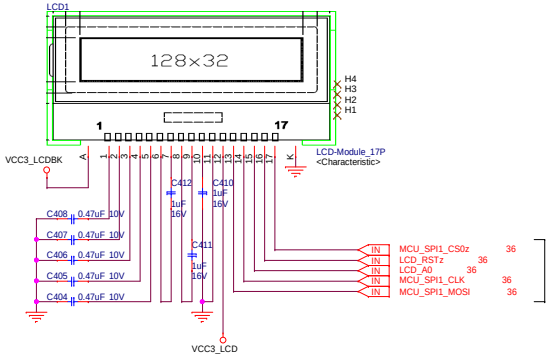


VO = 1.24v(1+R1/R2)+0.15uA*R1

3.018V =1.24 (1+10k/6.98k)+0.15u*10k



NHD-C12832A1Z-FSB-FBW-3V3



SPI1 CS0
LCD control

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Title: **MCU LCD**

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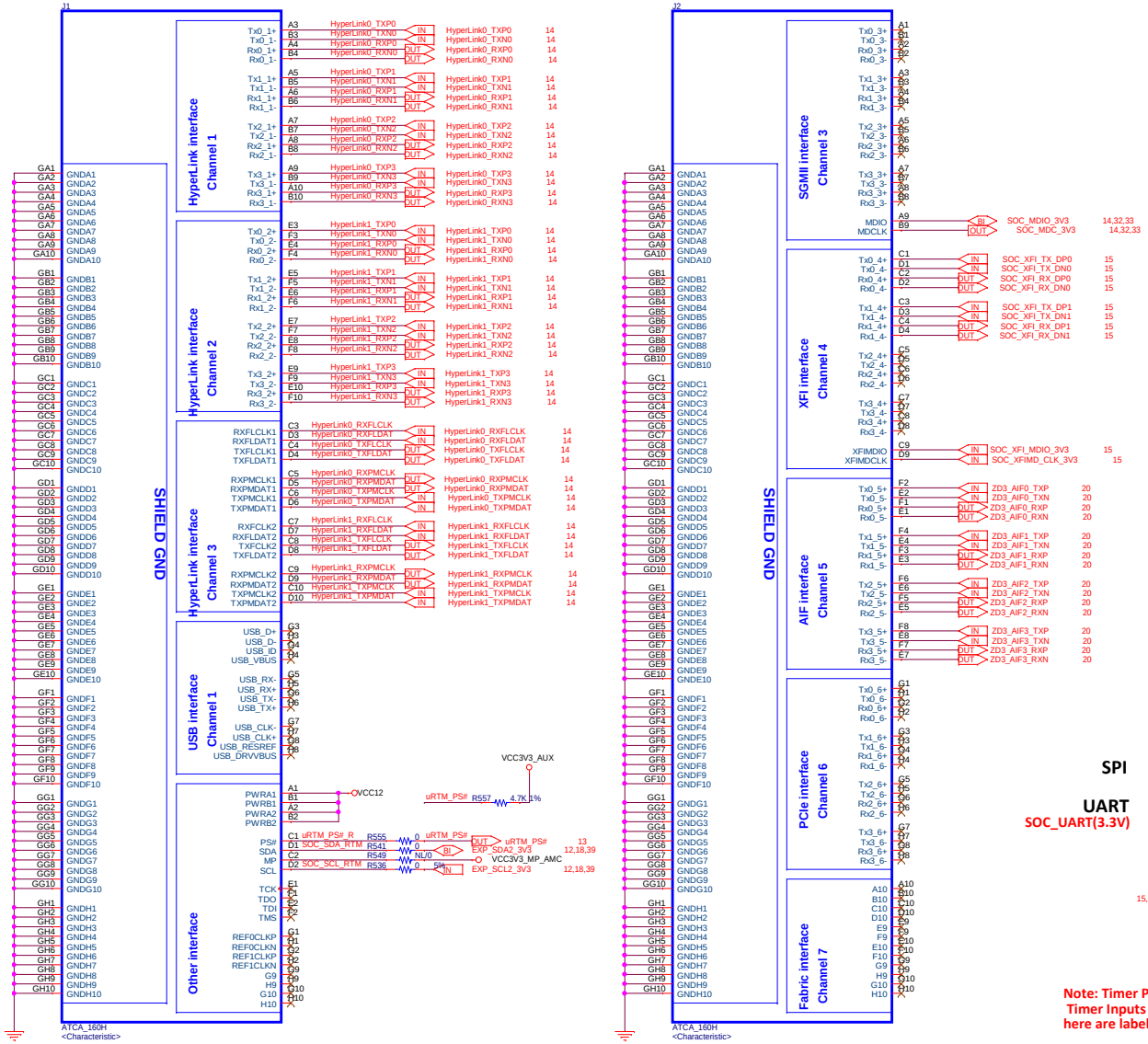
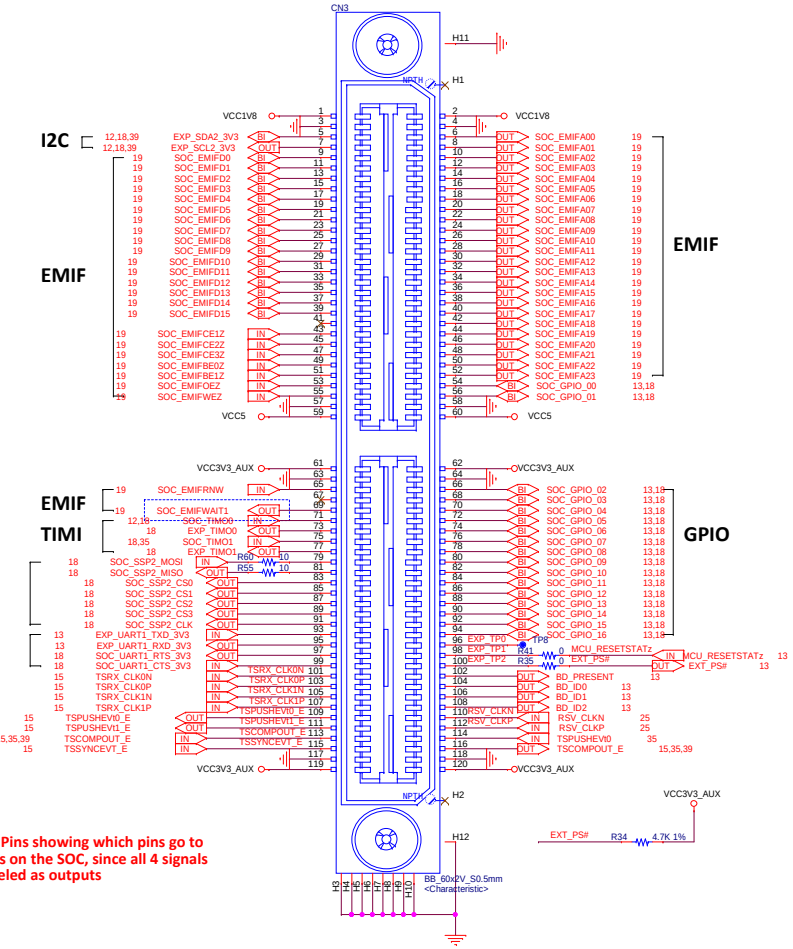
Note : J1 connector close to AMC Interface.

Note : J2 connector close to Key socket.



120-pin Expansion Header

the interfaces on the 120-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS



Note: Timer Pins showing which pins go to Timer Inputs on the SOC, since all 4 signals here are labeled as outputs

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TEXAS INSTRUMENTS ADVANTECH

Title: mTCA_ZD3/120-pin Expansion

Size	Document Number	Rev
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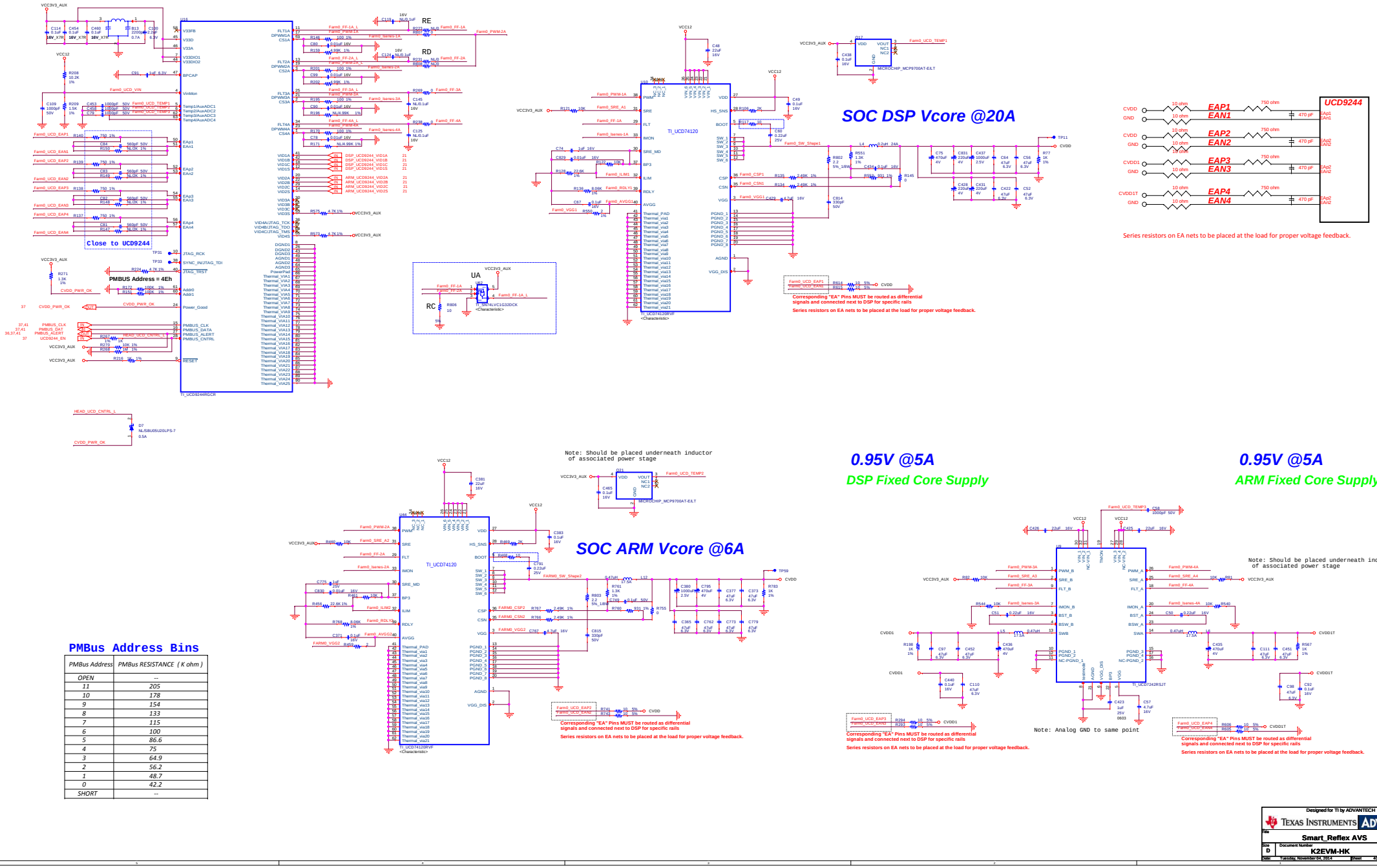

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

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TEXAS INSTRUMENTS ADVANTECH

Title: Smart_Reflex AVS

Size	Document Number	Rev
D	K2EVM-HK	A104

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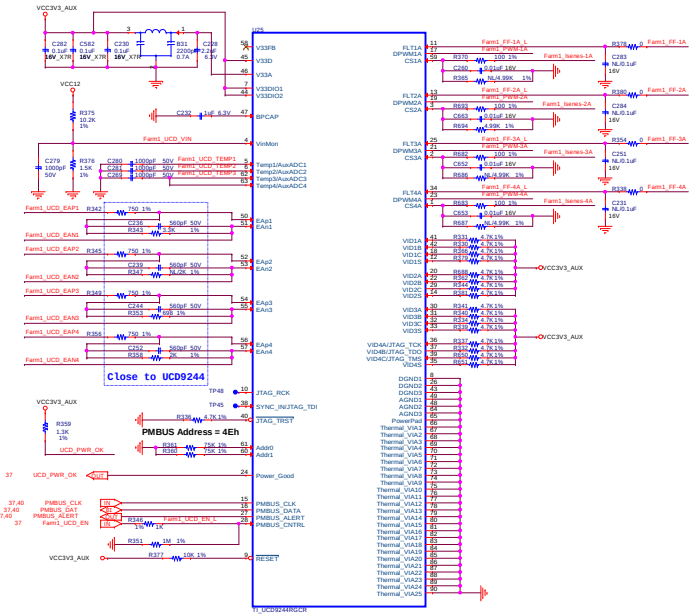
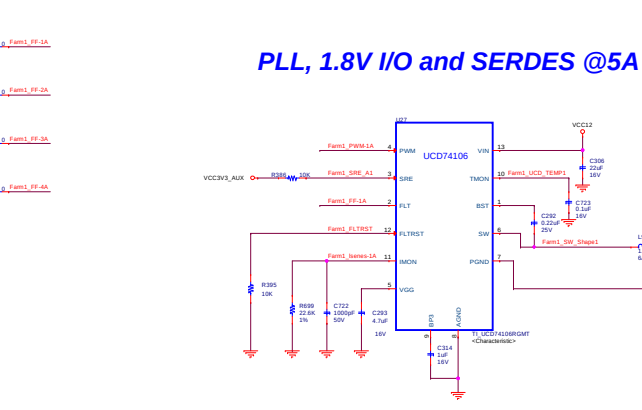
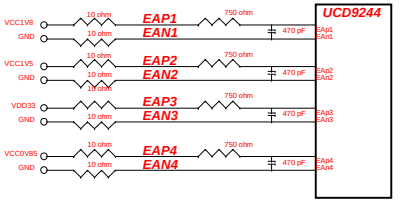




PLL, 1.8V I/O and SERDES @5A

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

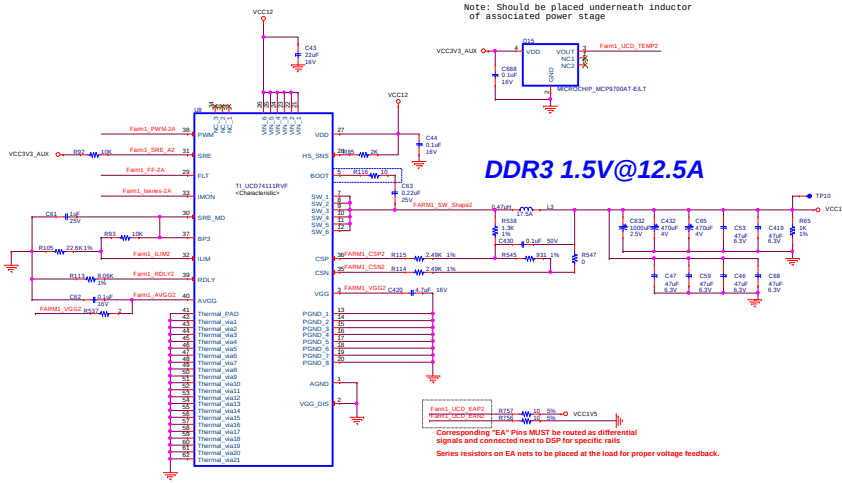
Series resistors on EA nets to be placed at the load for proper voltage feedback.



Series resistors on EA nets to be placed at the load for proper voltage feedback.

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--



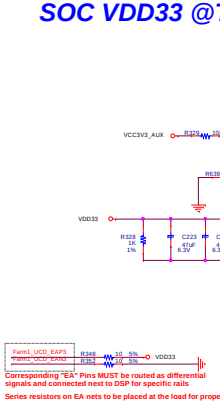
Note: Should be placed underneath inductor of associated power stage

DDR3 1.5V@12.5A

Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

SOC VDD33 @TBD

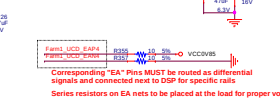


Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Note: Analog GND to same point

SOC USB and SERDES 0.85V @TBD



Corresponding "EA" Pins MUST be routed as differential signals and connected next to DSP for specific rails

Series resistors on EA nets to be placed at the load for proper voltage feedback.

Designed for TI by ADVANTECH

DSPM-8305E

TEXAS INSTRUMENTS ADVANTECH

Title: Smart_Reflex VDD33/1.8V/1.5V/0.85V

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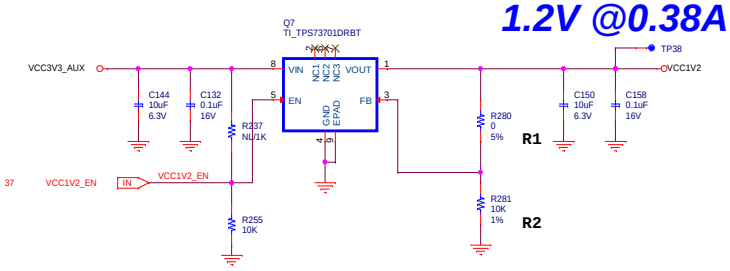
VCC1V2

1.2V @0.38A

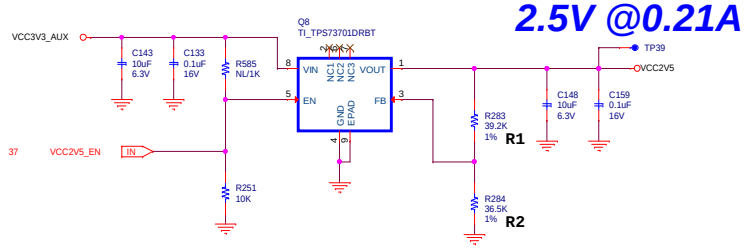


Vout=(R1+R2)/R2*1.204

1.204V = (0+10k)/10k*1.204

VCC2V5

2.5V @0.21A

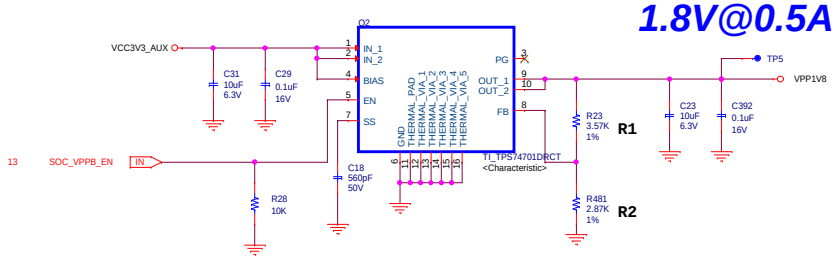


Vout=(R1+R2)/R2*1.204

2.50V =(39.2k+36.5k)/36.5k*1.204

VPP1V8

1.8V@0.5A

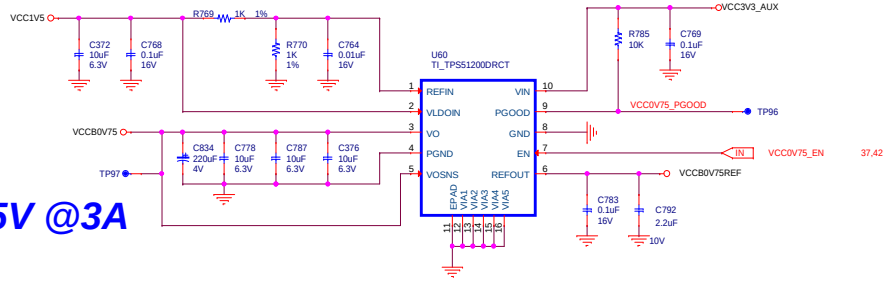


Vout=0.8*(1+R1/R2)

1.79512V =0.8*(1+3.57k/2.87k)

VCCB0V75

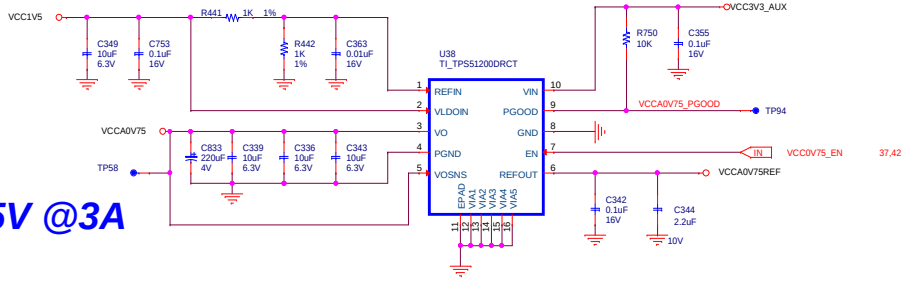
DDR3-1600
DiscreteSDRAM ArrayI



0.75V @3A

VCCA0V75

For DDR3-1600 SO-DIMM



0.75V @3A

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TEXAS INSTRUMENTS ADVANTECH

Title	Power_1.2V/2.5V/0.75V/1.8V	
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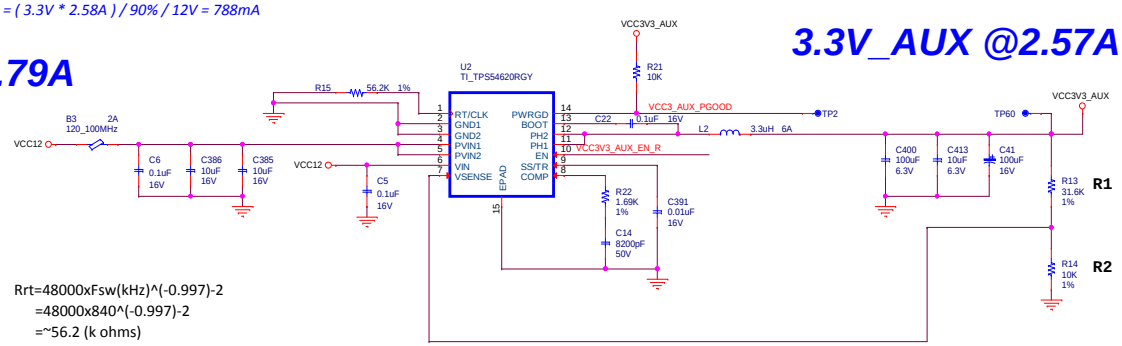
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.57A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x840^(-0.997)-2
=~56.2 (k ohms)

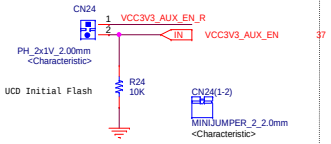
Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*3/(840kHz*0.0825)
Cout=~87uF

Reference Capacitor=100uF

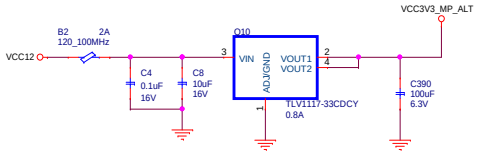
(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3A * 0.3) * (3.3 / (12 * 840kHz))
L = 9.67 * 0.33u
L = ~3.2 uH

Reference Inductor 3.3uH



VCC3V3_MP_ALT

3.3V_MP@150mA



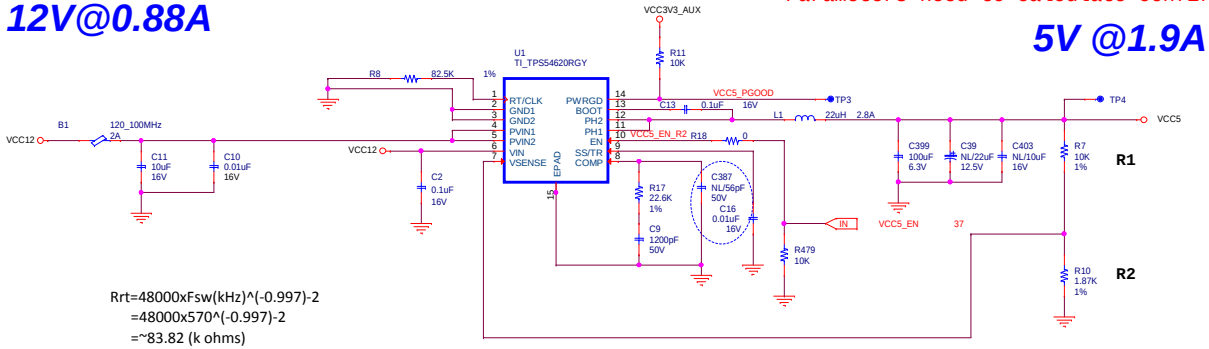
VCC5

Assume 90% Pe,
*Iin = (5V * 1.9A) / 90% / 12V = 880mA*

12V@0.88A

*Parameters need to calculate confirm

5V @1.9A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x570^(-0.997)-2
=~83.82 (k ohms)

Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2/(570kHz*0.125)
Cout=~56.14uF

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 5)/(2.3A * 0.3) * (5 / (12 * 570kHz))
L = 10 * 0.73u
L = ~7.3 uH

Reference Inductor 22uH

Designed for TI by ADVANTECH DSPM-8305E

Title: Power_VCC5 / VCC3V3_AUX/MP_ALT

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