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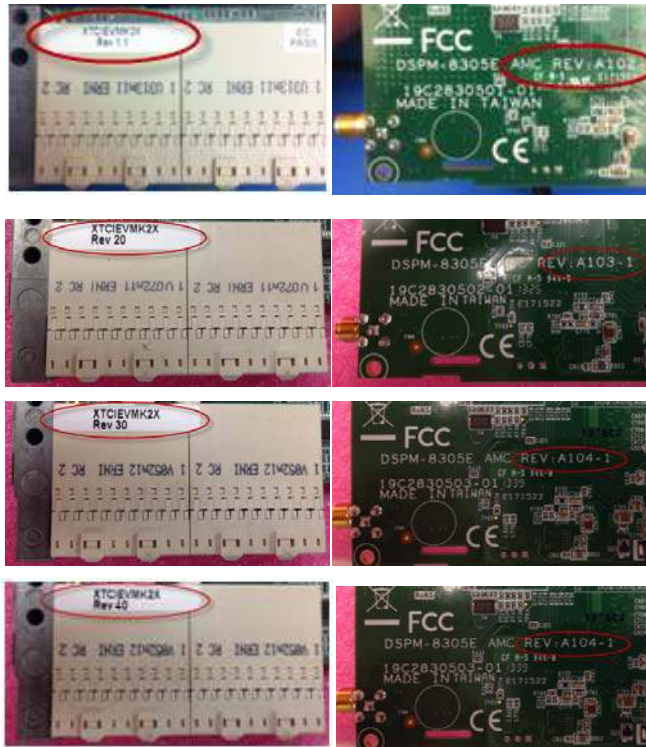
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1. Software and Firmware Version List

EVM Revisions could be identified by sticker on RTM Connector, and the PCB Revision is located on bottom of board near GPS Antenna Input



The initial firmware versions on Rev 1.1 EVMs are shown as below:

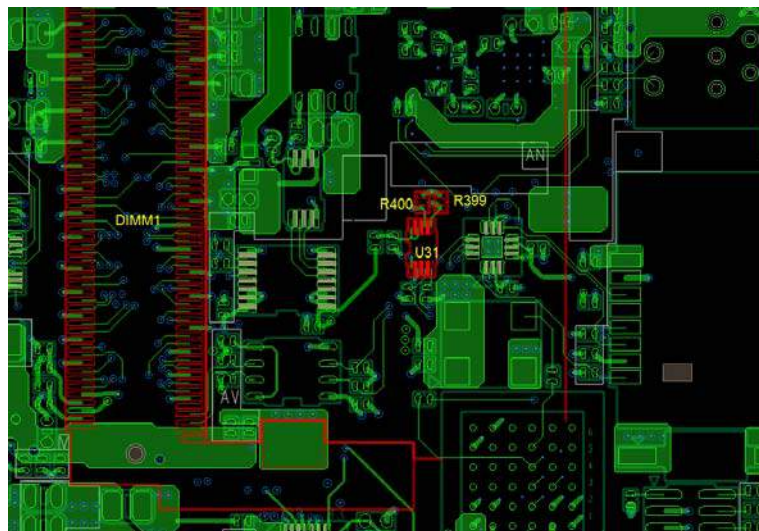
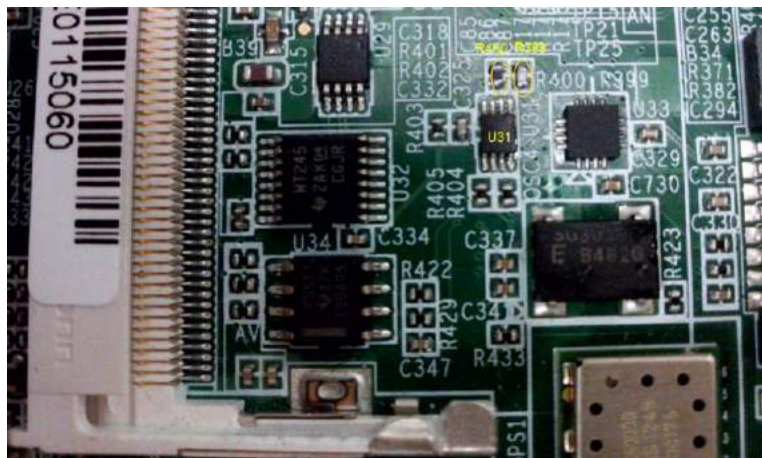
EVM Revision	SN Range	Ship Date	Silicon Rev	PCB Rev	BMC	LINUX-MCSDK	BIOS-MCSDK
				DSPM8305E	Rev	(NAND)	(NOR)
Rev1.0	ESE0075202 – 075236	13-Feb	PG1.0	A102	1.0.1.3a	N/A	Alpha7
Rev1.1	EPD0082118 – 0082227	22-May	PG1.0	A102	1.0.2.5	N/A	Alpha7
Rev2.0	EPD0085682-0090157	3Q 2013	PG1.1	A103	1.0.2.5	N/A	Alpha7
Rev3.0	EPD0091197-0093719	1Q 2014	PG1.1	A104	1.0.2.6	N/A	3_00_03_15
Rev4.0	TBD	4Q 2014	PG2.0	A104	1.0.2.6	N/A	3_00_03_15

Updated firmware/software could be available on Advantech website or TI MCSDK website.

2. EVMK2HX Rev 1.1 Known Issues

2.1 EMAC Link Down Issue

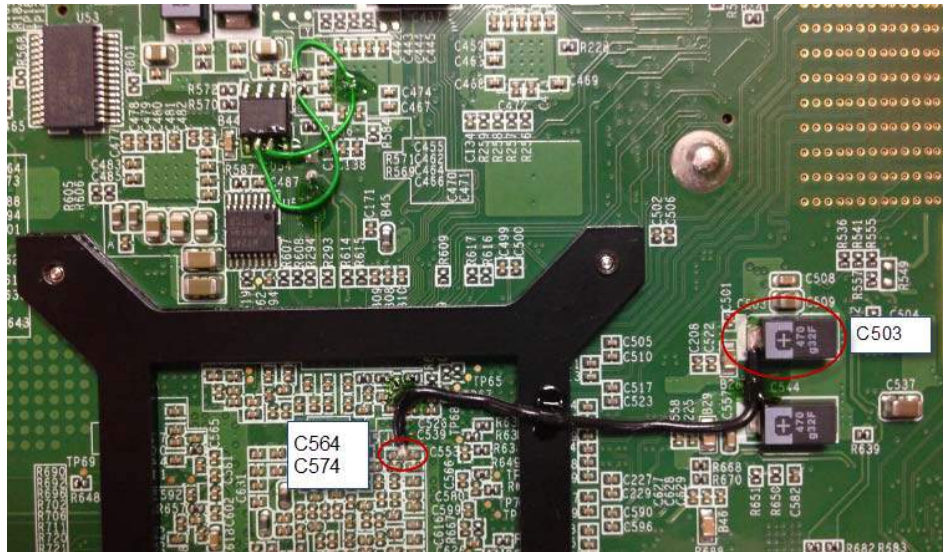
- Description: Noise on MDCLK signal impacts stability of the MDIO link. When Linux kernel sees MDIO link go down it tears down data link as well. Have not seen an issue with using MDIO link to configure external PHY.
- Workaround: Different options under investigation.
 1. Modify code not to depend upon MDIO link remaining active for EMAC communication
 2. Add stronger pull-up resistors on MDCLK and MDIO signal, by replacing R399/R400 from 4.7 kohm with 220 ohm resistors (0402 sized)



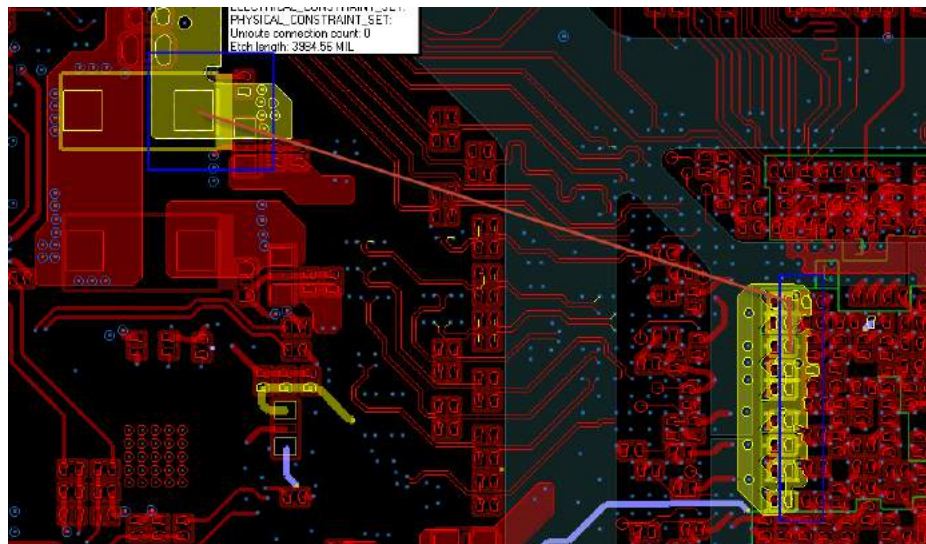
- Plans for a fix: Will clean up routing of MDCLK signal on Rev2.0. BOM will also be changed on future builds to incorporate 220ohm resistor pull-up changes.

2.2 VCC0V85 Voltage Drop Issue

- **Description:** The trace width of the VCC085 signal is too narrow and causes a voltage drop at the pin of the SOC. Since this supply is used for SerDes interfaces it could cause SerDes interfaces to lose link. This issue has only been identified and observed on the SGMII.
- **Workaround:** A couple different options are still under investigation for their effectiveness.
 1. Add external wire to provided adequate patch for expected current from pin 1 of “C503” (net VCC0V85) to pin 1 of “C564, C574” (net VDD0V85). (Wire length = 5 cm)



Note: That the rework should not link to GND and cause short circuit.

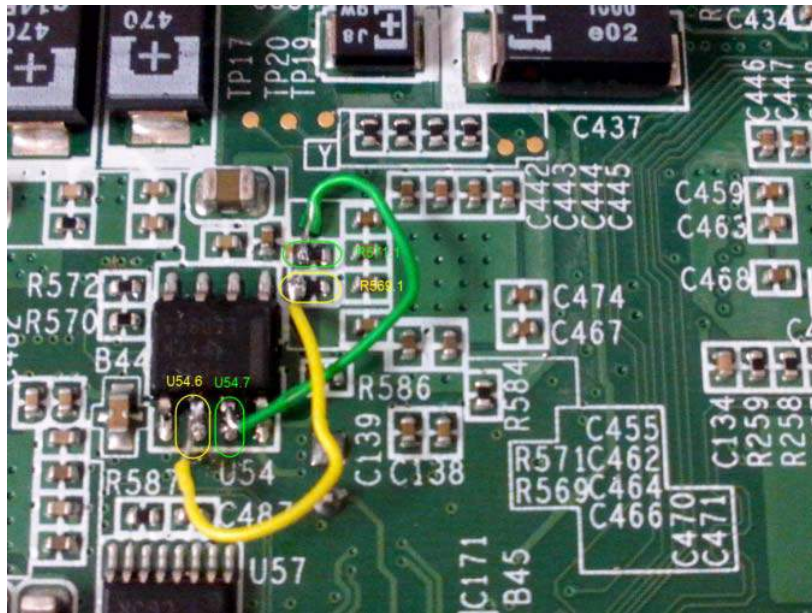


- Plans for a fix: The trace width will be fixed on Rev2.0. The filter element on AVDDALV requires an increased current capacity (suggest up to 4A) to allow for margin on worse-case power as per latest Snowbush power estimates when all SERDES are active. Increase of current capacity on filtering elements for AVDDAHV also recommended (suggest up to 3A). Please see latest estimates below. CVDD power budgeted already on the DSP AVS supply. Both of these nets shall be implemented as copper pours up to the filters and as a plane afterwards to minimize resistance and inductance and maximize plane capacitance.

	AVDDAS (0.85V)	AVDDHVS (1.8V)	CVDD (AVS)	Unit
Total per Kepler	2.951016043	1.274949495	0.005754011	A

2.3 I2C SDA/SCL Reserve Issue

- Description: SCL and SDA are swapped on U54 bus repeater. Impacts I2C going to 120p Expansion Connector and Zone 3 RTM connector.
- Workaround: Cut the jumper wire (30AWG) to swapped signal of EXP_SDA2_3V3 and EXP_SCL_3V3. Two wire each to similar yellow and green to link from U54.6 to R569.1 and U54.7 to R571.1 .



- Plans for a fix: This will be corrected on Rev2.0.

2.4 Incorrect UCD Setting

- **Description:** An invalid ‘over current’ setting in one of the UCD power management devices can cause the EVM to shut down when the SOC is heavily loaded.
- **Workaround:** Follow instructions on MCSDK wiki to perform a field update to get your UCD settings to the proper value.
(http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update)
- **Plans for fix:** The correct configuration will be programmed in future builds of EVMs.

2.5 SOC Power Fail

- **Description:** During power on of the board the UCD controller will detect a fault and will abort the power on sequence
- **Workaround:**
 1. Occasionally a successful “power on” will occur if multiple power cycles are performed.
 2. A script is in development to enable a field update to correct the UCD settings.
(http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update)
- **Plans for a fix:** Correct configuration will be programmed in future builds of EVMs

2.6 USB3.0 Performance

- **Description:** Lack of AC coupling and in-signal shunts for ESD protection can impact functionality by causing the link to intermittently go down or never come up.
- **Workaround:**
 1. Remove choke B26 , and add AC capacitors C839, C840 (0.1uf)
 2. Connect the EN pin of the USB power switch (U59) to USBDRVVBUS pin of SoC (U24) through R809 (10ohm). (USBDRVVBUS pin on U59 is used by the USB state-machine to control the VBUS supplied to the Type A connector)
- **Plans for a fix:** Expected to be fixed in future builds of EVMs

3. EVMK2HX Rev 1.1 Hardware Modifications

Rev 1.1 EVM keeps the schematics and PCB layout same as Rev 1.0 EVM, but following BOM change and reworks are made in Rev 1.1 EVMs for better stability.

3.1 EMAC Link Down Issue

- Workaround: R399 and R400 are changed from 4.7 kohm to 220 ohm resistors (0402 sized) in Rev 1.1 EVM.

3.2 VCC0V85 Voltage Drop Issue

- Workaround: An external wire is added to provided adequate patch for expected current from pin 1 of “C503” (net VCC0V85) to pin 1 “C564, C574” (net VDD0V85). (Wire length = 5 cm). Also, the wire is glued on heat sink back plate for stability.

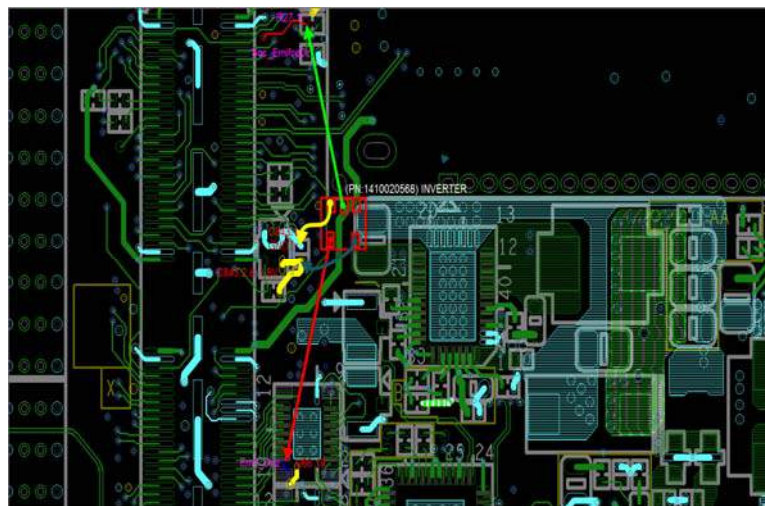
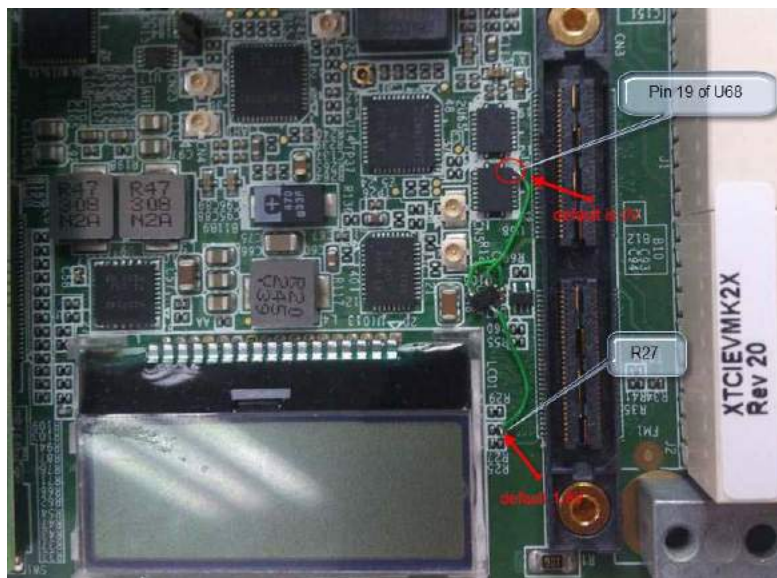
3.3 I2C SDA/SCL Reserve Issue

- Workaround: External rework wires (30AWG) are added to swapped signal of EXP_SDA2_3V3 and EXP_SCL2_3V3.

4. EVMK2HX Rev 2.0 Known Issues

4.1 EMIF and NAND Test cannot be Synchronized

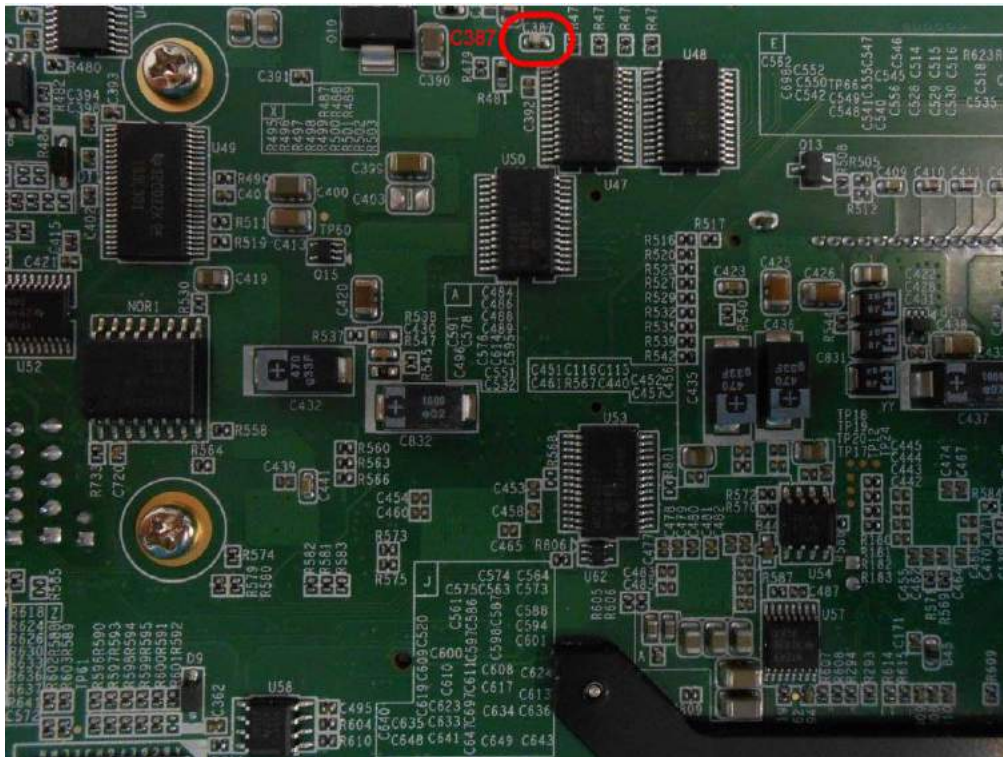
- Description: SoC could not access NAND flash through EMIF interface, and there will be one cause data transmission errors.
- Workaround:
 1. Add inverter (SN74LVC1G04DVR).
 2. Add wire (30AWG) from inverter PIN 3 to C843.1 (GND),
 3. Add wire (30AWG) from inverter PIN 5 to C843.2 (VCC1V8)
 4. Add wire (30AWG) from inverter PIN 2 to R27.1 (SOC_EMIFCE0Z)
 5. Add wire (30AWG) from inverter PIN 4 to U66.19 (EMIF_OEz).



- Plans for a fix: The rework is installed on all Rev 2.0 board before shipping.

4.2 USB Device Not Work

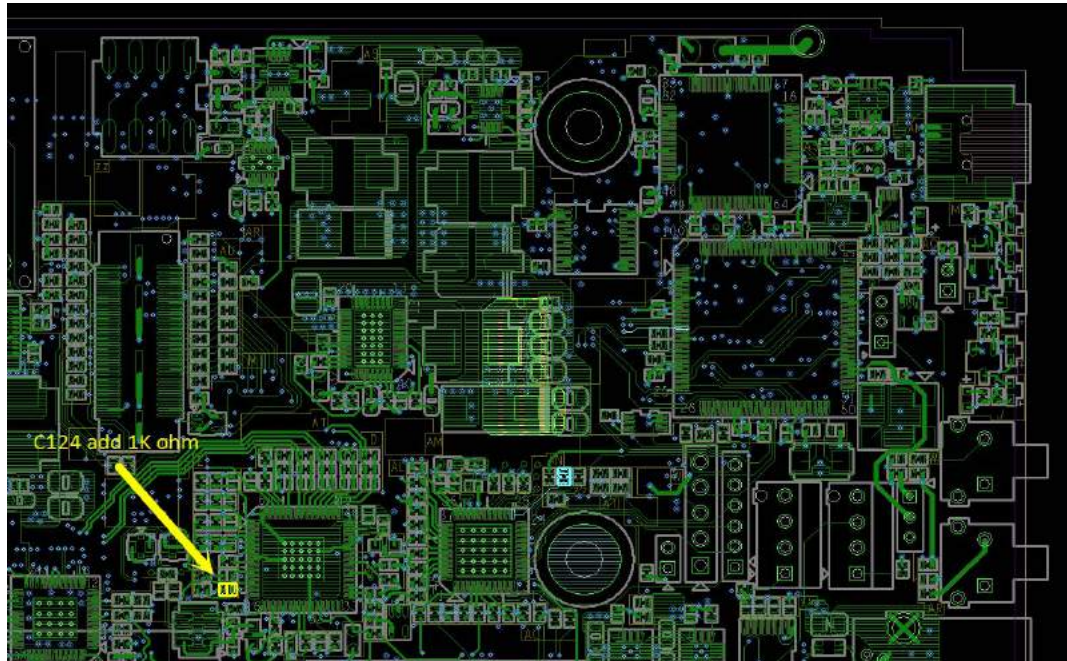
- **Description:** USB 3.0 port could not work even Linux kernel loaded. The cause is 5V rail turned off due to overshoot/undershoot protection.
- **Workaround:** A couple different options are still under investigation for their effectiveness.
 1. Increase 5V overshoot/undershoot margin in with UCD9090 XML File (UCD9090_104_A04.XML) in TI Fusion Power Manager Tool so 5V rail would not be turned off.
 2. Remove C387 (56pf) extra capacitor on 5V rail to solve overshoot/undershoot symptom. (The solution will be applied from Rev 3.0 EVM and later revisions.)



- **Plans for a fix:** C387 will be removed from Rev 3.0 EVM. User who has Rev 2.0 EVM could choose to remove C387 or apply updated xml file to solve the symptom.

4.3 SoC PWR stop on Power-up

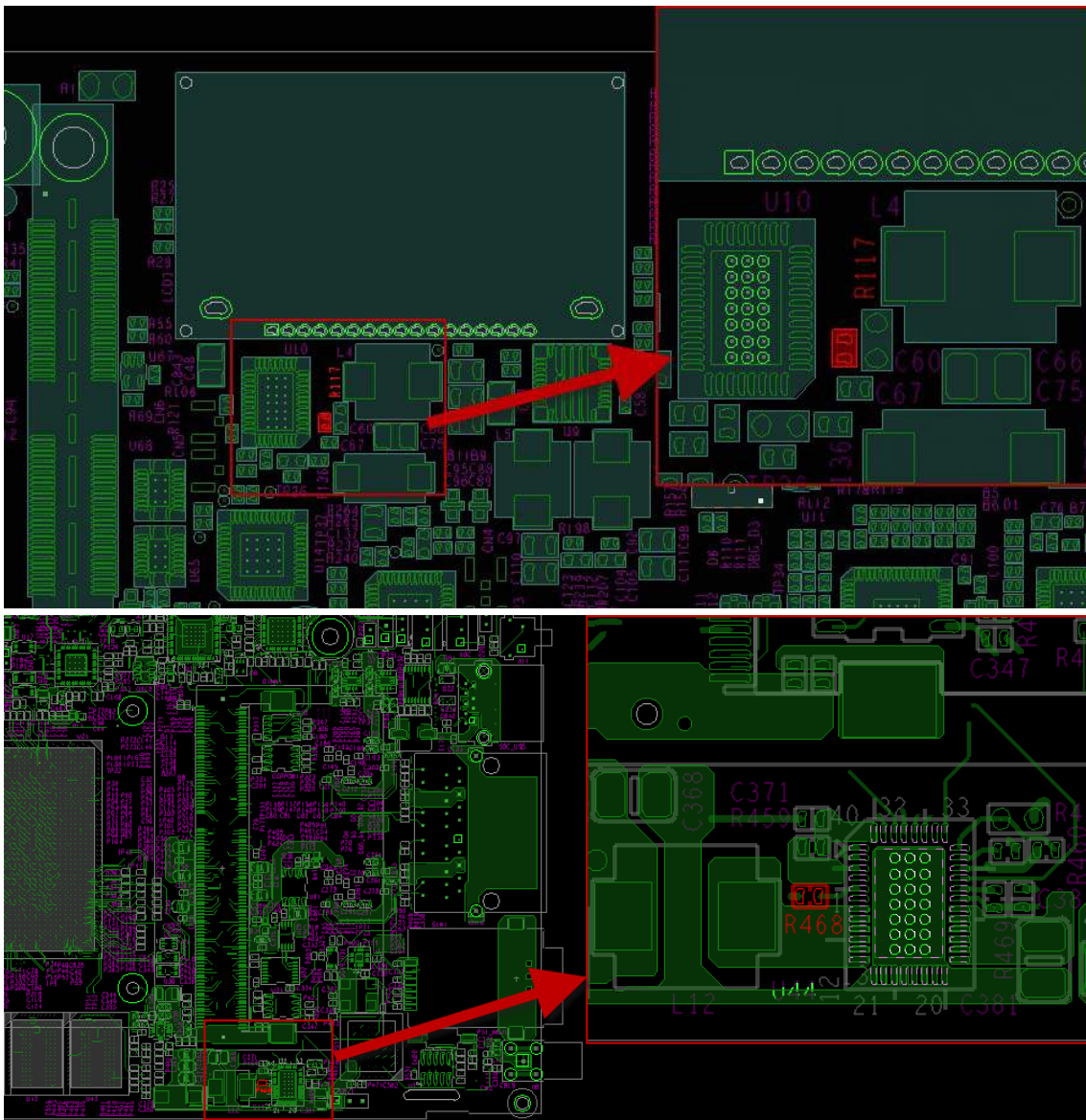
- Description: UCD controller detects a fault during power-on and aborts the power-on sequence.
- Workaround: The fault comes from un-used CVDDT rail and FLT pin is floating. Adding a 1K ohm resistor on location C124 will pull-down the un-used FLT pin and avoid false fault signal.

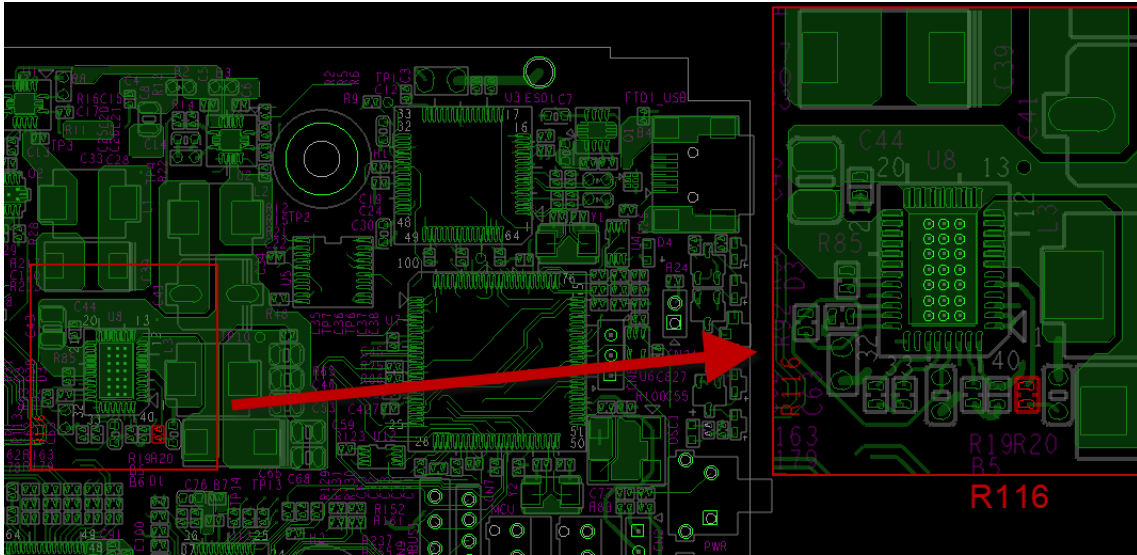


- Plans for a fix: The 1Kohm resistor is added before Rev 2.0 EVM shipping.

4.4 Warning Messages in TFTP test on NAND Flash

- **Description:** When performing TFTP test on NAND in Linux, there are warning messages frequently. The symptom is related to power phase noise coupling on EMIF signals. Increasing boot resistor value could mitigate the issue but won't solve the issue completely.
- **Workaround:**
 1. Change R117 from 0 ohm to 10 ohm (boot resistor for CVDD/U10/UCD74120)
 2. Change R468 from 0 ohm to 10 ohm (boot resistor for CVDD/U44/UCD74120)
 3. Change R116 from 0 ohm to 10 ohm (boot resistor for VCC1V5/U8/UCD74111)





- Plans for a fix: This issue is found in Rev 3.0 and it will also affect Rev 2.0 EVM. The resistor value change will be installed on all Rev 3.1 board before shipping. Root causes are still under investigation.

5. EVMK2HX Rev 2.0 Hardware Modifications

The schematics and layout design are modified for Rev 2.0 EVM, and major differences from Rev 1.0/1.1 EVM are described as below:

5.1 Design Changes:

1. Combine CVDD and CVDDT power rail
2. Change Boot resistor R116, R117, R468 from 10 ohm back to 0 ohm
3. Swap nets EXP_SCL2_3V3 and EXP_SDA2_3V3 on U54
4. Change on-board RAM (U39, U40, U41, U42, U43) from 128Mbit x16 to 256Mbit x16
5. Change EMIF termination resistor to EMIF buffers (U63, U64, U65, U68) for solving signal reflection issue
6. Connect enable pin of USB VBUS switch (U59) to SoC instead of enable directly
7. Rename "VDDAHV" rail to "AVDDAHV"
8. Rename "VDD0V85" rail to "AVDDALV"
9. Modify PCB stack-up so Top/Bottom layers are 1.2 oz (0.5 oz originally) and the inner Power/GND layers are 1.0 oz (0.5 oz originally) in thickness for sustaining larger AC ripple current.

Also, following reworks are installed on Rev 2.0 EVM before shipping:

5.2 EMIF and NAND Test cannot be synchronized

- Workaround:
 1. Add inverter (SN74LVC1G04DVR).
 2. Add wire (30AWG) from inverter PIN 3 to C843.1 (GND),
 3. Add wire (30AWG) from inverter PIN 5 to C843.2 (VCC1V8)
 4. Add wire (30AWG) from inverter PIN 2 to R27.1 (SOC_EMIFCE0Z)
 5. Add wire (30AWG) from inverter PIN 4 to U66.19 (EMIF_OEz).

5.3 Power up will happen SoC PWR stop

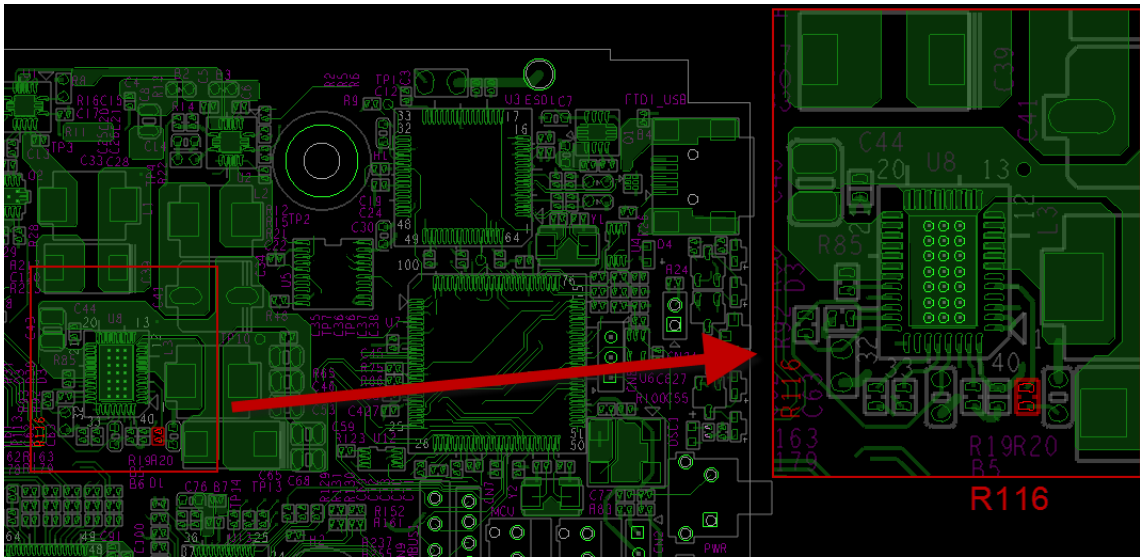
- Workaround: Add a 1K ohm resistor on to GND.

6. EVMK2HX Rev 3.0 Known Issues

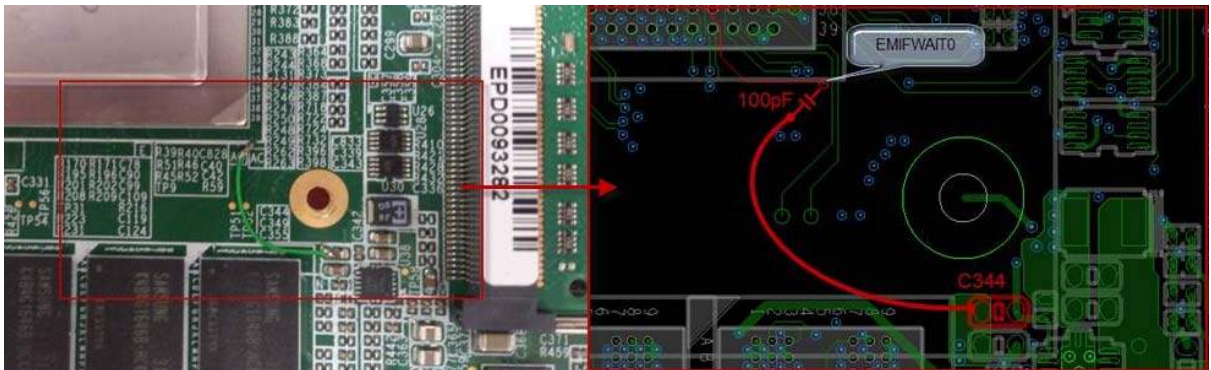
6.1 Warning Messages in TFTP test on NAND Flash

- Description: When performing TFTP test on NAND in Linux, there are warning messages frequently. The symptom is related to power phase noise coupling on EMIF signals. Increasing boot resistor value could mitigate the issue but won't solve the issue completely. (This is the same issue as 4.4.)
- Workaround:
 1. Change R117 from 0 ohm to 10 ohm (boot resistor for CVDD/U10/UCD74120)
 2. Change R468 from 0 ohm to 10 ohm (boot resistor for CVDD/U44/UCD74120)
 3. Change R116 from 0 ohm to 10 ohm (boot resistor for VCC1V5/U8/UCD74111)





Plans for a fix: The resistor value change will be installed on all Rev 3.1 board before shipping. If there are still NAND warning messages, please perform following rework: “add 100pF on R/B# of EMIF interface close to SoC (on the via of net “EMIFWAIT0”, green print on the via should be removed) and add GND connection to pin1 of C344”.



7. EVMK2HX Rev 3.0 Hardware Modifications

The schematics and layout design are modified for Rev 3.0 EVM, and major differences from Rev 2.0 EVM are described as below:

7.1 Design Changes:

1. Un-mount R812 for EMIF buffer OE control (page 13).
2. Add inverter U69 to solve NAND access issue on EMIF interface (page 19).
3. Add U70 (SN74LVC1G07) for USBDRVVBUS control (page 15).
4. Remove C387 to optimize VCC5 feedback compensation (page 43).
5. Add R815, R816, R817 pull down resistors for clock PDN (page 25, 26, 27).
6. Change R310 from 3K ohm to 200 ohm for USB PHY PVT Sense path (page 15).

8. EVMK2HX Rev 4.0 Hardware Modifications

There is no major change of schematics and layout design between Rev 3.0 and Rev 4.0. But SoC and memory IC will be changed to new parts:

8.1 Design Changes:

1. Change SoC (U1) from PG 1.1 to PG 2.0.

EVM	PG 1.1 SoC P/N	PG 2.0 SoC P/N
TCIEVMK2X	TCI6638K2KAXAA	TCI6638K2KBXAA24
EVMK2HX	66AK2H14AXAAW	66AK2H14BXAAW24
EVMK2H	66AK2H14BAAW	66AK2H14BAAW24

2. Phase-out original memory IC (Samsung K4B4G1646B/B-die) and switch to new memory IC (Samsung K4B4G1646D/D-die) on U39, U40, U41, U42, U43.

8.2 SoC PWR Failure on Power-up:

- Description: During power on of the board, the BMC controller may detect a fault and will abort the SOC power on sequence. This is caused by instability on some boards in the SOC VDD33 power rail.
- Workarounds:
 1. Normally, turning the EVM off by removing the power and then turning it back on will result in normal operation.
 2. A revised UCD configuration has been created to eliminate this VDD33 supply instability. The digital control loop compensation was changed to put Fz1 at half of the double pole frequency and Fz2 at the double pole frequency. Then the gain was reduced to limit the bandwidth to 5% of the switching frequency. This new UCD9244 XML File configuration is named UCD9244_52_A05.XML. It can be loaded directly in to the UCD9244 controller using the TI tool Fusion Digital Power Designer. A script is also available to perform a field update through the serial port using the BMC. This script file is named UCD9244_52_A05.txt. These files are available on this website. Please follow the instructions at http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update to perform this field update.
- Plans for a fix: Correct configuration will be programmed in future builds of EVMs

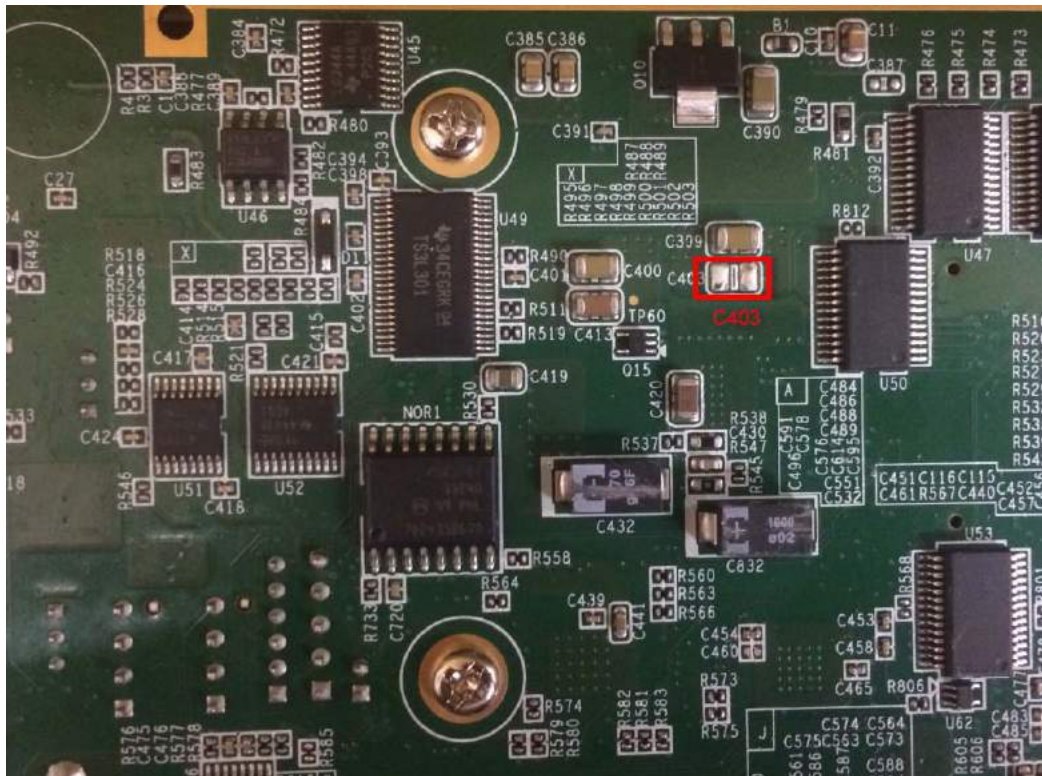
8.3 USB Device failures

- Description: USB not functional after power-up even after Linux kernel loaded. The cause is power supply instability of the VCC5 supply on some boards. This instability

occurs because the VCC5 supply has no load at startup until after the USB port is enabled in host mode. Once USB is enabled in host mode, the instability is eliminated.

▪ Workarounds:

1. Perform a field update of the UCD9090 power supply sequence and fault monitoring configuration. The VCC5 supply overshoot and undershoot fault limits are set at 30% (rather than 15%) in with UCD9090 XML configuration file UCD9090_104_A04_TI_30%_20151120.XML. This will prevent oscillation at start-up from causing the VCC5 supply to shut down. This can be loaded directly using the TI tool Fusion Digital Power Designer. Alternately, a script is also available to perform a field update through the serial port using the BMC. This script file is named UCD9090_104_A04_TI_30%_20151120.txt. These files are available on this website. Please follow the instructions at http://processors.wiki.ti.com/index.php/EVMK2H_Hardware_Setup#UCD_Power_Management_Field_Update) to perform this field update. This workaround is only recommended for customers that are having USB failures on existing EVMs that have already left Advantech's factory.
2. The instability can be resolved by adding a small load to the VCC5 supply. You can install a 510 ohm resistor on the NL capacitor location C403. This location is shown in the picture below. Note: this is on the back-side of the board.



- Plans for a fix: C403 will be stuffed with a 510 ohm resistor on all new production units. The UCD9090 configuration loaded will contain the standard 15% limits for overshoot and undershoot.