ADVANTECH

Enabling an Intelligent Planet

AMD E8860

PCIe® ADD-IN BOARD

Datasheet

(GFX-A5T8-40NST1)

CONTENTS

1. Feature

Model Name	GFX-A5T8-40NST1
Graphics Processing Unit	
GPU	AMD Radeon E8860
Process Technology	28nm
GPU TDP	37W
Graphics Engine Operating Frequency (max)	625Mhz
MXM type	MXM 3.0A,Type A
CPU Interface	PCI Express® 3.0 (x1, x2, x4, x8, x16)
Shader Processing Units	8 SIMD engines x 80 processing elements = 640 shaders
Floating Point Performance	768GFLOPs peak single-precision 48FLOPs peak double-precision
DirectX® capability	DirectX® 11.1
Shader Model	Shader Model 5.0
OpenGL	OpenGL 4.1+
OpenCL	OpenCL 1.1/1.2+
Unified Video Decoder (UVD)	UVD3 for H.264, VC-1, MPEG-2, MPEG-4 part 2 decode
Memory	
Operating Frequency (max)	1125 MHZ / 4.5 Gbps
Configuration, type	128-bit wide, 2 GB, GDDR5

2. Functional Overview

2.1. Memory Configuration Support

AMD Radeon™ E8860 has four DRAM sequencers. Each DRAM channel is 32-bit wide. Four 128 Mb × 32 GDDR5 memory chips are embedded on the ASIC for a total of 2 GB memory.

2.2. Acceleration Features

- Support for all DirectX® 11 features, including the full-speed 32-bit floating point per component operation:
  - Shader Model 5.0 geometry and pixel support in a unified shader architecture:
    - Vertex, pixel, geometry, compute, domain, and hull shaders.
    - 32- and 64-bit floating-point processing per component.
    - New advanced shader instructions, including flexible flow control with CPU-level flexibility on branching.
    - A nearly unlimited shader-instruction store, using an advanced caching system.
    - An advanced shader design, with an ultra-threading sequencer for high-efficiency operations.
    - A new advanced shader core, supporting native scalar instructions.
    - Advanced, high-performance branching support, including static and dynamic branching.
    - High dynamic-range rendering with floating-point blending, texture filtering, and anti-aliasing support.
    - 16- and 32-bit floating-point components for high dynamic-range computations.
    - Full anti-aliasing on renderable surfaces up to and including 128-bit floating-point formats.
    - A new read/write caching system, replacing texture cache with a unified read-write two-level cache.
- Support for OpenGL 4.1/4.1+.
- Support for OpenCL™ 1.1/1.2+.
- Anti-aliasing filtering:
  - 2×/4×/8× MSAA (multi-sample anti-aliasing) modes are supported.
  - A multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Custom filter anti-aliasing with up to 12-samples per pixel.
  - An adaptive anti-aliasing mode.
  - Lossless color compression (up to 16:1).
- Anisotropic filtering:
  - Continuous anisotropic with 1× through 16× taps.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved anisotropic filtering with unified non-power of two-tap distribution and higher precision filter computations.

- Advanced texture compression (3Dc+™).
- High quality 4:1 compression for normal and luminance maps.
- Angle-invariant algorithm for improved quality.
- Single- or two-channel data format compatibility.

- 3D resources virtualized to a 40-bit virtual addressing space, for support of large numbers of render targets and textures.
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Programmable arbitration logic maximizes memory efficiency and is software upgradeable.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.
- Lossless z-buffer compression for both z and stencil.
- Fast z-buffer clear.
- Fast color-buffer clear.
- Z-cache optimized for real-time shadow rendering.
- Z- and color-compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.3. Avivo™ Display System

- The AMD Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on six independent display controllers.
- The full features of the AMD Avivo display system are outlined in the following sections.

- Six independent display controllers that support true 30-bpp (bits per pixel) throughout the display pipe.
- Support for display resolutions up to 4096 × 2160 @ 30 Hz per display output, which do not oversubscribe available memory bandwidth.
- Flexible support for various combinations of display outputs based on clock dependencies:
  - Two internal display PLLs (phase-locked loops) and an integrated DisplayPort reference clock can support:
    - Any two legacy displays and up to four DisplayPorts, or
    - One legacy display and up to five DisplayPorts, or
    - Six DisplayPorts eDP (embedded DisplayPort) is also considered a DisplayPort).
- Advanced video capabilities, including high-fidelity gamma, color correction, and scaling.
- A high-precision color pipe with the support of XR-biased sRGB and xvYCC formats.
- An adaptive per-pixel de-interlacing and frame-rate conversion (temporal filtering).
- An enhanced dithering algorithm for LCD panels.
- Full RMX for sources up to 2560 pixels/line.
- HDCP can be supported on six independent displays, such as HDMI™, DVI, or DisplayPort.
  - **Note:** HDCP is available only to licensed HDCP buyers.
- HDCP Protection:
  - Key information is stored in the ASIC.

- An external ROM is not needed.
- Protects both audio and video content on all HDMI/DisplayPort outputs.

- Adaptive backlight modulation to reduce panel-power consumption in embedded applications.
- An improved memory-access pattern to reduce the memory-power consumption in embedded applications.
- 3D display capabilities for both graphic and overlay contents.

2.4. DVI/HDMI™/DisplayPort Features

- On TMDSA, TMDSB, TMDSC, and TMDSD the following display configurations are supported.
  - Two single-link DVIs (any two from TMDSA, TMDSB, TMDSC, and TMDSD)
  - Two dual-link DVIs
  - HDMI
- On LVDSE and LVDSF the following display configurations are supported.
- One dual-link LVDS
- One single-link LVDS
- One dual-link DVI
- Two single-link DVIs
- HDMI
  - On TMDPA, TMDPB, TMDPC, and TMDPD the following display configurations are supported (See Table 3–3 (p. 24)):
- Four version 1.2 DisplayPorts
  - On LVDPE and LVDPF the following display configurations are supported.
- Two version 1.2 DisplayPorts
  - Optional dithering or frame modulation from the 30-bpp internal display pipeline to 24- or 18-bit outputs on the DVI/HDMI/DisplayPort if not using a 30-bpp output mode.

2.5. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output.
- Supports industry-standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person.
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—162 MP/s (megapixels per second) for single-link DVI
  - DVI—268.5 MP/s for dual-link DVI
  - HDMI—297 MP/s.
- Compliant with the DVI electrical specification.
- The HDMI specification meets the Windows Vista® logo requirements.

2.6. DisplaPort 1.2 Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.2* and the following optional features on links A, B, C, D, E, and F:
  - ACM packet-type support.
- ISRC packet-type support.
  - Each DisplayPort link can transport up to six video streams; one from each display engine.
  - Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
- Four, two, or one lane(s).
- 5.4-, 2.7-, or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 718 MP/s for 24 bpp or 574 MP/s for 30 bpp.
    - 2560 × 2048 @ 60Hz, 30 bpp is supported.
  - Examples of supported pixel-rate/resolution for two lanes at 5.4-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
    - 2560 × 1600 @ 60Hz, 30 bpp is supported.
- Enhanced audio capabilities:
  - Supports PCM audio rates up to 192 kHz.
  - Dolby-TrueHD bit stream and DTS-HD Master Audio bit stream capable.

2.7. Integrated HD-Audio Controller (Azalia) and Codec

- HD-audio HDMI, DisplayPort, and wireless display outputs.
  - Multiple output stream DMAs.
  - Maximum output bandwidth of 73.728 Mbit/s.
  - Low power ECN support.
  - Hardware silent stream.
  - Function level reset.
  - Compatible Microsoft® UAA driver support for basic audio.
  - For advanced functionality (as follows), an AMD or a third party driver is required.
  - LPCM:
    - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
    - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
    - Bits per sample: 16, 20, and 24
- Non-HBR Compressed audio pass-through up to 6.144 Mbps:

- Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD.

- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD.
- Plug-and-Play:
  - Sink audio format capabilities declaration.
  - Sink information.
  - AV association.
- Lip sync information.
- HDCP content protection.

2.8. LVDS

- Single- or dual-link LVDS transmitter, which takes output from either one of the internal display controllers.
- Integrated with a built-in self-biasing circuitry.
- LVDS can operate in either single- or dual-channel mode supporting displays from XGA (or below) up to QXGA.
- LVDS can drive either 18- or 24-bpp displays with several dithering options from the internal 30-bpp display controller.
- Ratiometric expansion and compression supported on reduced-blank panels.
- Three-pairs (+1 clock) and four-pairs (+1 clock) modes for both single- and dual-channel LVDS.
- FPDI-2 compliant; compatible with receivers from National Semiconductor, Texas Instruments, and THine.
- LVDS eye pattern to improve testability of the LVDS module.
- Compliant with the electrical specifications of ANSI/TIA/EIA-644.
- CRT DAC
- One integrated triple 10-bit DAC with built-in reference circuit, which takes output from either one of the internal display controllers (primary or secondary).
- A single RGB-CRT output.
- Support for the stereo-sync signal to drive a 3D display.
- A maximum pixel frequency of 400 MHz.
- An individual power-down feature for each of the three guns.
- Compliant with the VSIS electrical specification.
- Integrated with a built-in bandgap reference circuitry.
- A static detection circuitry (S_detect) for hot-plug/unplug capability.
- An integrated static monitor-detection circuit.

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- An integrated static monitor-detection circuit.

2.10. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Fully inter-operative with PCI Express Base Specification Revision 2.1 and earlier devices.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

3. PIN Assignment and Description

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
E1	PWR_SRC_E1	Main power source 7-20V (recommend using 12V)	E2	PWR_SRC_E2	Main power source 7-20V (recommend using 12V) up to 10A
E3	GND_E3	GND	E4	GND_E4	GND
1	5V_1	5V +/- 5%	2	PRSNT_R#_2	MXM module present detects. Weak pull-up required on system if module detection is desired. Module pin is connected to ground.
3	5V_3	5V +/- 5%	4	WAKE#_4	N/A
5	5V_5	5V +/- 5%	6	PWR_GOOD_6	Power sequencing sideband. The module will assert this signal when all its internal power regulators are within the required tolerance.
7	5V_7	5V +/- 5%	8	PWR_EN_8	Module power enables. System must assert this signal to power on the module. May be asserted only after all input rails are within the specified tolerance.
9	5V_9	5V +/- 5%	10	N/A	N/A
11	GND_11	GND	12	N/A	N/A
13	GND_13	GND	14	N/A	N/A
15	GND_15	GND	16	N/A	N/A
17	GND_17	GND	18	PWR_LEVEL_18	Signals the module to switch to a lower power state. Modules must reduce the power by at least 20% within 50ms.
19	N/A	N/A	20	TH_OVERT#_20	Thermal shutdown request. System must power down the MXM module within 500ms to prevent permanent damage. Pull-up resistor to 3.3V of appropriate value is required on the system board.
21	N/A	N/A	22	TH_ALERT#_22	Thermal interrupt request. Signal may be used by the system to signal to module to reduce power consumption. The signal may also be used by the module to signal to the system a non critical temperature alert. Pull-up resistor to 3.3V of appropriate value is required on the system board.
23	PNL_PWR_EN_23	N/A	24	TH_PWM_24	Thermal PWM. This signal may be used to control a

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
					fan connected to the module thermal solution.
25	PNL_BL_EN_25	Internal panel back-light enable.	26	GPIO0_26	GPIO0
27	PNL_PWM_27	Internal panel PWM brightness control.	28	GPIO1_28	GPIO1
29	HDMI_CEC_29	N/A	30	GPIO2_30	GPIO2
31	DVI_HPD_31	Hot plug detect dedicated for the LVDS/DVI/HDMI port.	32	SMB_DAT_32	SMBus Data
33	LVDS_DDC_DAT_33	DDC clock/data for the LVDS/DVI/HDMI port.	34	SMB_CLK_34	SMBus Clock
35	LVDS_DDC_CLK_35	DDC clock/data for the LVDS/DVI/HDMI port.	36	GND_36	GND
37	GND_37	GND	38	N/A	N/A
39	N/A	N/A	40	N/A	N/A
41	N/A	N/A	42	N/A	N/A
43	N/A	N/A	44	N/A	N/A
45	N/A	N/A	46	GND_46	GND
47	GND_47	GND	48	PEX_TX15#_48	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
49	PEX_RX15#_49	PCI Express® input to the Root Complex. DC blocking caps must be placed on the system board.	50	PEX_TX15_50	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
51	PEX_RX15_51	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	52	GND_52	GND
53	GND_53	GND	54	PEX_TX14#_54	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
55	PEX_RX14#_55	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	56	PEX_TX14_56	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
57	PEX_RX14_57	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	58	GND_58	GND
59	GND_59	GND	60	PEX_TX13#_60	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
					(-)
61	PEX_RX13#_61	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	62	PEX_TX13_62	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
63	PEX_RX13_63	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	64	GND_64	GND
65	GND_65	GND	66	PEX_TX12#_66	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
67	PEX_RX12#_67	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	68	PEX_TX12_68	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
69	PEX_RX12_69	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	70	GND_70	GND
71	GND_71	GND	72	PEX_TX11#_72	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
73	PEX_RX11#_73	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	74	PEX_TX11_74	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
75	PEX_RX11_75	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	76	GND_76	GND
77	GND_77	GND	78	PEX_TX10#_78	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
79	PEX_RX10#_79	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	80	PEX_TX10_80	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
81	PEX_RX10_81	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	82	GND_82	GND
83	GND_83	GND	84	PEX_TX9#_84	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
					(-)
85	PEX_RX9#_85	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	86	PEX_TX9_86	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
87	PEX_RX9_87	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	88	GND_88	GND
89	GND_89	GND	90	PEX_TX8#_90	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
91	PEX_RX8#_91	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	92	PEX_TX8_92	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
93	PEX_RX8_93	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	94	GND_94	GND
95	GND_95	GND	96	PEX_TX7#_96	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
97	PEX_RX7#_97	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	98	PEX_TX7_98	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
99	PEX_RX7_99	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	100	GND_100	GND
101	GND_101	GND	102	PEX_TX6#_102	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
103	PEX_RX6#_103	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	104	PEX_TX6_104	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
105	PEX_RX6_105	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	106	GND_106	GND
107	GND_107	GND	108	PEX_TX5#_108	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
					(-)
109	PEX_RX5#_109	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	110	PEX_TX5_110	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
111	PEX_RX5_111	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	112	GND_112	GND
113	GND_113	GND	114	PEX_TX4#_114	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
115	PEX_RX4#_115	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	116	PEX_TX4_116	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
117	PEX_RX4_117	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	118	GND_118	GND
119	GND_119	GND	120	PEX_TX3#_120	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
121	PEX_RX3#_121	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	122	PEX_TX3_122	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
123	PEX_RX3_123	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	124	GND_124	GND
125	GND_125	GND	126	KEY	
127	KEY		128	KEY	
129	KEY		130	KEY	
131	KEY		132	KEY	
133	GND_133	GND	134	GND_134	GND
135	PEX_RX2#_135	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	136	PEX_TX2#_136	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
137	PEX_RX2_137	PCI Express input to the Root Complex. DC blocking caps must	138	PEX_TX2_138	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
		be placed on the system board.			(+)
139	GND_139	GND	140	GND_140	GND
141	PEX_RX1#_141	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	142	PEX_TX1#_142	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
143	PEX_RX1_143	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	144	PEX_TX1_144	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
145	GND_145	GND	146	GND_146	GND
147	PEX_RX0#_147	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	148	PEX_TX0#_148	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (-)
149	PEX_RX0_149	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.	150	PEX_TX0_150	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board. (+)
151	GND_151	GND	152	GND_152	GND
153	PEX_REFCLK#_153	PCI Reference Clock Differential Clock (-)	154	CLK_REQ#_154	PCI Express clock request. Pull-up resistor to 3.3V is required on the system board if the function is supported
155	PEX_REFCLK_155	PCI Reference Clock Differential Cock (+)	156	PEX_RST#_156	PCI Express reset signal.
157	GND_157	GND	158	VGA_DDC_DAT_158	DDC Data
159	N/A	N/A	160	VGA_DDC_CLK_160	DDC Clock
161	N/A	N/A	162	VGA_VSYC_162	VGA VSYNC
163	N/A	N/A	164	VGA_HSYC_164	VGA HYNC
165	N/A	N/A	166	GND_166	GND
167	N/A	N/A	168	VGA_RED_168	VGA RED
169	LVDS_UCLK#_169	LVDS clock output for dual-link displays.	170	VGA_GREEN_170	VGA GREEN
171	LVDS_UCLK_171	LVDS clock output for dual-link displays	172	VGA_BLUE_172	VGA BLUE
173	GND_173	GND	174	GND_174	GND
175	LVDS_UTX3#_175	LVDS/DVI output for dual-link	176	LVDS_LCLK#_176	LVDS/DVI/HDMI clock output for single and

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
		displays (upper/even link).			dual-link displays (lower/odd link)
177	LVDS_UTX3_177	LVDS/DVI output for dual-link displays (upper/even link).	178	LVDS_LCLK_178	LVDS/DVI/HDMI clock output for single and dual-link displays (lower/odd link)
179	GND_179	GND	180	GND_180	GND
181	LVDS_UTX2#_181	LVDS/DVI output for dual-link displays (upper/even link).	182	LVDS_LTX3#_182	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
183	LVDS_UTX2_183	LVDS/DVI output for dual-link displays (upper/even link).	184	LVDS_LTX3_184	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
185	GND_185	GND	186	GND_186	GND
187	LVDS_UTX1#_187	LVDS/DVI output for dual-link displays (upper/even link).	188	LVDS_LTX2#_188	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
189	LVDS_UTX1_189	LVDS/DVI output for dual-link displays (upper/even link).	190	LVDS_LTX2_190	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
191	GND_191	GND	192	GND_192	GND
193	LVDS_UTX0#_193	LVDS/DVI output for dual-link displays (upper/even link).	194	LVDS_LTX1#_194	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
195	LVDS_UTX0_195	LVDS/DVI output for dual-link displays (upper/even link).	196	LVDS_LTX1_196	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
197	GND_197	GND	198	GND_198	GND
199	DP_C_L0#_199	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	200	LVDS_LTX0#_200	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
201	DP_C_L0_201	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	202	LVDS_LTX0_202	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
203	GND_203	GND	204	GND_204	GND
205	DP_C_L1#_205	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	206	DP_D_L0#_206	DisplayPort D. DC blocking caps must be placed on the system board.
207	DP_C_L1_207	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	208	DP_D_L0_208	DisplayPort D. DC blocking caps must be placed on the system board.
209	GND_209	GND	210	GND_210	GND
211	DP_C_L2#_211	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	212	DP_D_L1#_212	DisplayPort D. DC blocking caps must be placed on the system board.

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
213	DP_C_L2_213	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	214	DP_D_L1_214	DisplayPort D. DC blocking caps must be placed on the system board.
215	GND_215	GND	216	GND_216	GND
217	DP_C_L3#_217	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	218	DP_D_L2#_218	DisplayPort D. DC blocking caps must be placed on the system board.
219	DP_C_L3_219	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.	220	DP_D_L2_220	DisplayPort D. DC blocking caps must be placed on the system board.
221	GND_221	GND	222	GND_222	GND
223	DP_C_AUX#_223	DisplayPort C auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.	224	DP_D_L3#_224	DisplayPort D. DC blocking caps must be placed on the system board.
225	DP_C_AUX_225	DisplayPort C auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.	226	DP_D_L3_226	DisplayPort D. DC blocking caps must be placed on the system board.
227	N/A	N/A	228	GND_228	GND
229	N/A	N/A	230	DP_D_AUX#_230	DisplayPort D auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
231	N/A	N/A	232	DP_D_AUX_232	DisplayPort D auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
233	N/A	N/A	234	DP_C_HPD_234	DisplayPort C hot plug detect.
235	N/A	N/A	236	DP_D_HPD_236	DisplayPort D hot plug detect.
237	N/A	N/A	238	N/A	N/A
239	RSVD_239	N/A	240	N/A	N/A
241	RSVD_241	N/A	242	N/A	N/A
243	RSVD_243	N/A	244	GND_244	GND
245	RSVD_245	N/A	246	DP_B_L0#_246	DisplayPort B. DC blocking caps must be placed on the system board.
247	RSVD_247	N/A	248	DP_B_L0_248	DisplayPort B. DC blocking caps must be placed on the system board.
249	RSVD_249	N/A	250	GND_250	GND

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
251	GND_251	GND	252	DP_B_L1#_252	DisplayPort B. DC blocking caps must be placed on the system board.
253	DP_A_L0#_253	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	254	DP_B_L1_254	DisplayPort B. DC blocking caps must be placed on the system board.
255	DP_A_L0_255	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	256	GND_256	GND
257	GND_257	GND	258	DP_B_L2#_258	DisplayPort B. DC blocking caps must be placed on the system board.
259	DP_A_L1#_259	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	260	DP_B_L2_260	DisplayPort B. DC blocking caps must be placed on the system board.
261	DP_A_L1_261	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	262	GND_262	GND
263	GND_263	GND	264	DP_B_L3#_264	DisplayPort B. DC blocking caps must be placed on the system board.
265	DP_A_L2#_265	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	266	DP_B_L3_266	DisplayPort B. DC blocking caps must be placed on the system board.
267	DP_A_L2_267	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	268	GND_268	GND
269	GND_269	GND	270	DP_B_AUX#_270	DisplayPort B auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
271	DP_A_L3#_271	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	272	DP_B_AUX_272	DisplayPort B auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
273	DP_A_L3_273	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.	274	DP_B_HPD_274	DisplayPort B hot plug detect.
275	GND_275	GND	276	DP_A_HPD_276	DisplayPort A hot plug detect.
277	DP_A_AUX#_277	DisplayPort A auxiliary channel/DDC. DC blocking caps must be placed on the system	278	3V3_278	3.3V +/-5%

Pin#	Pin Name	Pin Description	Pin#	Pin Name	Pin Description
		board.			
279	DP_A_AUX_279	DisplayPort A auxiliary channel/DDC. DC blocking caps must be placed on the system board.	280	3V3_280	3.3V +/-5%
281	PRSNT_L#_281	MXM module present detects. Weak pull-up required on system if module detection is desired. Module pin is connected to ground.			

4. Power Consumption

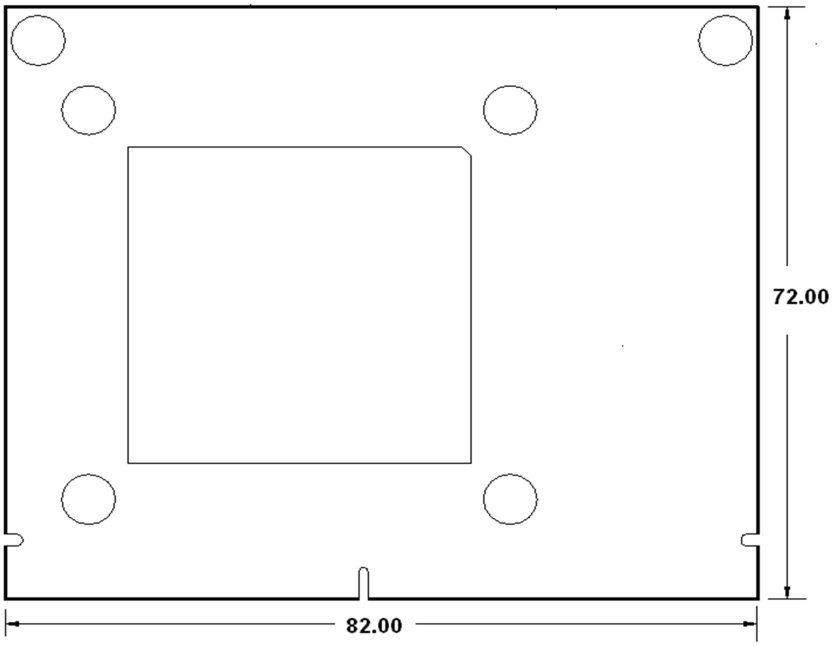
Application	Total ASIC Power + DRAM Power (W)
Static Windows - 65c	**5.86**

Application	Total ASIC Power + DRAM Power (W)
3D Mark Vantage FT6	**30.73**

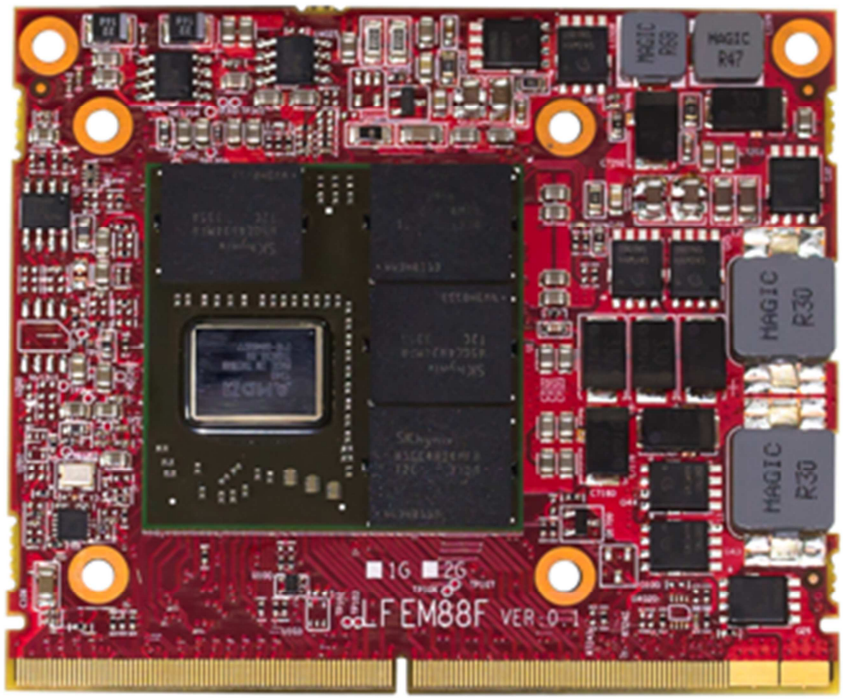
5. Board Dimension

5.1 Board Dimension

(Unit : mm)



Tolerances: +/_ 0.13 mm



Change log or update history

Rev.	Date	Description
0.1	2014/3/27	1st Draft.