TOSHIBA

2.5 type Disk Drives
MK6476GSX
MK5076GSX
MK3276GSX
MK2576GSX
MK1676GSX
MK1276GSX
Product Specification

株式会社　東芝

TOSHIBA CORPORATION

No.
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TOSHIBA

TITLE: 2.5 type Disk Drives MK6476/5076/3276/2576/1676/1276GSXroduct Specification

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SAFETY

The hard disk drive and product specifications contain essential information for the protection of users and others from possible injury and property damage and to ensure correct handling. Please check that you fully understand the definition of the following messages (signs and graphical symbols) before going on to read the text, and always follow the instructions. Please describe requirements in the instruction manual of the product in which the drive is mounted and ensure that users are made thoroughly aware of them.

IMPORTANT MESSAGES

Read this manual and follow its instructions. Signal words such as CAUTION and NOTE, will be followed by important safety information that must be carefully reviewed.

⚠CAUTION	Indicates a potentially hazardous situation which if not avoided, may result in minor injury or property damage.
NOTE	Gives you helpful information.

LIMITATION OF LIABILITY

- Toshiba Corporation shall not be liable for any damage due to the fault or negligence of users, fire, earthquake, or other accident beyond the control of Toshiba Corporation.
- Toshiba Corporation shall not be liable for any incidental or consequential damages including but not limited to change or loss of stored data, loss of profit, or interruption of business, which are caused by use or non-usability of the product.
- Toshiba Corporation shall not be liable for any damage result from failure to comply with the contents in the product specification.
- Toshiba Corporation shall not be liable for any damage based on use of the product in combination with connection devices, software, or other devices provided by Toshiba Corporation with the product.

USAGE RESTRICTIONS

- Since the drive is not designed or manufactured to be used for a system including equipment (*1) directly linked with human life, etc., Toshiba Corporation shall not be liable for this type of use.

  *1: Equipment directly linked with human life, etc. corresponds to the following.

  －Medical equipment such as life support systems, equipment used in operations, etc.

- When the drive is to be used for a system including equipment (*2) linked with human safety or having a serious influence on the safe maintenance of public function, etc., special consideration (*3) must be given with regard to operation, maintenance, and management of the system.

  *2: A system including equipment linked with human safety or having a serious influence on the safe maintenance of public function, etc. corresponds to the following.

  －A main equipment control system used in atomic power plants, a safety protection based system used in atomic facilities, other important safety lines and systems.

  －An operation control system for mass transport, an air-traffic control system.

  *3: Special consideration means that a safety system (fool proof design, fail safe design, redundancy design, etc.) is established as a result of adequate consultation with Toshiba engineers.

SAFETY

⚠CAUTION
■ Do not disassemble, remodel or repair. Disassembly, remodeling or repair may cause injury, failure, or data loss.
■ Do not drop. Dropping may cause injury.
■ Do not touch sharp edges or pins of the drive. Sharp protrusions etc. may cause injury. Hold the drive by both sides when carrying it.

SAFETY

Observe the following to prevent failure, malfunction or data loss.

NOTE

●Follow the specifications for 6. POWER SUPPLY (page15), 8. ENVIRONMENT (page 21), etc. when using.

Failure to do so may cause damage to the drive.

●Observe cautions in 7.4 MOUNTING INSTRUCTION (page16) and 9.6 LOAD / UNLOAD (page26) when handling, setting up, or using the drive.

●Take anti-static measures in order to avoid damage to the drive when handling it.

The drive uses parts susceptible to damage due to ESD (electrostatic discharge).
Wear ESD proof wrist strap in accordance with the usage specified when handling a drive that is not in an anti-static protection bag.

●There is a certain probability of the drive causing failure including data error or data loss.

Take preventive steps such as backing up data etc. without exception in order to prevent loss etc. in cases where data loss may result in loss or damage.
Please include this in the instruction manual etc. of the system in which this device is used and ensure that users are made thoroughly aware of it.

●Inserting or pulling out the drive when the power is turned on may cause damage to the drive.

Exchange the drive etc. after the power of HDD is turned off.

●Extreme shock to the drive may cause damage to it, data corruption, etc..

Do not subject the drive to extreme shock such as dropping, upsetting or crashing against other objects.

●Do not touch the top cover since application of force to it may cause damage to the drive.

●Do not stack the drive on another drive or on other parts etc. or stack them on top of it during storage or transportation.

Shock or weight may cause parts distortion etc..

●Labels and the like attached to the drive are also used as a seal for maintenance of its performance.

Do not remove them from the drive.

●Attachment of dielectric materials such as metal powder, liquid, etc. to live parts such as printed circuit board patterns or pins etc. may cause damage to the drive.

Avoid attachment of these materials.

●Do not place objects which generate magnetic fields such as magnets, speakers, etc. near the drive.

Magnetism may cause damage to the drive or data loss.

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1. SCOPE

This document describes the specifications of the following model, **MK6476/5076/3276/2576/1676/1276GSX** of 2.5- type Winchester disk drives.

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Factory Number	Sales Number
HDD2J92	MK6476GSX
HDD2J93	MK5076GSX
HDD2J94	MK3276GSX
HDD2J95	MK2576GSX
HDD2J96	MK1676GSX
HDD2J97	MK1276GSX

2. GENERAL DESCRIPTION

The **MK6476/5076/3276/2576/1676/1276GSX** which is noted hereinafter as **"MK6476/5076/3276/2576/1676/1276GSX "** or as " the drive " comprises a series of intelligent disk drives .

The drive features an ATA8 and Serial ATA 2.6 interface embedded controller that requires a simplified adapter board for interfacing to a Serial ATA or Serial ATA compatible bus. The drives employ Winchester technology and a closed loop servo control system which have realized the highest recording density of the series 753.2 M bit/mm^2 (486.0 G bit/in^2, **MK6476/3276/1676GSX**) , 597.1M bit/mm^2(385.2 G bit/in^2, **MK5076/2576/1276GSX**) and average access time of 12 msec with highest reliability of 600,000 hours for MTTF (Mean Time to Failure).

MK6476/5076/3276/2576/1676/1276GSX is distinctive for its small and light body with 9.5mm height and 102 grams of weight.

The **MK6476/5076/3276/2576/1676/1276GSX** consists of an HDA (Head Disk Assembly) and a printed circuit board. The HDA has a sealed module which contains a disk spindle assembly, a head actuator assembly and an air filtration system. This HDA adopts Winchester technology which enhances high reliability. The actuator is a rotary voice coil motor which enables high-speed access.

The disk is driven directly by a DC spindle motor. Air filtration is provided by a high performance air filtration system using both breather and circulation filters.

The drive provides a carriage lock mechanism which is activated automatically upon power down in order to prevent head/media from being damaged when it is not operating or under shipment.

The printed circuit board which is set externally to the HDA and equipped with all the electric circuitry necessary to operate the drive except the head. The power supply and interface signal connectors are mounted on the board. Only the head control IC's are located within the HDA. The circuitry performs the following functions:

Read/Write, OOB Control, FIS Control, Spindle Motor Control, Seek and Head Positioning Servo Control, Abnormal Condition Detection and Shock Sensor Control.

SAFETY

⚠CAUTION	■Do not disassemble, remodel or repair. Disassembly, remodeling or repair may cause injury, failure, or data loss.

NOTE
●There is a certain probability of the drive causing failure including data error or data loss. Take preventive steps such as backing up data etc. without exception in order to prevent loss etc. in cases where data loss may result in loss or damage.
●Do not touch the top cover since application of force to it may cause damage to the drive.
●Do not stack the drive on another drive or on other parts etc. or stack them on top of it during storage or transportation. Shock or weight may cause parts distortion etc..
●Labels and the like attached to the drive are also used as hermetic sealing for maintenance of its performance. Do not remove them from the drive.

3. KEY FEATURES

- High capacity in smallest size

  · 2.5-type 2 platters accommodating formatted capacity of 640.135GB(MK6476GSX)

/500.107GB(MK5076GSX)/320.072GB(MK3276GSX)/250.065GB(MK2576GSX)

/160.041 GB(MK1676GSX)/ 120.034GB(MK1276GSX).

  · Slim (9.5 mm in height) and light (MK6476GSX: 102gram in weight) design.

- Fast access and fast transfer rate

  · Quick spin up of Spindle Motor 3.5 sec.

  · Average access time 12 msec enabled by optimized balance of a head actuator assembly and an efficiently designed magnet of rotary VCM.

  · Interface speed up to 3 gigabits per second.

  · Disk transfer : 1147.1(MK6476/3276/1676GSX)/976.2(MK5076/2576/1276GSX) megabits maximum per second.

  · Read ahead cache and write cache enhancing system throughput.

- Intelligent Interface

  · ATA8/Serial ATA 2.6 interface supported.

  · Quick address conversion in translation mode.

  · Translation mode which enables any drive configuration.

  · Support 28 bit LBA (Logical Block Address) mode commands and 48bit LBA mode commands.

  · Multi word DMA, Ultra-DMA modes and Advanced PIO mode settings / commands supported.

  · Native Command Queue supported.

  · Staggered Spin / Activity supported.

- Data integrity

  · Automatic retries and corrections for read errors.

  · 2320 bits computer generated ECC polynomial with 10 bits symbol 26 burst on-the-fly error correction capability.

- High reliability

  · Powerful self- diagnostic capability.

  · Shock detection with shock sensor circuit for high immunity against operating shock up to 3,920 m/s^2

  (400 G).

  · Automatic carriage lock secures heads on the ramp with high immunity against non operating shock up to 8,820 m/s^2 (900G).

- Low power consumption

  · Low power consumption by Adaptive Power Mode.

  · Low power consumption by Serial ATA Device Initiated Power Management.

4. BASIC SPECIFICATION

MODEL	MK6476/3276/1676GSX	MK5076/2576/1276GSX
Formatted Capacity(gigabytes)	640.135GB 320.072GB 160.041GB	500.107GB 250.059GB 120.034GB
Servo design method	Sector Servo	
Recording method	Iterative-Noise Predictive PR+NLV	
Recording density		
Track / mm (TPI)	11635(296k) typical	10472(266k) typical
Bit / mm max. (BPI max.)	64.4k(1636.9k) typical	56.4k(1432.6k) typical
Bit / mm2 max. (bpsi max.)	750.8M(484.4G) typical	591.4M(381.6G) typical
Number of disks	2/1/1	2/1/1
Number of data heads	4/2/1	4/2/1
Number of user data cylinders	187231 typical	168511 typical
Bytes per sector	512	

Note:One gigabyte(GB)=one billion bytes;accessible capacity will be less and actual capacity depends on the operating environment and formation.

5. PERFORMANCE

Access time (msec) <*1>	
Track to track seek <*2>	2
Average seek <*3>	12
Max. seek <*4>	22
Rotation speed (RPM)	5,400 $\pm$ 0.1%
Average Latency Time (msec)	5.55
Internal Transfer rate (Mbits / sec)	584.3~ 1195.5 typical
Host Transfer rate (Gbit / sec)	3
Sector Interleave	1:1
Track skew	Yes
Buffer size (Kbytes)	8,192
Cache	Read Ahead Cache Write Cache
Start time <*5> (Up to Drive Ready)	3.5 sec (Typical) 9.5 sec (Maximum)
Recovery time from Stand- by <*5>	3.5 sec (Typical) 9.5 sec (Maximum)
Command Overhead (msec)	1

<*1> Under the condition of normal voltage, 25^{O}C normal temperature and bottom side down.
<*2> Average time to seek all possible adjacent track without head switching.
<*3> Weighted average time to travel between all possible combination of track calculated as below.
Weighted average access time = [Sum of P(n)*t(n)] / [Sum of P(n)], n = 1 to N.
Where, N ; Total number of tracks.
P(n); Total number of seek for stroke n [= 2*(N - n)].
t(n); Average seek time for stroke n.
Average seek time to seek to stroke n is the average time to 1,000 seeks for stroke n, with random head switches.
<*4> Average time for 1,000 full stroke seeks with random head switches.
<*5> Typical values are for the condition of normal voltage, 25^{O}C normal temperature and placing bottom side down. Maximum values are for all conditions specified in this document.

6. POWER REQUIREMENTS

6.1 Supply Voltage

Allowable voltage	5V ± 5%
Allowable noise/ripple	100 mV p-p or less
Allowable supply rise time	2 –100 msec

(note 1) When DC power is turned off, +5V voltage must not be lower than 0V.

6.2 Power Consumption

	Average (note 1,2)
	MK6476/5076/3276/2576/1676/1276GSX
Start (note 3)	4.5W Peak,Maximum
Seek (note 4)	1.85W Typical
Read / Write(note 5)	1.5W Typical
Active idle (note 6,7)	0.85W Typical
Low power idle (note 7,8)	0.55W Typical
Stand- by (note 7,9)	0.18W Typical
Sleep(note 7)	0.15W Typical

(note 1) Under normal condition (25^{O}C, 101.3 kPa (1,013 mb)) and 5V ± 0%.

(note 2) The values is DIPM(Device Initiated Power Management) enable.

(note 3) This is the maximum current value between power on to ready and the maximum value is the RMS(Root Mean Square) of 10 ms. Does not include rush current.

(note 4) The seek average current is specified based on three operations per 100 ms.

(note 5) The read/write current is specified based on three operations of 63 sector read/write per 100 ms.

(note 6) Motor is rotating at normal speed but none of Read, Write or Seek is executed.

(note 7) The values are based on using S-ATA power management features. The Partial mode is used for the idle modes power consumption measurements and the Slumber mode is used for Stand-by and Sleep modes power consumption measurements

(note 8) Motor is rotating at normal speed but heads are unloaded on the ramp.

(note 9) Motor is not rotating and heads are unloaded on the ramp.

6.3 Energy Consumption Efficiency

Energy consumption efficiency	Average(W/GB)	Classification
Power consumption at Low power idle / Capacity		
MK6476GSX	0.00086	H
MK5076GSX	0.0011	H
MK3276GSX	0.0017	E
MK2576GSX	0.0022	E
MK1676GSX	0.0034	E
MK1276GSX	0.0045	E

Energy consumption efficiency is calculated in accordance with the law regarding efficiency of energy consumption : Energy saving law, 1979 law number 49.
Calculation of Energy consumption is dividing consumed energy by the capacity.
The consumed energy and capacity shall be measured and specified by the Energy saving low.

7. MECHANICAL SPECIFICATIONS

7.1 Dimension

Width	69.85mm (2.75”)
Height	9.5 mm (0.37”)
Depth	100.0 mm (3.94”)

Figure 1 and Table 7.4-1 show an outline of the drive.

7.2 Weight

MK6476/5076GSX	101 gram (typ.) / 102 gram(max.)
MK3276/2576/1676/1276GSX	97 gram (typ.) / 98 gram(max.)

7.3 Drive Orientation

The drive can be installed in all axes (6 directions).

7.4 Mounting Instructions

SAFETY

NOTE
●Take anti-static measures in order to avoid damage to the drive when handling it. The drive uses parts susceptible to damage due to ESD (electrostatic discharge). Wear ESD proof wrist strap in accordance with the usage specified when handling a drive that is not in an anti-static protection bag.
●Extreme shock to the drive may cause damage to it, data corruption, etc.. Do not subject the drive to extreme shock such as dropping, upsetting or crashing against other objects.
●Do not place objects which generate magnetic fields such as magnets, speakers, etc. near the drive. Magnetism may cause damage to the drive or data loss.

7.4.1 Screwing

Four screws should be tightened equally with 0.39 N·m (4 kgf·cm) torque. The depth should be 3.0 mm min. and 3.5 mm maximum.

7.4.2 Installation

① The drive should be mounted carefully on the surface of 0.1mm or less flatness to avoid excessive distortion.
② In order to prevent short-circuit under any circumstances, the space of 0.5mm or more should be kept under the PCB and the design have to be checked carefully (See fig. 2).
③ Enough space should be kept around the drive especially around the convex portion of HDA (See fig. 2) to avoid any contact with other parts, which may be caused by receiving shock or vibration.
④ The temperature of the top cover and the base must always be kept under 63℃ to maintain the required reliability. (If the drive runs continuously or spins-up frequently, the temperature of the top cover may rise to 15℃ maximum. If the drive is used in ambient temperature of 48℃ or more, it should be kept where adequate ventilation is available to keep the temperature of top cover under 63℃)
⑤ M3 mounting screw holes are tapped directly on the base for electrical grounding between the drive and the base. In order to prevent the drive performance from being affected by the system noise, appropriate evaluation should be conducted before deciding loading method.
⑥ Do not apply force exceeding 2[N] on the Top Cover.
⑦ The drive contains several parts which may be easily damaged by ESD(Electric Static Discharge). Avoid touching the interface connector pins and the surface of PCB. Be sure to use ESD proof wrist strap when handling the drive.
⑧ A rattle heard when the drive is moved is not a sign of failure.

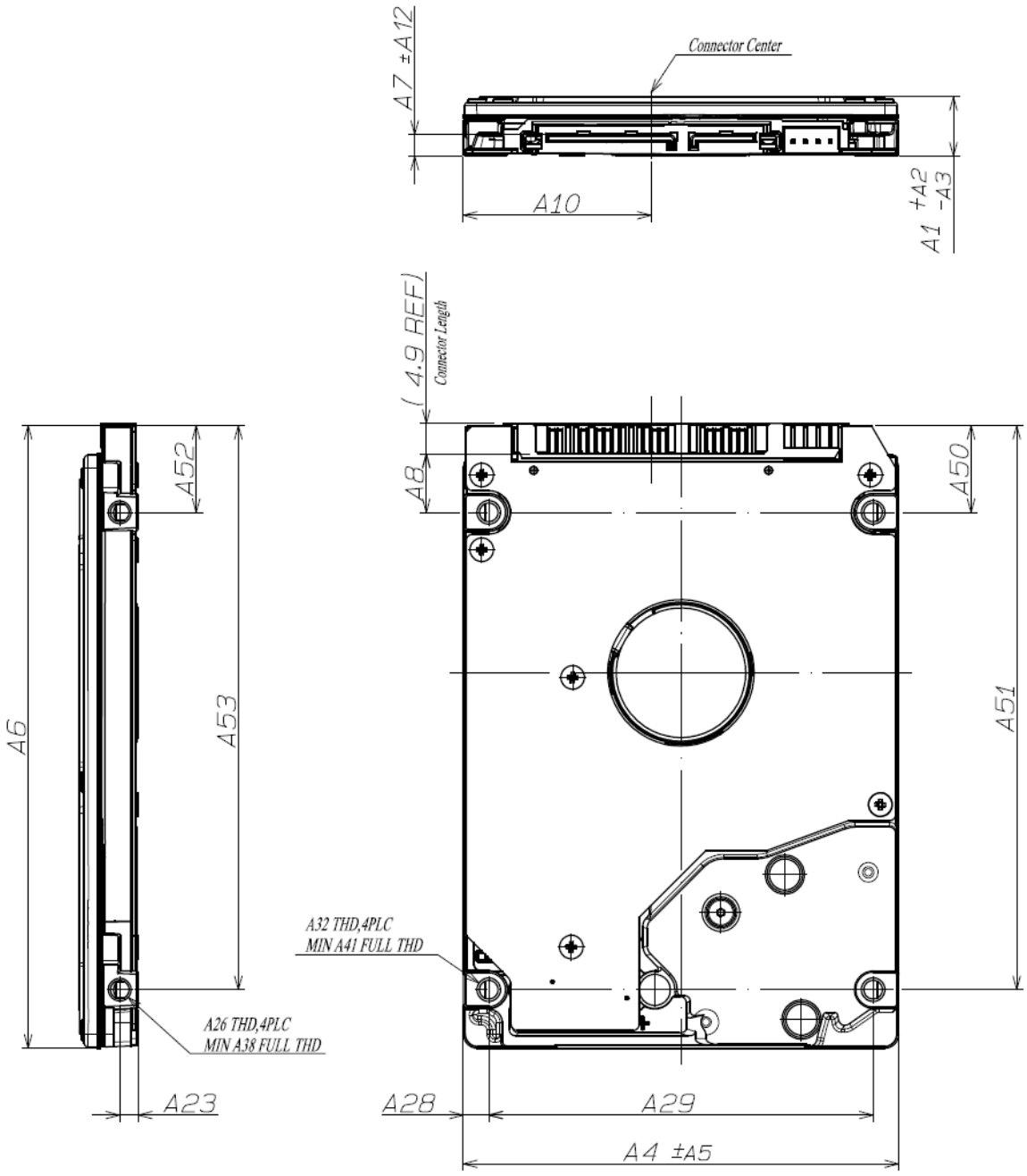


Figure 1 MK6476GSX Dimensions

Table 7.4-1 Dimensions

	SFF-8200 Rev2.0(*1) SFF-8201 Rev2.4 SFF-8223 Rev2.5		Toshiba S-ATA Model (Differences only)	
Dimension	Millimeters	Inches	Millimeters	Inches
A1	9.5	0.374		
A2	0.20	0.008		
A3	0.20	0.008		
A4	69.85	2.750		
A5	0.25	0.010		
A6(*2)	100.45 max	3.954 max	100.00 ±0.41	3.937 ±0.016
A7	3.50	0.137		
A8	9.40	0.370	9.40 ±0.51	0.370 ±0.020
A10(*3)	-	-	30.125 ±0.28	1.186 ±0.011
A12	0.38	0.015		
A23	3.00	0.118	3.00 ±0.20	0.118 ±0.007
A26	M3	N/A		
A28	4.07	0.160	4.07 +0.295 -0.305	0.160 +0.011 -0.012
A29	61.72	2.430	61.72 ±0.25	2.430 ±0.010
A32	M3	N/A		
A38	3.00 min	0.118 min	3.50 min	0.137 min
A41	2.50 min	0.980 min	3.50 min	0.137 min
A50(*2)	14.00	0.551	14.00 ±0.25	0.551 ±0.010
A51(*2)	90.60	3.567	90.60 ±0.30	3.567 ±0.012
A52(*2)	14.00	0.551	14.00 ±0.25	0.551 ±0.010
A53(*2)	90.60	3.567	90.60 ±0.30	3.567 ±0.012

(*1)SFF-8200:Small Form Factor Standard
(*2)PCA, Connector not included
(*3) ConnectorCenter defined the same as SFF-8223 A11

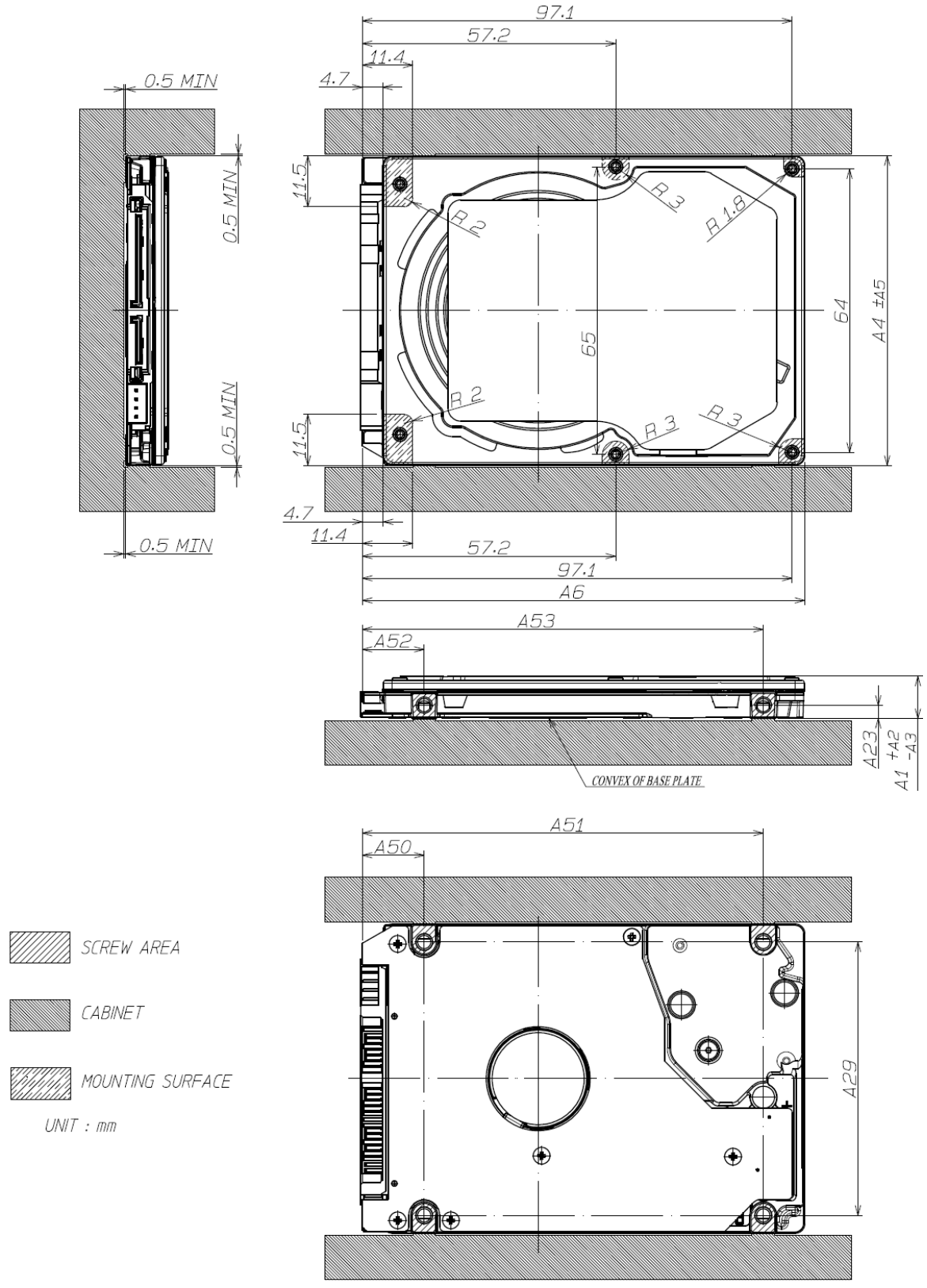
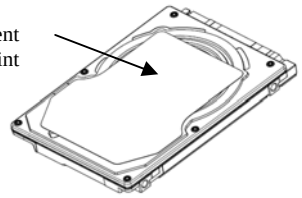


Figure 2 Mounting Recommendation

8. ENVIRONMENTAL LIMITS

8.1 Temperature and Humidity

8.1.1 Temperature

Operating	5^{o}C- 55^{o}C Gradient 20^{o}C / Hour maximum *) The temperature of top cover and base must be kept under 63℃ at any moment. Measurement point 
Non- operating	- 40^{o}C- 60^{o}C Gradient 20^{o}C / Hour maximum
Under shipment	- 40^{o}C- 70^{o}C Gradient 30^{o}C / Hour maximum (Packed in Toshiba's original shipping package)

8.1.2 Humidity

Operating	8%- 90% R.H. (No condensation)
Non- operating	8%- 90% R.H. (No condensation)
Under shipment	5%- 90% R.H. (Packed in Toshiba's original shipping package)
Max. wet bulb	29^{o}C (Operating) 40^{o}C (Non- operating)

8.2 Vibration

Operating	9.8 m/s^{2} (1.0G) 5- 500 Hz Sine wave sweeping 1 oct./ minute No unrecoverable error.
Non operating	10.0 mm p-p displacement. 5-15 Hz No unrecoverable error. 49 m/s^{2} (5.0G) 15- 500 Hz Sine wave sweeping 1 oct./ minute No unrecoverable error.

8.3 Shock

Operating	1,960 m/s^2 (200G) 1 msec half sine wave 3,920 m/s^2 (400G) 2 msec half sine wave Repeated twice maximum / second No unrecoverable error.
Non- operating	8,820 m/s^2 (900G) 1msec half sine wave 1,960 m/s^2 (200G) 11 msec half sine wave Repeated twice maximum / second No unrecoverable error.
Under shipment	70 cm free drop No unrecoverable error. Apply shocks in each direction of the drive's three mutually perpendicular axes, one axis at a time. (Packed in Toshiba's original shipping package)

8.4 Altitude

Operating	- 300 m to 3,000 m
Non operating	- 300 m to 12,000 m

8.5 Acoustics (Sound Power)

MK6476/5076GSX MK3276/2576/1676/1276GSX	25 dBA Average 19 dBA Average	For idle mode (Spindle in rotating)
MK6476/5076GSX MK3276/2576/1676/1276GSX	25 dBA Average 20 dBA Average	Randomly select a track to be sought in such a way that every track has equal probability of being selected. Seek rate(n_S) is defined by the following formula: $n_S = 0.4 / (t_T + t_L)$ t_T is published time to seek from one random track to another without including rotational latency; t_L is the time for the drive to rotate by half a revolution

Measurements are to be taken in accordance with ISO 7779.

8.6 Safety/EMI Standards

The drive satisfies the following standards.

	MK6476/5076/ 3276/2576/1676/1276GSX
Underwriters Laboratories(UL)	**UL 60950 Third Edition:2000**
Canadian Standard Association(CSA)	**CAN/CSA-C22.2 No.60950-01-03**
Technischer Uberwachungs-Verein(TUV)	**EN 60950-1:2001+A11**
Bureau of Standards, Metrology and Inspection (BSMI)	**CNS 13438 (CISPR Pub. 22 Class B):D33003**
Ministry of Information and Communication (KCC)	**電磁波障害防止基準　告示2004-23号 (CISPR Pub. 22 Class B) (Note1)**
Spectrum Management Agency (SMA)	**AS/NZS CISPR22**

(Note 1) Marks of KCC

	MK6476/5076/3276/2576/1676/1276GSX
Made in Japan	1. 기기의 명칭(모델명) : MK6476GSX 2. 인증번호 : TSD-MK6476GSX(B) 3. 인증받은 자의 상호 : TOSHIBA CORPORATION 4. 제조년월일 : 2010-09 5. 제조자 / 제조국가 : TOSHIBA CORPORATION / 일본
Made in Philippines	1. 기기의 명칭(모델명) : MK6476GSX 2. 인증번호 : TSD-MK6476GSX(B) 3. 인증받은 자의 상호 : TOSHIBA CORPORATION 4. 제조년월일 : 2010-09 5. 제조자 / 제조국가 : TOSHIBA CORPORATION / 필리핀
Made in China	1. 기기의 명칭(모델명) : MK6476GSX 2. 인증번호 : TSD-MK6476GSX(B) 3. 인증받은 자의 상호 : TOSHIBA CORPORATION 4. 제조년월일 : 2010-09 5. 제조자 / 제조국가 : TOSHIBA CORPORATION / 중국

8.7 EMC Adaptability

The drive satisfies the following standards.

	MK6476/5076/ 3276/2576/1676/1276GSX
EN55024	EN55022 with *
	EN61000-3-2 with *
	EN61000-3-3 with*
	EN61000-4-2 with *
	EN61000-4-3 with *
	EN61000-4-4 with *
	EN61000-4-5 with *
	EN61000-4-6 with *
	EN61000-4-11 with *
	ENV50204 with *

8.8 Magnetic Fields

The disk drive shall work without degradation of the soft error rate under the following Magnetic Flux Density Limits at the enclosure surface.

MK6476/5076/ 3276/2576/1676/1276GSX	1.5mT (15 Gauss)

9. RELIABILITY

A failure is defined as an inability of the drive to perform its specified function described in the requirements of this document when being operated under the normal conditions or conditions specified in this document. However, damages caused by operation mistake, mishandling, accidents, system errors and other damages that can be induced by the customers are not defined as failure.

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9.1 Error Rate

9.1.1 Non- Recoverable Error Rate

1 error per 10^{14} bits read

The defective sectors allocated to the spare locations in the factory are not counted in the error rate.

9.1.2 Seek Error Rate

1 error per 10^{6} seeks

A seek error is a positioning error recoverable by a retry including recalibration.

9.2 Mean Time to Failure (MTTF)

600,000 hours

A failure means that the drive can not execute the function defined in this document under the nominal temperature, humidity and the other conditions specified in this document . Damages caused by operation mistake, mishandling,system failure and other damages occurred under the conditions which are not described in this document are not considered as the failure.

- Power on hours (note1) : Less than 333 hours/month
- Operating (note2) : Less than 20% of power on hour
- Number of seek : 1.30 x 10^6 seeks / month
- Enviroment : Normal (25^{o}C, 101.3 kPa (1,013 mb))
- Do not apply electrical static discharge, vibration and shock to the drive.
- Do not press top cover and bottom PCBA surface of the drive.
- All others condition should be within specification show in section 6/7/8/9.

(note1) Power on hour includes sleep and standby mode.
(note2) Operating : seeking, writing and reading.

Applicable warranty and warranty period should be covered by the purchase agreement.

9.3 Product Life

Approximately 5 years or 20,000 power on hours whichever comes earlier under the following conditions.

- Power on hours (note1) : Less than 333 hours/month
- Operating (note2) : Less than 20% of power on hour
- Number of seek : 1.30 x 10^6 seeks / month
- Enviroment : Normal (25^{o}C, 101.3 kPa (1,013 mb))
- Do not apply electrical static discharge, vibration and shock to the drive.
- Do not press top cover and bottom PCBA surface of the drive.
- All others condition should be within specification show in section 6/7/8/9.

(note1) Power on hour includes sleep and standby mode.
(note2) Operating : seeking, writing and reading.

Applicable warranty and warranty period should be covered by the purchase agreement.

9.4 Repair

A defective drive should be replaced. Parts and subassemblies should not be repaired individually.

9.5 Preventive Maintenance (PM)

No preventive maintenance is required.

9.6 Load/Unload

Be sure to issue and complete the following commands for unloading before cutting off the power supply.
600,000 times of normal Load /Unload can be performed by a command and power management.
Unload is executed by the following commands:

- Standby
- Standby Immediate
- Sleep

Load/unload is also executed as one of the idle modes of the drive.

If power is removed from the drive while the heads are over the media an Emergency Unload will take place. An Emergency Unload is performed by routing the back-EMF of the spindle motor to the actuator voice coil. An Emergency Unload is mechanically much more stressful to this drive than a controlled Unload. The minimum number of Emergency Unloads that can be successfully performed is 20,000. Emergency Unload should only be performed when it is not possible to perform a controlled Unload.

9.7 Required power-off sequence

Required power-off sequence is as follows:

1. Issued one of the following commands.
   - Standby
   - Standby Immediate
   - Sleep

2. Wait until the command completion.

3. Turn off power to the drive.

10. HOST INTERFACE

Related Standards

Information technology - AT Attachment-3 Interface (ATA-3)
X3T10/2008D Revision 6 October 26, 1995

Information technology - AT Attachment with Packet Interface Extension (ATA -4)
T13/1153D Revision 17 October 30, 1997

Information technology - AT Attachment with Packet Interface-5 (ATA-5)
T13/1321D Revision 3 February 29, 2000

Information technology - AT Attachment with Packet Interface-6 (ATA-6)
T13/1410D Revision 3b February 26, 2002

Information technology - AT Attachment with Packet Interface-7 (ATA-7)
T13/1532D Volume 1 Revision 4b April 21, 2004

T13/1410D Volume 2 Revision 4b April 21, 2004

T13/1410D Volume 3 Revision 4b April 21, 2004

Information technology - AT Attachment 8 - ATA/ATAPI Command Set (ATA8-ACS)
T13/1699-D Revision 4b July 4, 2007

Serial ATA: High Speed Serialized AT Attachment
SerialATA Workgroup Revision 2.6

10.1 Cabling

10.1.1 Interface Connector

Drive side connector		DDK: SAT-PG22-S1A-FG
Recommended host side connector	for board	Right Angle Type : DDK SAT-RC22-S23-FG or equivalent
	for cable	DDK SAT-RG07-C2-FG or equivalent (for signal) (No recommendation now for power segment)

10.1.2 Cable

When connecting the drive and host system with Serial ATA cable, use of the Serial ATA 2.6 specification compliant cable is recommended.

10.2 Electrical specification

10.2.1 Physical Layer

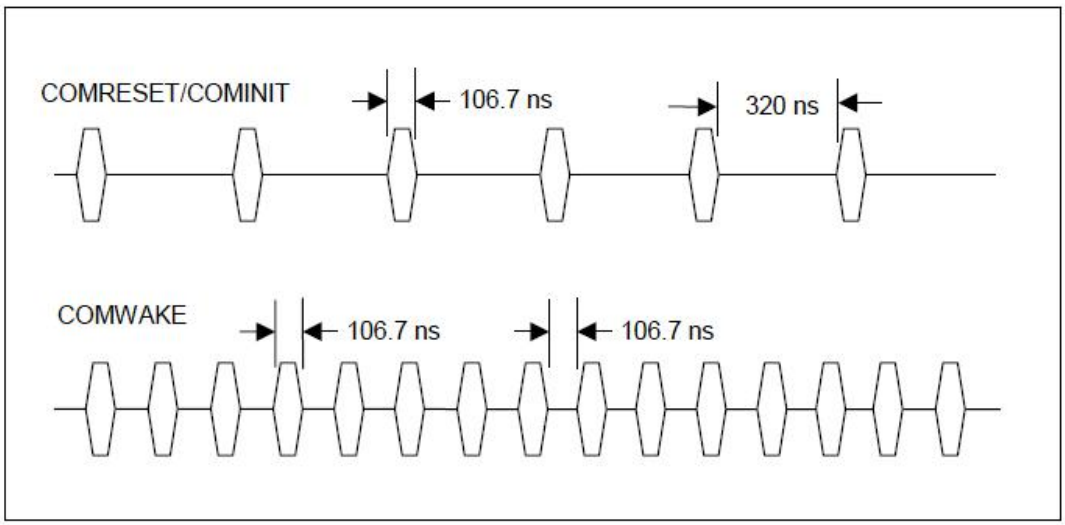
Table 10.2-1 Physical Layer parameters

Parameter	Min	Nom	Max	Units
Channel Speed		3.0		Gbps
Fbaud		3.0		GHz
FER, Frame Error Rate			8.2e-8 at 95% confidence level	
T_{UI}, Unit Interval	333.2167	333.3333	335.1167	Ps
f_{tol}, TX Frequency Long Term Stability	-350		+350	Ppm
f_{SSC}, Spread-Spectrum Modulation Frequency	30		33	kHz
SSC_{tol}, Spread-Spectrum Modulation Deviation	-5000		+0	Ppm
$C_{ac\ coupling}$, AC Coupling Capacitance			12	nF
V_{trans} , Sequencing Transient Voltage	-2.0		2.0	V
V_{thresh}, OOB Signal Detection Thresholod	75	125	200	mVppd
UI_{OOB}, UI During OOB Signaling	646.67	666.67	686.67	ps
COMINIT/COMRESET and COMWAKE Transmit Burst Length		160		UI_{OOB}
COMINIT/COMRESET Transmit Gap Length		480		UI_{OOB}
COMWAKE Transmit Gap Length		160		UI_{OOB}
COMWAKE Gap Detection Window (May detect)	55		175	ns
COMWAKE Gap Detection Window(Shall detect)	101.3		112	ns
COMWAKR Gap Detection Window(Shall not detect)	<55		>=175	ns
COMINIT/COMRESET Gap Detection Window (May detect)	175		525	ns
COMINIT/COMRESET Gap Detection Window (Shall detect)	304		336	ns
COMINIT/COMRESET Gap Detection Window (Shall not detect)	<175		>=525	ns

10.2.2 OOB signaling

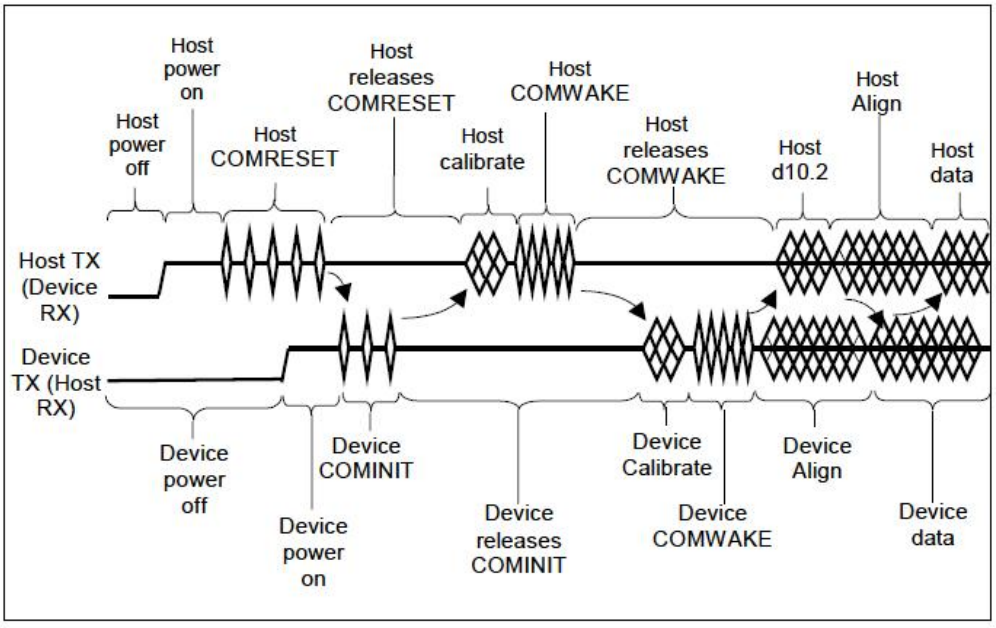
10.2.2.1 OOB signal spacing

There shall be three Out Of Band (OOB) signals used/detected by Phy, COMRESET, COMINIT and COMWAKE. When transmitting these signals, keep following spacing as follows.



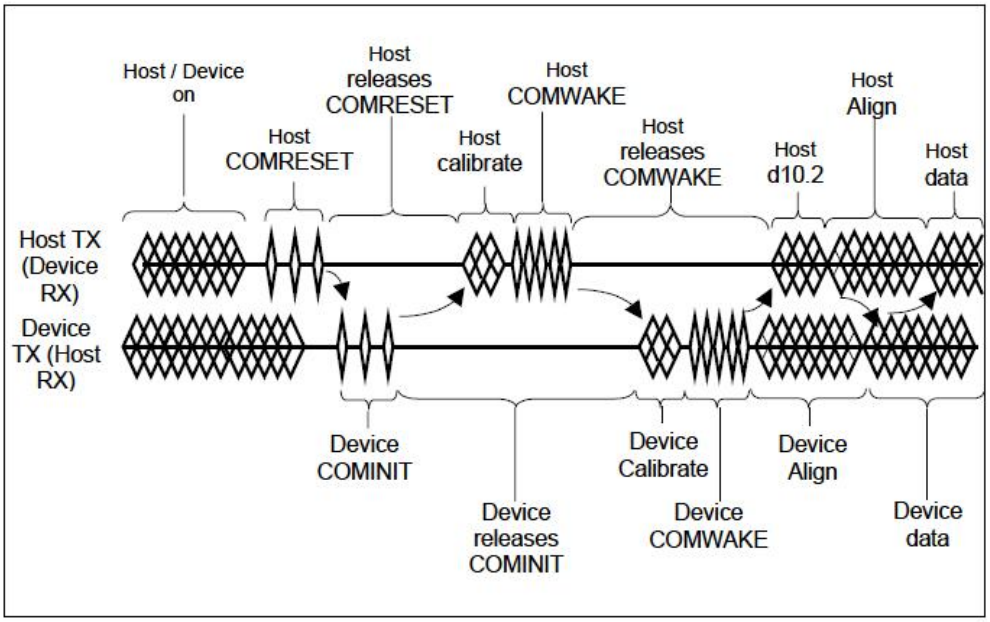
10.2.2.2 POWER ON sequence timing

Power-on sequence state diagram is follows.



10.2.2.3 COMRESET sequence timing

COMRESET sequence state diagram is follows.



10.2.2.4 Power Segment Pin 11

Pin 11 of the power segment of the drive connector has two functions One function is used by the drive to provide the host with an activity indication. Another function is used by the host to indicate whether staggered spin-up should be used. To accomplish both of these these goals, pin 11 acts as an input from the host to the drive prior to PhyRdy for “staggered spin-up control”. Also pin 11 acts as an output from the drive to the host after PhyRdy for activity indication. The activity indication provided by pin 11 is primaly for use in backplane application.

A host may only support one pin 11 feature, either receiving activity indication or “staggered spin-up disable control”. If a host supports receiving activity indication via pin 11, then the host shall not use pin 11 to disable staggered spin-up. If a host does not support receiving activity indication via pin 11, then the host may use pin 11 to disable staggered spin-up.

10.2.2.4.1 Activity signal

10.2.2.4.1.1 Activity Signal Electrical definition

The signal the drive provides for activity indication is a low-voltage low-current driver intended for efficient integration into current and future IC manufacturing processes. The signal is NOT suitable for directly driving an LED and must first be buffered using a circuit external to the drive before driving an LED.

Table 10.2-2 Drive connector pin 11 activity signal electrical parameters

Parameter	Min Value	Max Value	Description & Conditions
V_{Din}	-0.5V	2.1V	Tolerated input voltage
V_{Dact}	0mV	225mV	Drive output voltage when driving low under the condition I_D less than or equal to 300uA
V_{Dinact}	-0.1V	3.3V	Drive output voltage when not driving low
I_{Dinact}	-100uA	100uA	Drive leakage current when not driven

Table 10.2-3 Drive connector pin 11 Host activity signal electrical parameters

Parameter	Min Value	Max Value	Description & Conditions
V_{Hin}	-0.5V	3.3V	Tolerated input voltage
V_{HH}		2.1V	Host voltage presented to drive when drive not driving signal low.
V_{HL}	-0.1V		Minimum allowable host voltage that may be presented to the drive.
I_{HAct}		300uA	Host current delivered to drive when drive driving signal low. Value specified at V_{DAct} voltage of 0V.

10.2.2.4.2 Staggered Spin-up Disable Control

Before the drive spins up its media, drives that supported “staggered spin-up disable control” shall detect whether pin 11 is asserted low by the host. If pin 11 is asserted to low the drive shall disable staggered spin-up and immediately initiate media spin-up. If pin 11 is not connected in the host (floating), the drive that supported “staggered spin up disable” through pin 11 shall enable staggered spin-up.

Host staggered spin-up control electrical requirements

Table 10.2-4 Host staggered spin electrical parameters

Parameter	Min Value	Max Value	Description & Conditions
V_{HENB}	1.8V	V_{Hhmax}	Host voltage presented to drive to not disable staggered spin-up in drives that support staggered spin-up control. Value specified for all allowable I_{Dinact} leakage currents.
V_{Hdis}	-0.1V	225mV	Host voltage presented to drive to disable staggered spin-up in drives that support staggered spin-up control. Value specified for all allowable I_{Dinact} leakage currents.

If supported, the drive will sample the staggered spin-up disable condition after the DC power is applied and before PhyRdy is asserted.

10.3 Interface connector

10.3.1 Serial ATA interface connector

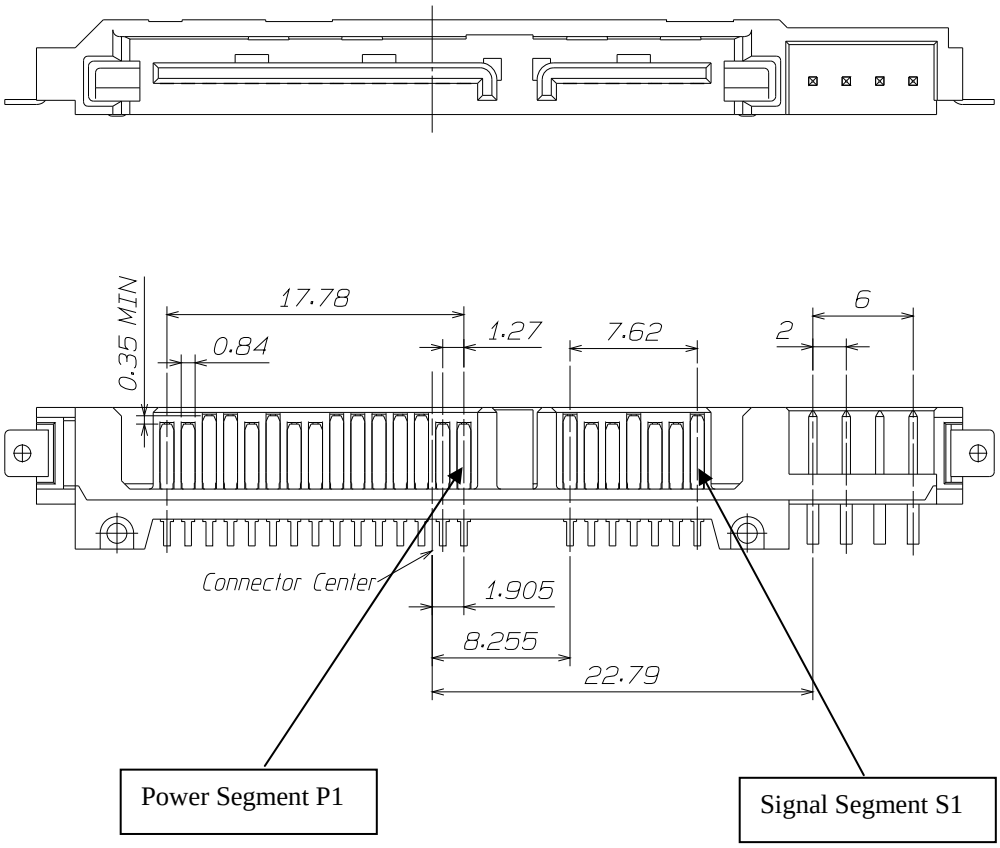


Figure 3 Serial ATA interface connector

10.3.2 Pin Assignment

The following table describes all of the pins on Serial ATA connector.

Table 10.3-1 Signal pin assignment

Signal segment key			
Signal segment	S1	GND	2nd mate
	S2	A+	Differential Pair A from PHY
	S3	A-	
	S4	GND	
	S5	B-	Differential Pair B from PHY
	S6	B+	
	S7	GND	2nd mate
Signal segment "L"			
Central connector polarizer			
Power segment "L"			
Power segment	P1	V33	3.3V power (Unused)
	P2	V33	3.3V power (Unused)
	P3	V33	3.3V power pre-charge 2nd mate (Unused)
	P4	GND	
	P5	GND	
	P6	GND	
	P7	V5	5V power pre-charge 2nd mate
	P8	V5	5V power
	P9	V5	5V power
	P10	GND	
	P11	ACT/ Spin	
	P12	GND	1st mate
	P13	V12	12V power pre-charge 2nd mate (Unused)
	P14	V12	12V power (Unused)
	P15	V12	12V power (Unused)
Power segment key			

Notice: This drive uses 5V power only. 3.3V and 12V power are not used.

10.4 Grounding

HDA (Head Disk Assembly) and DC ground(ground pins on interface) are connected electrically each other.

10.5 Frame Information Structure (FIS)

A FIS is a group of Dword that convey information between host and drive

10.5.1 Register – Host to Device (RegHD)

See Register Details 10.7

Table 10.5-1 Register – Host to Device layout (48bit LBA mode, EXT commands, NCQ commands)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features								Command								C	R	R	Reserved (0)					FIS Type (27h)							
1	Device								LBA High								LBA Mid								LBA Low							
2	Features (exp)								LBA High (exp)								LBA Mid (exp)								LBA Low (exp)							
3	Control								Reserved(0)								Sector Count (exp)								Sector Count							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Table 10.5-2 Register – Host to Device layout (CHS mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features								Command								C	R	R	Reserved (0)					FIS Type (27h)							
1	Device/Head								Cylinder High								Cylinder Low								Sector Number							
2	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							
3	Control								Reserved(0)								Reserved(0)								Sector Count							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Table 10.5-3 Register – Host to Device layout (28bit LBA mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Features								Command								C	R	R	Reserved (0)					FIS Type (27h)							
1	Device/LBA 27:24								LBA 23:16								LBA 15:8								LBA 7:0							
2	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							
3	Control								Reserved(0)								Reserved(0)								Sector Count							
4	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							

Field Name	Descriptions
FIS Type	Set a value of 27h
C	This bit is set to one when the register transfer is due to an update of the Command Register. The bit is set to zero when the register transfer is due to an update of the Device Control Register.
Command	Contains the contents of the Command register of the Shadow Command Block
Feature	Contains the contents of the Features register of the Shadow Command Block.
LBA Low	Contains the contents of the LBA Low register (48bit LBA addressing, EXP commands, NCQ commands), LBA 7:0 register (28 bit LBA addressing) or Sector Number register (CHS addressing)
LBA Mid	Contains the contents of the LBA Mid register (48bit LBA addressing, EXP commands, NCQ commands), LBA 15:8 register (28 bit LBA addressing) or Cylinder Low register (CHS addressing).
LBA High	Contains the contents of the LBA High register (48bit LBA addressing, EXP commands, NCQ commands), LBA 23:16 register (28 bit LBA addressing) or Cylinder High register (CHS addressing).
Device	Contains the contents of the Device register of the Shadow Command Block. Not used bit 4:0 for 48bit LBA addressing commands. Bit 4:0 used for LBA 27:24 for 28bit LBA addressing. Also used head number for CHS addressing.
LBA Low (exp)	Contains the contents of the expanded address field of the Shadow command Block. (48 bit LBA addressing, EXP commands, NCQ commands)
LBA Mid (exp)	Contains the contents of the expanded address field of the Shadow Command Block. (48 bit LBA addressing, EXP commands, NCQ commands)
LBA High(exp)	Contains the contents of the expanded address field of the Shadow Command Block. (48bit LBA addressing, EXP commands, NCQ commands)
Features (exp)	Contains the contents of the expanded Feature field of the Shadow Command Block.
Sector Count	Contains the contents of the Sector Count field of the Shadow Command Block. When the command is using 48bit LBA addressing, this value is the lower 8bit value for the number of sectors to be transferred. When the command is using 28bit LBA addressing or CHS addressing, this value is the number of the sectors to be transferred.
Sector Count (exp)	Contains the contents of the expanded Sector Count field of the Shadow Command Block.
Control	Contains the contents of the Device Control register of the Shadow Command Block.
R	Reserved

10.5.2 Register – Device to Host (RegDH)

See Register details 10.7

Table 10.5-4 Register – Device to Host layout (48bit LBA mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Error**								**Status**								**R**	**I**	**R**	**Reserved (0)**					**FIS Type (34h)**							
1	**Device**								**LBA High**								**LBA Mid**								**LBA Low**							
2	**Features (exp)**								**LBA High (exp)**								**LBA Mid (exp)**								**LBA Low (exp)**							
3	**Reserved (0)**								**Reserved(0)**								**Sector Count (exp)**								**Sector Count**							
4	**Reserved (0)**								**Reserved (0)**								**Reserved (0)**								**Reserved (0)**							

Table 10.5-5 Register – Device to Host layout (CHS mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Error**								**Status**								**R**	**I**	**R**	**Reserved (0)**					**FIS Type (34h)**							
1	**Device/Head**								**Cylinder High**								**Cylinder Low**								**Sector Number**							
2	**Reserved (0)**								**Reserved (0)**								**Reserved (0)**								**Reserved (0)**							
3	**Reserved (0)**								**Reserved(0)**								**Reserved(0)**								**Sector Count**							
4	**Reserved (0)**								**Reserved (0)**								**Reserved (0)**								**Reserved (0)**							

Table 10.5-6 Register – Device to Host layout (28bit LBA mode)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**Error**								**Status**								**R**	**I**	**R**	**Reserved (0)**					**FIS Type (34h)**							
1	**Device/LBA 27:24**								**LBA 23:16**								**LBA 15:8**								**LBA 7:0**							
2	**Reserved (0)**								**Reserved (0)**								**Reserved (0)**								**Reserved (0)**							
3	**Reserved (0)**								**Reserved(0)**								**Reserved(0)**								**Sector Count**							
4	**Reserved (0)**								**Reserved (0)**								**Reserved (0)**								**Reserved (0)**							

10.5.3 Data

Table 10.5-7 Data FIS Layout

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	N Dwords of data (minimum of one Dword – maximum of 2048 Dwords)																															
…																																
…																																
n																																

10.5.4 PIO Setup (PIOSU)

See Register details 10.7

Table 10.5-8 PIO Setup Layout(48bit LBA mode: Read/Write Sector EXT)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	R	Reserved (0)					FIS Type (5Fh)							
1	Device								LBA High								LBA Mid								LBA Low							
2	Reserved (0)								LBA High (exp)								LBA Mid (exp)								LBA Low (exp)							
3	E_STATUS								Reserved(0)								Sector Count (exp)								Sector Count							
4	Reserved (0)								Reserved (0)								Transfer Count															

Table 10.5-9 PIO Setup Layout (CHS Mode: Commands include PIO data transfer)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	R	Reserved (0)					FIS Type (5Fh)							
1	Device/Head								Cylinder High								Cylinder Low								Sector Number							
2	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							
3	E_status								Reserved(0)								Sector Count (exp)								Sector Count							
4	Reserved (0)								Reserved (0)								Transfer Count															

Table 10.5-10 PIO Setup Layout (28bit LBA mode: Read/Write Sector(s),i.e.)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								Status								R	I	R	Reserved (0)					FIS Type (5Fh)							
1	Device/LBA 27:24								LBA 23:16								LBA 15:8								LBA 7:0							
2	Reserved (0)								Reserved (0)								Reserved (0)								Reserved (0)							
3	E_Status								Reserved(0)								Reserved(0)								Sector Count							
4	Reserved (0)								Reserved (0)								Transfer Count															

10.5.5 DMA Activate (DMACT)

Table 10.5-11 DMA Activate Layout (Write DMA/Write DMA Queued/Service (Drive to Host))

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Reserved (0)								R	R	R	Reserved (0)					FIS Type (39h)							

10.5.6 DMA Setup (DMASU)

Table 10.5-12 DMA Setup Layout (NCQ, Read/Write FpDMA Queued)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved (0)								Reserved (0)								A	I	D	Reserved (0)					FIS Type (41h)							
1	0																											TAG				
2	0																															
3	Reserved (0)																															
4	DMA Buffer Offset																															
5	DMA Transfer Count																															
6	Reserved (0)																															

10.5.7 Set Device Bits (SDB)

Table 10.5-13 Set Device Bits Layout (NCQ, Result of Read/Write FpDMA Queued commands)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Error								R	Status Hi			R	Status Lo			N	I	R	Reserved (0)					FIS Type (A1h)							
1	SActive 31:0																															

10.5.8 Shadow Register Block Registers, Control Block Registers

Shadow Register Block Registers are interface registers used for delivering commands to the drive or posting status from the drive.

Table 10.5-14 Shadow Register Block registers

Command Block Registers			
READ		WRITE	
Data		Data	
Error		Features(exp)	Features
Sector Count (exp)	Sector count	Sector Count(exp)	Sector count
LBA Low(exp)	Sector number / LBA bit 0- 7/LBA Low	LBA Low(exp)	Sector number / LBA bit0-7/LBA Low
LBA Mid(exp)	Cylinder low / LBA bit 8-15/LBA Mid	LBA Mid(exp)	Cylinder low / LBA bit8-15
LBA High(exp)	Cylinder high / LBA bit16- 23/ LBA High	LBA High(exp)	Cylinder high / LBA bit16-23 / LBA High
Device head register / LBA bit 24- 27		Device head register / LBA bit 24-27	
Status		Command	
Alternate Status		Device control	

10.6 Shadow Register Block registers Description

In the following register descriptions, unused write bit should be treated as “don't care”, and unused read bits should be read as zeros.

10.6.1 Error Register

	RegH2D	RegD2H	PIO SU
FIS bit position	None	Dword 0: 31:24	Dword 0 : 31:24

10.6.1.1 Operational Mode

The following descriptions are bit definitions for the operational mode including the error information from the last command. This command is valid only when the ERROR BIT (bit 0) is set.

ICRC	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7	Interface CRC error was found during the transfer of DMA commands [1]
Bit 6	**UNC** (Uncorrectable Data Error) – This bit indicates that an uncorrectable error has been encountered in the data field during a read command.
Bit 5	Reserved (No specification for fixed drive)
Bit 4	**IDNF** (ID Not Found) –The requested sector could not be found.
Bit 3	Reserved (No specification for fixed drive)
Bit 2	**ABRT** (Aborted Command) -- This bit Indicates that the requested command has been aborted due to the reason reported in the drive status register (Write Fault, Not Seek Complete, Drive Not Ready, or an invalid command). The status registers and the error registers may be decoded to identify the cause.
Bit 1	Reserved (No specification for fixed drive)
Bit 0	**AMNF** (AM Not Found) -- This bit is set to indicate that the required Data AM pattern on read operation has not been found.

[1] ATA-2 Notes: Prior to the development of ATA-2 standard**,** this bit was defined as BBK (Bad Block Detected) -- This bit was used to indicate that the block mark was detected in the target’s ID field. The mark does not exist when shipping from the factory.The Mark will be written by FORMAT command. Read or Write commands will not be executed in any data fields marked bad. The drive does not support this bit.

10.6.1.2 Diagnostic Mode

The drive enters diagnostic mode immediately after the power -on or after an Execute Diagnostics command. Error bit in Status Register shall not be set in these cases. The following table shows bit values for the diagnostic mode.

Table 10.6-1 Diagnostic mode error register

01	No errors
02	Controller register error
03	Buffer RAM error
04	ECC device error
05	CPU ROM/RAM error
06-7F	Reserved
8x	Reserved

10.6.2 Features Register (Write Precompensation Register)

	RegH2D
FIS bit position	Dword 0 31:24

Write precompensation is automatically optimized by the drive internally. This register is used with Set Features command.

10.6.2.1 Smart command

This command is used with the Smart commands to select subcommands.

10.6.3 Features Exp Register

	RegH2D
FIS bit position	Dword 2 : 31:24

Features Exp register is optional register for 48bit LBA addressing mode.

10.6.4 Sector Count Register

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 3: 7:0	Dword 3: 7:0	Dword 3: 7:0

10.6.4.1 Disk Access command

The Sector Count register determines the number of sectors to be read or written for Read, Write, and Verify commands. A 0 in the Sector Count register specifies a 256 sector transfer. After normal completion of a command, the content shall be 0.

During a multi-sector operation, the sector count is decremented and the sector number is incremented. If an error should occur during multi-sector operation, this command shows the number of remaining sectors in order to avoid duplicated transfer.

For exp commands, the Sector Count register determines the lower 8bit number of sectors to be read or written for Read Sector Exp, Write Sector EXP, Read Sector Exp, Write Sector Exp, Read Verify EXP, Read FpDMA Queued and Write FpDMA Queued commands.

10.6.4.2 Initialize Device Parameters command

This register determines number of sectors per track.

10.6.4.3 Power Control command

This register returns a value in accordance with the operation mode (idle mode or stand-by mode).

10.6.4.4 Set Features Command

If features register for this command is 03h, this register sets the data transfer mode.

10.6.5 Sector Count EXP Register

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 3: 15:8	Dword 3: 15:8	Dword 3: 15:8

10.6.5.1 Disk Access command

The Sector Count exp register determines the number of sectors to be read or written for Read, Write, Verify EXP, Read FpDMA Queued and Write FpDMA Queued commands. In these cases, the numbers of sectors to be read or write described in the Sector Count EXP register and Sector Count register. The Sector Count register describe the higher part of the 16bit. As a result a 0 in the Sector Count register and the Sector Count EXP register specifies a 65536 sector transfer. After normal completion of a command, the content shall be 0.

During a multi-sector operation, the sector count is decremented and the sector number is incremented. If an error should occur during multi-sector operation, this command shows the number of remaining sectors in order to avoid duplicated transfer.

10.6.6 Sector Number (LBA low, LBA7:0) Register

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 1: 7:0	Dword 1: 7:0	Dword 1: 7:0

The target logical sector number (starting from 1) for Read, Write, and Verify commands is set in this register. After completion of a command, it shows the sector number of the last sector transferred to the host.

The starting sector number is set in this register for multi-sector operations. But when error occurs during multi-sector transfer, it shows the number of the sector in which the error has been detected. During multi-sector transfer, the number of the next sector to be transferred will not necessarily be shown.

In LBA mode, this register contains Bits 0 - 7 logical block address. After completion of a command, the register is updated to reflect the current LBA Bits.

10.6.7 Cylinder Low (LBA Middle, LBA 23:16) Registers

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 1: 15:8	Dword 1: 15:8	Dword 1: 15:8

10.6.7.1 Disk Access command

Lower 8 bits of the starting cylinder number (starting from 0) for Read, Write, Seek, and Verify commands are contained in these registers. After completion of the command or sector transfer, the current cylinder is shown in this register.

In LBA mode, Bits 8 - 15 of the target address in logical block address are set in this register. After completion of a command, the register is updated to reflect the current LBA Bits 0 - 7.

10.6.7.2 SMART commands

This register should be set to 4Fh for SMART commands

10.6.8 Cylinder High (LBA High, LBA 23:16) Registers

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 1: 15:8	Dword 1: 15:8	Dword 1: 15:8

10.6.8.1 Disk Access command

The high order bits of the starting cylinder number (starting from 0) for Read, Write, Seek, and Verify commands are set in this register. After completion of the command or sector transfer, the current cylinder is shown in this register.

In LBA mode, Bits 16 - 23 of the target address in logical block address are contained in this register. After completion of the command, it shows the Bits 0 - 7 of the last logical block address.

	Cylinder High	Cylinder Low
Register Bits	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Cylinder Bits	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0

10.6.8.2 SMART commands

This register should be set to C2h for SMART commands

10.6.9 Device/Head Register

	RegH2D	RegD2H	PIO SU
FIS bit position	Dword 1: 31:24	Dword 1: 31:24	Dword 1: 31:24

The value of this register is used to select the drive, Drive0 or Drive1, and head. On multiple sector read/write operation that requires to cross track boundaries, the head select bit will be updated to reflect the currently selected head number.

1	L	1	DEV	HS3	HS2	HS1	HS0

Bit 7	Reserved (recommended to set 1)
Bit 6	**L** (Select LBA mode) L=0: CHS mode. L=1: LBA mode.
Bit 5	Reserved (recommended to set 1)
Bit 4	**DEV** (Device Select): - (Drive0/Drive1 mode) This bit is used to select the drive. DEV= 0 indicates the first fixed disk drive (Drive0), and DEV= 1 indicates the second (Drive1). - (Single mode) should be 0. If this is 1, a drive is not selected but 00h shall be returned to status register.
Bit 3 - Bit 0	**HS3-HS0** (Head Select Bits) -- Bits 3 through 0 determine the required read/write head. Bit 0 is the least-significant bit. If the L bit is equal to one (LBA Mode), the HS3 through HS0 bits contain bits 27 through 24 of the LBA except “EXP” commands.

10.6.10 Status Register

	RegD2H	PIO SU	SDB
FIS bit position	Dword 0: 23:16	Dword 0: 23:16	Dword 0: 23:16

This register contains the command status. The contents of the register are updated at the completion of each command and whenever the error occurs. The host system reads this register in order to acknowledge the status and the result of each operation.

When the BSY bit (bit 7) is set, no other bits in the register are valid. And read/write operations of any other register are negated in order to avoid the returning of the contents of this register instead of the other resisters' contents.

If the host reads this register when an interrupt is pending, interrupt request (INTRQ) is cleared in order to work as Interrupt Acknowledge.

The bits of the status register are defined as below:

BSY	DRDY	DF	DSC[3]	DRQ	0	0	ERR

Bit 7	**BSY** (Busy) -- This bit is set when Host Reset (HRST) line is activated or Software Reset (SRST) bit in Device Control register is set or when the COMMAND register is written and until a command is completed but when Data Request is set to 1, this bit shall be reset. The host shouldn't write or read any registers when BSY = 1.
Bit 6	**DRDY** (Drive ready) -- DRDY=1 when seek complete bit (bit 4) = 1, indicates that the drive is ready to respond read, write, or seek command. DRDY=0 indicates that read, write and seek are negated. A command execution shall be interrupted if Not-Ready condition occurs during a command execution and will be reset until the next command whether the drive condition is Ready or Not Ready. Error bit is set on this occasion and will be reset just after power on and set again after the drive begins revolving at normal speed and gets ready to receive a command.
Bit 5	**DF** (Device Fault) -- DF=1 indicates that the drive has detected a fault condition during the execution of a Read Write commands; read, write, and seek commands are negated and Error bit is set. DF is set to 1 until the next command, whether the drive is in fault condition or not.
Bit 4	**DSC[2]** (Drive Seek Complete) – DSC³= 1 indicates that a seek operation has been completed. DSC³ is set to 0 when a command accompanied by a seek operation begins. If a seek is not complete, a command is terminated and this bit is not changed until the Status Register is read by the host. This bit remains reset immediately after power on until the drive starts revolving at a nominal speed and gets ready to receive command.
Bit 3	**DRQ** (Data Request) -- DRQ=1 indicates that the sector buffer requires 1 sector of data during a Read or Write command.
Bit 2	Reserved
Bit 1	Reserved
Bit 0	**ERR** (Error) -- ERR = 1 indicates that an error occurred during execution of the previous command. The cause of the error is reported on the other bit or in the error register. The error bit can be reset by the next command from the controller. When this bit is set, a multi-sector operation is negated.

[2] ATA-2 Notes: Prior to ATA-2 standard, this bit indicated that the device was on track. This bit may be used for other purposes in future standards. For compatibility the drive supports this bit as ATA-1 specifies. User is recommended not to use this bit.

10.6.11 Command Register

	RegH2D
FIS bit position	Dword 1: 23:16

The command register accepts commands for the drive to perform fixed disk operations. Commands are executed when the Shadow Block Registers are loaded and the command register is written and only when:

The status is not busy (BSY is inactive).
and
DRDY (drive ready) is active.

Any code NOT defined in the following list causes an Aborted Command error. Interrupt request (INTRQ) is reset when a command is written. The following are acceptable commands to the command register.

Table 10.6-2 Command Code

Command Code								
Command Name		Hex Value	PARAMETERS USED					
			SC	SN	CY	DRV	HD	FT
Nop		00H	X	X	X	O	X	X
Recalibrate		1xH	X	X	X	O	X	X
Read Sector(s)		20/21H	O	O	O	O	O	X
Read Sector(s) EXT		24h	O	O	O	O	O	X
Read DMA EXT		25H	O	O	O	O	O	X
Read Native Max Address EXT		27H	X	X	X	O	X	X
Read Multiple EXT		29H	O	O	O	O	O	X
Read Log EXT		2FH	O	O	O	O	X	X
Write Sector(s)		30/31H	O	O	O	O	O	X
Write Sector(s) EXT		34H	O	O	O	O	O	X
Write DMA EXT		35H	O	O	O	O	O	X
Set Max Address EXT		37H	O	O	O	O	O	X
Write Multiple EXT		39H	O	O	O	O	O	X
Write Verify		3CH	O	O	O	O	O	X
Write DMA FUA EXT		3DH	O	O	O	O	O	X
Write Log EXT		3FH	O	O	O	O	X	X
Read Verify Sector(s)		40/41H	O	O	O	O	O	X
Read Verify Sector(s) EXT		42H	O	O	O	O	O	X
Read Log DMA EXT		47h	O	O	O	O	X	X
Write Log DMA EXT		57h	O	O	O	O	X	X
Read FPDMA Queued		60H	O	O	O	O	O	O
Write FPDMA Queued		61H	O	O	O	O	O	O
Seek		7xH	X	O	O	O	O	X
Execute Diagnostics		90H	X	X	X	O	X	X
Initialize Device Parameters		91H	O	X	X	O	O	X
Download Microcode		92H	O	O	O	O	X	O
SMART		B0H	O	O	O	O	X	O
Device Configuration		B1H	X	X	X	O	X	O
Read Multiple		C4H	O	O	O	O	O	X
Write Multiple		C5H	O	O	O	O	O	X
Set Multiple Mode		C6H	O	X	X	O	X	X
Read DMA		C8/C9H	O	O	O	O	O	X
Write DMA		CA/CBH	O	O	O	O	O	X
Write Multiple FUA EXT		CEH	O	O	O	O	O	X
Power Control	Stand-by Immediate	E0 / 94H	O	X	X	O	X	X
	Idle Immediate	E1 / 95H	O	O	O	O	X	O
	Stand-by	E2 / 96H	O	X	X	O	X	X
	Idle	E3 / 97H	O	X	X	O	X	X
	Check Power Mode	E5 / 98H	O	X	X	O	X	X
	Sleep	E6 / 99H	O	X	X	O	X	X
Read Buffer		E4H	X	X	X	O	X	X
Flush Cache		E7H	X	X	X	O	X	X
Write Buffer		E8H	X	X	X	O	X	X
Flush Cache EXT		EAH	X	X	X	O	X	X
Identify Device		ECH	X	X	X	O	X	X
Set Features		EFH	X	X	X	O	X	O
Security	Set Password	F1H	X	X	X	O	X	X
	Unlock	F2H	X	X	X	O	X	X
	Erase Prepare	F3H	X	X	X	O	X	X
	Erase Unit	F4H	X	X	X	O	X	X
	Freeze	F5H	X	X	X	O	X	X
	Disable Password	F6H	X	X	X	O	X	X
Read Native Max Address		F8H	X	X	X	O	X	X
Set Max		F9H	O	O	O	O	O	X

Note: O and X are defined as follows.
O = Must contain valid information for this command.
X = Don't care for this command.

Parameters are defined as follows.

SC = SECTOR COUNT register.
SN = SECTOR NUMBER register.
CY = CYLINDER LOW and CYLINDER HIGH register.
DRV = DRIVE SELECT bit (bit 4 in DRIVE/HEAD register)
HD = HEAD SELECT bits (bit 3-0 in DRIVE/HEAD register)
FT = FEATURES register (WRITE PRECOMPENSATION register)

10.6.12 Device Control Register

	RegH2D
FIS bit position	Dword 3: 31:24

This register contains the following three control bits.

HOB	----	----	----	1	SRST	- IEN	----

Bit 7	**HOB** (High Order Byte) is defined by the 48-bit Address feature set. A write to any Command register shall clear the HOB bit to zero.
Bit 6-4	not used
Bit 3	Reserved (recommended to set 1)
Bit 2	**SRST** (Soft Reset) -- SRST= 1 indicates that the drive is held reset and sets BSY bit in Status register. All internal registers are reset as shown in Table 10.13-1 . If two drives are daisy chained on the interface, this bit will reset both drives simultaneously, regardless of the selection by Device address bit in DEVICE/HEAD register.
Bit 1	**- IEN** (Interrupt Enable) -- When -IEN = 0, and the drive is selected by Drive select bit in DEVICE/HEAD register, the drive interrupt to the host is enabled. When this bit is set, the “I” bit in the RegH2D, PIOSU, SDB and DMASU will be set, whether a pending interrupt is found or not.
Bit 0	not used

To change these register bits, C bit of RegH2D should be set.

10.7 Command Descriptions

The drive interprets the commands written in the command register by the host system and executes them. This table shows the drive's response to the valid commands written in command-register.

Command	Status register				Error register					
	DRDY	DF	CORR	ERR	ICRC	UNC	IDNF	ABRT	TK0NF	AMNF
CHECK POWER MODE	√	√		√				√		
EXECUTE DEVICE DIAGNOSTIC	√	√		√	See Table 10.6-1					
DEVICE CONFIGRATION RESTORE	√	√		√				√		
DEVICE CONFIGRATION FRESZE LOCK	√	√		√				√		
DEVICE CONFIGRATION IDENTIFY	√	√		√				√		
DEVICE CONFIGRATION SET	√	√		√				√		
DOWNLOAD MICROCODE	√	√		√				√		
FLUSH CACHE (EXT)	√	√		√			√	√		
IDENTIFY DEVICE	√	√		√				√		
IDLE	√	√		√				√		
IDLE IMMEDIATE	√	√		√				√		
INITIALIZE DEVICE PARAMETERS	√	√								
READ BUFFER	√	√		√				√		
READ DMA (EXT)	√	√		√	√	√	√	√		√
READ MULTIPLE (EXT)	√	√		√		√	√	√		√
READ NATIVE MAX ADDRESS (EXT)	√			√						
READ SECTOR(S) (EXT)	√	√		√		√	√	√		√
READ VERIFY SECTOR(S) (EXT)	√	√		√		√	√	√		√
READ FPDMA QUEUED	√	√		√	√	√	√	√		√
READ LOG EXT	√	√		√		√	√	√		√
READ LOG DMA EXT	√	√		√		√	√	√		√
RECALIBRATE	√	√		√				√	√	
SECURITY DISABLE PASSWORD	√	√		√				√		
SECURITY ERASE PREPARE	√	√		√				√		
SECURITY ERASE UNIT	√	√		√				√		
SECURITY FREEZE LOCK	√	√		√				√		
SECURITY SET PASSWORD	√	√		√				√		
SECURITY UNLOCK	√	√		√				√		
SEEK	√	√		√			√	√		
SET FEATURES	√	√		√				√		
SET MAX ADDRESS (EXT)	√			√			√	√		
SET MAX SET PASSWORD	√			√				√		
SET MAX LOCK	√			√				√		
SET MAX UNLOCK	√			√				√		
SET MAX FLEEZE LOCK	√			√				√		
SET MULTIPLE MODE	√	√		√				√		
SLEEP	√	√		√				√		
SMART Enable/Disable Attribute autosave	√	√		√				√		
SMART Enable/Disable Automatic Off-line	√	√		√				√		
SMART DISABLE OPERATIONS	√	√		√				√		
SMART ENABLE OPERATIONS	√	√		√				√		
SMART RETURN STATUS	√	√		√				√		
SMART Read Attribute Values	√	√		√		√	√	√		
SMART Read Attribute Thresholds	√	√		√				√		
SMART Save Attribute Values	√	√		√				√		
SMART Execute OFF-LINE Immediate	√	√		√			√	√		
SMART Read Log Sector	√	√		√		√	√	√		
SMART Write Log Sector	√	√		√			√	√		
STANDBY	√	√		√				√		
STANDBY IMMEDIATE	√	√		√				√		
WRITE BUFFER	√	√		√				√		
WRITE DMA (EXT)	√	√		√	√		√	√		

Command	Status register				Error register					
	DRDY	DF	CORR	ERR	ICRC	UNC	IDNF	ABRT	TK0NF	AMNF
WRITE DMA FUA EXT	√	√		√	√		√	√		
WRITE MULTIPLE (EXT)	√	√		√			√	√		
WRITE MULTIPLE FUA EXT	√	√		√			√	√		
WRITE SECTOR(S) (EXT)	√	√		√			√	√		
WRITE VERIFY	√	√		√			√	√		
WRITE FPDMA QUEUED	√	√		√	√		√	√		
WRITE LOG EXT	√	√		√			√	√		
WRITE LOG DMA EXT	√	√		√			√	√		
Invalid command code	√	√		√				√		

√ = valid on this command

10.7.1 Nop (00h)

COMMAND CODE	0 0 0 0 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	Reserved	na
LBA	na	na

The Nop command reports the status. The drive terminates the command with aborted error after receiving this command.

10.7.2 Recalibrate[3] (1xh)

COMMAND CODE	0 0 0 1 X X X X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY		na
HD		na
SN		na
SC		na
FT		na
LBA		na

This command will set BSY bit and move the R/W heads on the disk to cylinder 0. At the completion of a seek , it revises the status, resets BSY and generates an interrupt.

10.7.3 Flush Cache (E7h)

COMMAND CODE		1 1 1 0 0 1 1 1
RESISTER SETTING	DR	drive no.

This command reports the completion of a Write cache to the host. At the completion of a Write cache, the drive revises the status, resets BSY and generates an interrupt.

10.7.4 Flush Cache EXT (EAh)

COMMAND CODE		1 1 1 0 1 0 1 0
RESISTER SETTING	DR	drive no.

This command reports the completion of a Write cache to the host. At the completion of a Write cache, the drive revises the status, resets BSY and generates an interrupt.

[3] ATA/ATAPI-4 defines this command as Vendor specific. The drive supports this command to maintain ATA-3, and the previous models compatibility. User is recommended not to use this command.

10.7.5 Read Sector (20h/21h)

COMMAND CODE	0 0 1 0 0 0 0 X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to read	na
FT	na	na
LBA	staring address	na

Setting BSY bit, the drive will seek to the target cylinder if the head is not on target track (implied seek), select the head and begin to read the number of sector defined in SC register (1-256) starting from the target sector. After finding ID of target sector and having 1 sector of data read into the buffer RAM, the drive sets DRQ in status register and generates interrupt to report to the host that the drive is ready to transfer the next data.

In case of multi-sector transfer, DRQ bit is reset and BSY is set after 1 sector transfer to prepare for the next sector transfer.

An uncorrectable data can also be transferred but the subsequent operation will terminate at the cylinder, head, and sector (or LBA) position in the Shadow Block register. When a sector is ready to be read by the host, an interrupt is issued. After the last sector is read by the host, no interrupt is issued at the end of a command.

10.7.6 Read Sector EXT (24h)

COMMAND CODE	0 0 1 0 0 1 0 0	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

Setting BSY bit, the drive will seek to the target cylinder if the head is not on target track (implied seek), select the head and begin to read the number of sector defined in SC register (1-65536) starting from the target sector. After finding ID of target sector and having 1 sector of data read into the buffer RAM, the drive sets DRQ in status register and generates interrupt to report to the host that the drive is ready to transfer the next data.

In case of multi-sector transfer, DRQ bit is reset and BSY is set after 1 sector transfer to prepare for the next sector transfer.

An uncorrectable data can also be transferred but the subsequent operation will terminate at the LBA position in the Shadow Register Block registers. When a sector is ready to be read by the host, an interrupt is issued. After the last sector is read by the host, no interrupt is issued at the end of a command.

This command is available in LBA addressing only.

10.7.7 Write Sector (30h/31h)

COMMAND CODE	0 0 1 1 0 0 0 X	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to write	na
FT	na	na
LBA	starting address	na

The drive seeks to the target cylinder and selects the head and begins to write to the number of sectors defined in SC register (1-256) starting from the target sector. DRQ in status register is set as soon as the command register is written and the buffer RAM receives the data transferred from the host. After 1 sector is transferred to the buffer RAM, the drive resets DRQ, sets BSY and begins write operation. In case of multi-sector transfer, it sets DRQ bit, resets BSY and generates Interrupt to inform host that it is ready to transfer the next 1 sector of data. The drive will seek to the target cylinder if the head is not on the target track (implied seek). After transferring the last data in the buffer, it resets BSY and issues an interrupt.

If an error occurs during multi-sector transfer, it will terminate the transfer by setting error information in status register and error register, without shifting into data transfer mode from the host. CY, HD, SN (LBA) registers show the address where error has occurred.

10.7.8 Write Sector EXT (34h)

COMMAND CODE	0 0 1 1 0 1 0 0	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

The drive seeks to the target cylinder and selects the head and begins to write to the number of sectors defined in SC register (1-65536) starting from the target sector. DRQ in status register is set as soon as the command register is written and the buffer RAM receives the data transferred from the host. After 1 sector is transferred to the buffer RAM, the drive resets DRQ, sets BSY and begins write operation. In case of multi-sector transfer, it sets DRQ bit, resets BSY and generates Interrupt to inform host that it is ready to transfer the next 1 sector of data. The drive will seek to the target cylinder if the head is not on the target track (implied seek). After transferring the last data in the buffer, it resets BSY and issues an interrupt.

If an error occurs during multi-sector transfer, it will terminate the transfer by setting error information in status register and error register, without shifting into data transfer mode from the host. LBA registers show the address where error has occurred.

This command is available in LBA addressing only.

10.7.9 Read Verify (40h/41h)

COMMAND CODE	0 1 0 0 0 0 0 X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to be read	na
LBA	starting address	na

This command is identical to a Read command except that the drive has read the data from the media, and the DRQ bit is not set and no data is sent to the host. This allows the system to verify the integrity of the drive. A single interrupt is generated upon completion of a command or when an error occurs.

10.7.10 Read Verify EXT (42h)

COMMAND CODE	0 1 0 0 0 0 1 0	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command is identical to a Read EXT command except that the drive has read the data from the media, and the DRQ bit is not set and no data is sent to the host. This allows the system to verify the integrity of the drive. A single interrupt is generated upon completion of a command or when an error occurs.

This command is available in LBA addressing only.

10.7.11 Write Verify[4] (3Ch)

COMMAND CODE	0 0 1 1 1 1 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to be written	na
LBA	starting address	na

[4] ATA/ATAPI-4 defines this command as Vendor specific. The drive supports this command to maintain ATA-3 compatibility. User is recommended not to use this command.

This command is all identical to a Write sector command. Read verification is not performed in this command. A Write verify command transfers the number of sectors (1-256) defined in SC register from the host to the drive, then the data is written on the media. The starting sector is defined in CY, HD, SN (LBA) registers.

Upon receipt of the command, the drive sets DRQ until one sector of data is transferred from the host, then resets DRQ, sets BSY. In case of multi- sector transfer, it sets DRQ, resets BSY and generates an interrupt to report the host that the host is ready to receive 1 sector of data. The drive will seek to the target track if the R/W head is not on the target track (implied seek). Reaching the target sector, the command transfers the sector data from the host to the media. After transferring the last data in the buffer, it sets BSY and issues an Interrupt.

10.7.12 Seek (7xh)

COMMAND CODE	0 1 1 1 X X X X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	cylinder to seek	na
HD	head to seek	na
SN	sector to seek	na
SC	na	na
FT	na	na
LBA	address to seek	na

This command moves the R/W heads to the cylinder specified in the Shadow Register Block registers. The drive sets BSY and starts seek operation. After the completion of a seek operation, the drive asserts DSC[5], negates BSY, and return the interrupt.

If CY, HD and SN registers show invalid address, “ID Not Found” error is reported and no seek operation shall be executed. All commands related to data access possess Implied Seek function and don't need this command.

10.7.13 Toshiba Specific

COMMAND CODE	1 0 0 0 X X X X
	1 0 0 1 1 0 1 0
	1 1 1 1 0 0 0 0
	1 1 1 1 0 1 1 1
	1 1 1 1 1 0 1 X
	1 1 1 1 1 1 X X

These commands are only for factory use. Host must not issue them.

10.7.14 Execute Diagnostics (90h)

COMMAND CODE	1 0 0 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	na	0H
CY	na	0000H
HD	na	0H
SN	na	01H
SC	na	01H
FT	na	na

[5] ATA-2 Notes: Prior to ATA-2 standard, this bit indicated that the device was on track. This bit may be used for other purposes in future standards. For compatibility the drive supports this bit as ATA-1 specifies. User is recommended not to use this bit.

This command enables the drive to execute following self-test and reports the results to the error register described in Table 10.7.2-1.

(1) ROM checksum test
(2) RAM test
(3) Controller LSI register test

An interrupt is generated at the completion of this command.

When two drives are daisy-chained on the interface, both drives execute the self test and the Drive0 reports valid error information of the two drives.

10.7.15 Initialize Device Parameters (91h)

COMMAND CODE	1 0 0 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive number	no change
CY		na
HD	total number of heads-1	na
SN		na
SC	number of sector per track	na
FT		na

This command specifies the number of sectors per track and the number of heads per cylinder to set head switching point and cylinder increment point. Specified values affect Number of the current logical heads, Number of logical sectors per track, which can be read by Identify Device Command.

On issuing this command, the content of CY register shall not be checked. This command will be terminated with ABORT error when it is issued on an invalid HD or SC register setting (the combination of HD and SC register exceeds the drive parameter.

Any drive access command should accompany correct HD, SN register with heads and sectors within the number specified for this command. Otherwise, it results in “ID not found” error. If the number of heads and drives is within the specified number, command gives parameter to convert an address to access into Logical Block Address (LBA). “ ID Not Found” error also occur when this LBA exceeds the total number of user addressable sectors. The command does not affect LBA address mode.

10.7.16 Download Microcode (92h)

COMMAND CODE	1 0 0 0 0 0 1 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive number	no change
CY	Buffer offset (only used for FT = 03h, otherwise 00h)	na
HD	0h	na
SN	number of sector(high order)	na
SC	number of sector(low order)	01h/02h (only used for FT=03h, otherwise na)
FT	subcommand code	na

This command enables the host to alter the drive's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number register and the Sector Count register. The Sector Number register shall be used to extend the Sector Count register to create a 16-bit sector count value. The Sector Number register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number register and the Sector Count register shall specify no data is to be transferred. This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Features register are suppored:

- 03h - Download with offsets and save microcode for immediate and future use.
- 07h - Download and save microcode for immediate and future use.

The Download with offsets and save microcode for immediate and future use allows the application client to transfer microcode in two or more DOWNLOAD MICROCODE commands.

The download block count value in the Count and Sector Number register shall specify how many 512-byte blocks of data are being transferred in one command.

The Buffer Offset value is defined by the value in Cylinder Register. The buffer offset value is the starting location in the data relative to the last successful DOWNLOAD MICROCODE command received by the device with a Buffer Offset of zero. The buffer offset value is the byte count divided by 512.

If the current buffer offset is not equal to the sum of the previous DOWNLOAD MICROCODE command buffer offset and the previous sector count, then the device reports command aborted for the DOWNLOAD MICROCODE command and discards all previously downloaded microcode. The first DOWNLOAD MICROCODE command shall have a buffer offset of zero.

If the device receives a command other than DOWNLOAD MICROCODE prior to the receipt of the last segment, then the device processes the new command and discards previously downloaded microcode. During the processing of a power-on reset, a hardware reset, or a software reset prior to applying the new microcode, the device discards any received microcode segments.

Please refer to ATA8-ACS for details.

10.7.17 Read Multiple (C4h)

COMMAND CODE	1 1 0 0 0 1 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive number	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	number of sector to read	na
FT	na	na
LBA	starting address	na

The read multiple command performs similarly to the Read Sectors command except for the following features. Interrupts are not issued on each sector, but on the transfer of each block which contains the number of sectors defined by a Set Multiple Mode command or the default, if no intervening Set Multiple command has been issued.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple Mode command are transferred without interrupts. DRQ qualification of the transfer is required only at the start of a data block transfer, not required for the transfer of each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which shall be executed prior to the Read Multiple command.

When the Read Multiple command is issued, the Sector Count Register contains the number of required sectors (not the number of blocks or the block count). If the number of required sectors is not evenly divisible by the block count, The redundant sectors are transferred during the final partial block transfer. The partial block transfer shall be for N sectors, where

N = The redundant sector count (block count)

If the Read Multiple command is attempted when Read Multiple command are disabled, the Read Multiple operation shall be rejected with an Aborted Command error.

Disk errors occurred during Read Multiple command are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data, including corrupted data, shall be transferred as they normally would .

The contents of the Command Block Registers following the transfer of a data block which has a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or defective blocks are transferred only when the error is a correctable data error. All other errors after the transfer of the block containing the error terminates the command . Interrupts are generated when DRQ is set at the beginning of each block or partial block.

10.7.18 Read Multiple EXT (29h)

COMMAND CODE	0 0 1 0 1 0 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	Drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command is basically identical to Read Multiple command except register setting.

This command is available in LBA addressing only.

10.7.19 Write Multiple (C5h)

COMMAND CODE	1 1 0 0 0 1 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive number	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	number of sector to write	na
FT	na	na
LBA	starting address	na

This command performs similarly to the Write Sectors command except for the following features. The Drive sets BSY immediately upon receipt of the command, and interrupts are not issued on each sector but on the transfer of each block which contains the number of sectors defined by Set Multiple Mode command or the default if no intervening Set Multiple command has been issued.

Command execution is identical to the Write Sectors operation except that no interrupt is generated during the transfer of number of sectors defined by the Set Multiple Mode command but generated for each block. DRQ qualification of the transfer is required only for each data block, not for each sector.

The block count of sectors to be transferred without programming of intervening interrupts by the Set Multiple Mode command, which shall be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the host sets the number of sectors (not the number of blocks or the block count) it requests in the Sector Count Register. If the number of required sectors is not evenly divisible by the block count, the redundant sectors are transferred during the final partial block transfer. The partial block transfer shall be for N sectors, where

N = The redundant sector count (block count)

If the Write Multiple command is attempted when Write Multiple command are disabled, the Write Multiple operation shall be rejected with an Aborted Command error.

Disk errors occurred during Write Multiple command are posted after the attempted disk write of the block or partial block which are transferred. The Write Multiple command is terminated at the sector in error , even if it was in the middle of a block. Subsequent blocks are not transferred after an error. Interrupts are generated for each block or each sector, when DRQ is set .

After the transfer of a data block which contains a sector with error, the contents of the Command Block Registers are undefined. The host should retry the transfer as individual requests to obtain valid error information.

10.7.20 Write Multiple EXT (39h)

COMMAND CODE	0 0 1 1 1 0 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command is basically identical to Write Multiple command except register setting.

This command is available in LBA addressing only.

10.7.21 Write Multiple FUA EXT (CEh)

COMMAND CODE	0 0 1 1 1 0 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command provides the same function as the Write Multiple EXT command except the regardless of whether write caching in the device is enabled or not, the user data shall be written to the media before ending status for the command is reported.

This command is available in LBA addressing only.

10.7.22 Set Multiple Mode (C6h)

COMMAND CODE	1 1 0 0 0 1 1 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	na	na
HD	na	na
SN	na	na
SC	The number of sectors / block	na
FT	na	na

This command enables the drive to perform Read and Write Multiple operations and sets the block count for these commands.

The Sector Count Register is loaded with the number of sectors per block. The drive supports 1,2,4,8 or16 sectors per block.

Upon receipt of the command, the drive sets BSY=1 and checks the content of Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands. And these commands are enabled to be executed. If a block count is not supported, this command shall be terminated with the report of an Aborted Command error , and Read Multiple and Write Multiple commands are disabled.

If the Sector Count Register contains 0 when the command is issued, Read Multiple and Write Multiple commands are disabled.

In case of software reset, the result depends on the setting of Set Feature command. If FT=66h, the mode is not changed. If FT = CCh, the mode reverts to power on default (16 sectors).

10.7.23 Read DMA (C8h/C9h)

COMMAND CODE	1 1 0 0 1 0 0 X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to read	na
FT	na	na
LBA	staring address	na

This command is basically identical to Sector command except following features.

- Host initialize the DMA channel before issuing command.
  - Data transfer is initiated by DMARQ and handled by the DMA channel in the host.
  - Drive issues only one interrupt at the completion of each command to show the status is valid after data transfer.

  During DMA transfer phase, either BSY or DRQ is set to 1.
  When a command is completed, CY, HD, SN register (LBA register) shows the sector transferred the latest.

  If the drive detects unrecoverable error, the drive terminate the command and CY, HD, SN register (LBA register) shows the sector where error occurred.

10.7.24 Read DMA EXT (25h)

COMMAND CODE	0 0 1 0 0 1 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command is basically identical to Read DMA command except for the register settings.

This command is available in LBA addressing mode only.

10.7.25 Write DMA (CAh/CBh)

COMMAND CODE	1 1 0 0 1 0 1 X	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
CY	starting cylinder	na
HD	starting head	na
SN	starting sector	na
SC	no. of sector to write	na
FT	na	na
LBA	staring address	na

This command is basically identical to Sector command except for the following differences.

- Host initialize the DMA channel before issuing command.
  - Data transfer is initiated by DMARQ and handled by the DMA channel in the host.
  - Drive issue only one interrupt at the completion of each command to show the status is valid after data transfer.

During DMA transfer phase, either BSY or DRQ is set to 1.
When a command is completed, CY, HD, SN register (LBA register) shows the sector transferred the latest.
If the drive detects unrecoverable error, the drive terminates the command and CY, HD, SN register (LBA register) shows the sector where error has occurred.

10.7.26 Write DMA EXT (35h)

COMMAND CODE	0 0 1 1 0 1 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command is basically identical to Write DMA command for the register settings

This command is available in LBA addressing mode only.

10.7.27 Write DMA FUA EXT (3Dh)

COMMAND CODE	0 0 1 1 0 1 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	Reserved
LBA Low(exp)	LBA(31:24)	Reserved
LBA Mid	LBA(15:8)	Reserved
LBA Mid(exp)	LBA(39:32)	Reserved
LBA High	LBA(23:16)	Reserved
LBA High(exp)	LBA(47:40)	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command provides the same function as the WRITE DMA EXT command except that regardless of whether write caching in the device is enabled or not, the user data shall be written to the media before ending status for the command is reported.

This command is available in LBA addressing mode only.

10.7.28 READ FPDMA QUEUED (60h)

COMMAND CODE	0 1 1 0 0 0 0 0	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	F 1 R 0 R R R R	Na
LBA Low	LBA(7:0)	na
LBA Low(exp)	LBA(31:24)	na
LBA Mid	LBA(15:8)	na
LBA Mid(exp)	LBA(39:32)	na
LBA High	LBA(23:16)	na
LBA High(exp)	LBA(47:40)	na
SC	TAG(7:3) Reserved(2:0)	na
SC(exp)	Reserved	na
FT	Sector Count 7:0	-
FT(exp)	Sector Count 15:8	-

TAG The TAG value shall be assigned by host software to be different from all other TAG values corresponding to outstanding commands. The assigned TAG value shall not exceed the value in IDENTIFY DEVICE word 75.

F When set to one forces the data to be retrieved from the storage media regardless of whether the drive holds the requested information in its buffer or cache. If the drive holds a modified copy of the requested data as a result having cached writes, the modified data is first written to the media before being retrieved from the storage media as part of this operation. When cleared to zero the data may retrieved either from the drive's storage media or from buffers/cache that the drive may include.

Others All Other resisters have contents consistent with the READ DMA QUEUED EXT commands defined in parallel ATA, including the Sector Count 15:0 convention where a value of zero specifies that 65,536 sectors are to be transferred.,

10.7.29 WRITE FPDMA QUEUED (61h)

COMMAND CODE	0 1 1 0 0 0 0 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	F 1 R 0 R R R R	Na
LBA Low	LBA(7:0)	na
LBA Low(exp)	LBA(31:24)	na
LBA Mid	LBA(15:8)	na
LBA Mid(exp)	LBA(39:32)	na
LBA High	LBA(23:16)	na
LBA High(exp)	LBA(47:40)	na
SC	TAG(7:3) Reserved(2:0)	na
SC(exp)	Reserved	na
FT	Sector Count 7:0	-
FT(exp)	Sector Count 15:8	-

TAG The TAG value shall be assigned by host software to be different from all other TAG values corresponding to outstanding commands. The assigned TAG value shall not exceed the value in IDENTIFY DEVICE word 75.

F When set to one forces the data to be retrieved from the strage media regardless of whether the drive holds the requested information in its buffer or cache. If the drive holds a modified copy of the requested data as a result having cached writes, the modified data is first written to the media before being retrieved from the storage media as part of this operation. When cleared to zero the data may retrieved either from the drive's storage media or from buffers/cache that the drive may include.

Others All Other resisters have contents consistent with the READ DMA QUEUED EXT commands defined in parallel ATA, including the Sector Count 15:0 convention where a value of zero specifies that 65,536 sectors are to be transferred.,

10.7.30 POWER CONTROL (Exh/9xh)

COMMAND CODE	1 1 1 0 X X X X	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	Reserved (except for E1h command)	na
HD	Reserved	na
SN	Reserved (except for E1h command)	Reserved (except for E1h command)
SC	shown below	00/FFH (for E5/98 command) na(for other command)
FT	Reserved (except for E1h command)	na

Power Control is a group of commands which controls low power mode in the drive. The drive has three types of power mode:

Idle, Stand-by and Sleep mode

At the completion of disk access, the drive automatically enters the idle mode.

There are two ways to shift to the stand-by mode (to stop rotation of spindle motor).

By a command from the host
By internal timer

The internal timer is set by Stand-by or Idle command. If the drive receives disk access command from the host when it is in stand-by mode, the spindle starts rotating and the drive executes read/write operation.

After power on, the spindle starts rotating and enters the idle mode. During idle or stand-by, READY bit is set and the drive is ready to receive a command.

To be specific, there are four different sub-commands defined by lower 4 bits of command as follows. The drive is in the idle mode when it is in default condition after power-on.

10.7.30.1 Stand-by Immediate (E0/94)

SC=X (Don't care)

The drive enters the stand-by mode immediately by this command. If the drive is already in the stand-by mode, it does no-operation and the stand-by timer doesn't start .The drive issues an interrupt and reports the host that the command has been completed before it virtually enters the stand-by mode.

10.7.30.2 Idle Immediate (E1/95) (Except for the Idle Immediate with Unload feature)

FT=X, SC=X, CY(LBA High/Mid)=X, SN(LBA Low)=X

The drive enters the idle mode immediately by this command. If the drive is already in the idle mode, it does no-operation. If stand-by timer is enabled, timer will start. After the drive enters the idle mode, the drive issues interrupt to report the host that the command has been completed.

10.7.30.3 Idle Immediate with Unload Feature (E1)

Register Setting:
FT=44h, SC=00h, CY(LBA High/Mid)=554Eh, SN(LBA Low)=4Ch

The UNLOAD FEATURE of the IDLE IMMEDIATE command provides a method for the host to cause a device that is a hard disk drive to move its read/write heads to a safe position as soon as possible. Upon receiving an IDLE IMMEDIATE command with the UNLOAD FEATURE, a device shall:

a) stop read look-ahead if that operation is in process;
b) stop writing cached data to the media if that operation is in process;
c) the device shall retract the heads onto the ramp;
d) transition to the Idle mode.

A device shall report command completion after the heads have been unloaded.

Normal comletion:
SN(LBA Low) shall be set to C4h if the unload has completed successfully.
Shall be set to 4Ch if the unload was not accepted or has failed.

10.7.30.4 Stand-by (E2/96)

This command causes the drive to enter stand-by mode.

If SC is non-zero then stand-by timer shall be enabled. The value in SC shall be used to determine the time programmed into the stand-by timer.

If SC is zero then the stand-by timer is disabled.

Value in SC register	Setting
0	Time out disabled
1-240	(SC x 5) sec.
241-251	((value - 240) x 30) min.
252	21 min
253	Period between 8 and 12 hrs
254	Reserved
255	21 min 15 sec.

When the specified time period has passed, the drive enters stand-by mode. If a disk access command is received during stand-by mode, the spindle starts rotating and the drive executes read/write operation. After completing the command, the drive reset stand-by timer and the timer starts counting down.

10.7.30.5 Idle (E3/97)

This command causes the drive to enter idle mode.

If SC is non-zero then stand-by timer shall be enabled. The value in SC shall be used to determine the time programmed into the stand-by timer.

If SC is zero then the stand-by timer is disabled.

Value in SC register	Setting
0	Time out disabled
1-240	(SC x 5) sec.
241-251	((value - 240) x 30) min.
252	21 min
253	Period between 8 and 12 hrs
254	Reserved
255	21 min 15 sec.

When the specified time period has expired, the drive enters the stand-by mode. If disk access command is received during the stand-by mode, the spindle starts rotating and executes read/write operation. After completing the command, The drive resets stand-by timer and the timer starts counting down.

10.7.30.6 Check Power Mode (E5/98)

SC result value=00 indicates that the drive is in stand-by mode or going into stand-by mode or is shifting from stand-by mode into idle mode.

SC result value=FFH indicates that the drive is in idle mode.

10.7.30.7 Sleep (E6/99)

When SC=X, the drive enters sleep mode immediately. After entering the sleep mode, the drive issues an interrupt to report the host that the command has been completed. The drive recovers from sleep mode and enters stand-by mode by receiving a reset.

10.7.31 Read Buffer (E4h)

COMMAND CODE	1 1 1 0 0 1 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command transfers a specified sector of data (512 bytes) from the buffer in the drive to the host. When this command is issued, the drive sets BSY, sets up the buffer for read operation, sets DRQ, resets BSY, and generates an interrupt. The host reads up to 512 bytes of data from the buffer.

10.7.32 Write Buffer (E8h)

COMMAND CODE	1 1 1 0 1 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	Drive no.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command transfers a sector of data from the host to the specified 512 bytes of the drive . When this command is issued, the drive will set up the buffer for write operation, and set DRQ. The host may then write up to 512 bytes of data to the buffer.

10.7.33 Identify Device (ECh)

COMMAND CODE	1 1 1 0 1 1 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	drive no.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

The identify device command requests the drive to transfer parameter information to the host. When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and issues an interrupt. The host may read the parameter information of the sector buffer. The parameter words in the buffer are arranged as shown in Table 10.7-1 ~ Table 10.7-6.

Table 10.7-1 Identify Information

WORD	DESCRIPTION	Hex.
0	General configuration 15 0=ATA device 14-8 Reserved 7 1=Removable cartridge device 6 1=Fixed device 5-3 Reserved 2 Response incomplete 1-0 Reserved	0040
1	Number of default logical cylinders	[1*]
2	Specific configuration	C837
3	Number of default logical heads	[2*]
4	Reserved	0000
5	Reserved	0000
6	Number of default logical sectors h logical track	[3*]
7-9	Reserved	
10-19	Serial Number (20 ASCII characters)	
20	Reserved	0000
21	Buffer Size	4000
22	Reserved	0000
23-26	Firmware Revision (8 ASCII characters)	
27-46	Controller model # (40 ASCII characters)	
47	15-8 80h 7-0 00_H = READ/WRITE MULTIPLE command not implemented 01_H- FF_H = Maximum number of sectors that can be transferred per interrupt on READ/WRITE MULTIPLE commands	8010
48	Reserved	0000
49	Capabilities 15-14 Reserved 13 1=Standby timer values as specified in ATA/ATAPI-6 specification are supported 0=Standby timer values are vendor specific 12 Reserved 11 1=IORDY supported 10 1=IORDY can be disabled 9 1=LBA supported 8 1=DMA supported 7-0 Reserved	2F00
50	Capabilities 15 0 (Fixed) 14 1 (Fixed) 13-1 Reserved 0 1= a device specific Standby timer value minimum.	4000
51	15-8 PIO data transfer cycle timing mode 7-0 Reserved	0200
52	Reserved	0000
53	15-3 Reserved 2 1=the fields reported word 88 are valid 0=the fields reported word 88 are not valid 1 1=the fields reported words 64-70 are valid 0=the fields reported words 64-70 are not valid 0 1=the fields reported words 54-58 are valid 0=the fields reported words 54-58 are not valid	0007
54	Number of current cylinders	XXXX
55	Number of current heads	XXXX
56	Number of current sectors per track	XXXX

Table 10.7-2 Identify Information (Continued)

WORD	DESCRIPTION	Hex.
57-58	Current capacity in sectors (Number of current cylinders * Number of current heads * Number of current sectors per track)	XXXX
59	15-9 Reserved 8 1=Multiple sector setting is valid 7-0 XXh=Current setting for number of sectors that can be transferred per interrupt on R/W Multiple command	01XX
60-61	Total number of user addressable sectors (LBA mode only)	XXXXXXX
62	15-0 Reserved	XX07
63	15-8 Multiword DMA transfer mode active 7-0 Multiword DMA transfer mode supported	XX07
64	15-8 reserved 7-0 Advanced PIO Transfer Modes Supported bit 7-2 Reserved bit 1 = 1 PIO MODE 4 supported bit 0 = 1 PIO MODE 3 supported	0003
65	Minimum Multiword DMA Transfer Cycle Time Per Word (ns)	0078
66	Manufacturer's Recommended Multiword DMA Transfer Cycle Time	0078
67	Minimum PIO Transfer Cycle Time Without Flow Control (ns)	0078
68	Minimum PIO Transfer Cycle Time With IOCHRDY Flow Control	0078
69-74	Reserved	0000
75	Queue depth 15-5 Reserved 4-0 Maximum queue depth – 1	001F
76	Serial ATA capabilities 15-12 Reserved 11 Supports Unload while NCQ commands outstanding 10 Supports Phy event counters 9 Supports receipt of host-initiated interface power management request 8 Supports native command queuing 7-4 Reserved 3 Reserved for future Serial ATA 2 1=Supports Serial ATA Gen-2 signaling speed 1 1=Supports Serial ATA Gen-1 signaling speed (1.5Gbps) 0 Reserved (cleared to zero)	0F06
77	Serial ATA Additional capabilities 15-6 Reserved 5 Supports NCQ Queue Management Command 4 Supports NCQ Streaming 3-1 Coded value indicating current negotiated Serial ATA signal speed 0 Reserved (cleared to zero)	000X
78	Serial ATA features supported 15-7 Reserved 6 1=Supports software setting preservation 5 Reserved 4 1=Supports in-order data delivery 3 1=device supports initiating interface power management 2 1=supports DMA Setup Auto Activate Optimization 1 1=supports non-zero buffer offsets in DMA Setup FIS 0 Reserved (cleared to zero)	004C
79	Serial ATA features enabled 15-7 Reserved 6 1=Software settings preservation enabled 5 Reserved 4 1=in-order data delivery enabled 3 1=device initiating interface power management enabled 2 1=DMA Setup Auto Activate optimization enabled 1 1=non-zero buffer offsets in DMA Setup FIS enabled 0 Reserved (cleared to zero)	00XX

Table 10.7-3 Identify Information (Continued)

WORD	DESCRIPTION	Hex.
80	Major version number 0000h or FFFFh = device does not report version 15-9 Reserved for ATA-9~14 8 1=supports ATA/ATAPI-8 7 1=supports ATA/ATAPI-7 6 1=supports ATA/ATAPI-6 5 1=supports ATA/ATAPI-5 4 1=supports ATA/ATAPI-4 3 1=supports ATA-3 2 1=supports ATA-2 1 1=supports ATA-1 0 Reserved	01F8
81	Minor version number 0000h or FFFFh = device does not report version	0000
82	Command set supported. 0000h or FFFFh = command set notification not supported 15 Reserved 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 Reserved 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt supported 7 1=release interrupt supported 6 1=look-ahead supported 5 1=write cache supported 4 1=supports PACKET Command feature set 3 1=supports power management feature set 2 1=supports removable feature set 1 1=supports security feature set 0 1=supports SMART feature set	746B
83	Command set supported. 0000h or FFFFh = command set notification not supported 15 0 (Fixed) 14 1(Fixed) 13 1=FLUSH CACHE EXT command supported 12 1=FLUSH CACHE command supported 11 1=Device Configuration Overlay supported 10 1=48-bit Address feature set supported 9 1=Automatic Acoustic Management feature set supported 8 1=Set MAX security extension supported 7 Reserved 6 1=SET FEATURES subcommand required to spin up after power-up 5 1=Power-Up in Standby feature set supported 4 1=Removable Media Status Notification feature set supported 3 1=Advanced Power Management feature set supported 2 1=CFA feature set supported 1 1=READ / WRITE DMA QUEUED supported 0 1=DOWNLOAD MICROCODE command supported	7D09

Table 10.7-4 Identify Information (Continued)

WORD	DESCRIPTION	Hex.
84	Command set/feature supported extension 15 0 (Fixed) 14 1(Fixed) 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12-9 Reserved 8 1= 64-bit World wide name supported 7 Reserved 6 1=Write DMA FUA EXT and WRITE multiple FUA EXT commands supported 5 1=General Purpose Logging feature set supported 4 1=Reserved 3 1=Media Card Pass Through Command feature set supported 2 1=Media serial number supported 1 1=SMART self-test supported 0 1=SMART error logging supported	6163
85	Command set/feature enabled 15 Reserved 14 1=NOP command enabled 13 1=READ BUFFER command enabled 12 1=WRITE BUFFER command enabled 11 Reserved 10 1=Host Protected Area feature set enabled 9 1=DEVICE RESET command enabled 8 1=SERVICE interrupt enabled 7 1=release interrupt enabled 6 1=look -ahead enabled 5 1=write cache enabled 4 1=PACKET Command feature set supported 3 1=power management feature set enabled 2 1=removable feature set enabled 1 1=Security feature set enabled 0 1=SMART feature enabled	XXXX
86	Command set/feature enabled 15 1=WORDS 119 and 120 are valid 14 Reserved 13 1=FLUSH CACHE EXT command supported 12 1=FLUSH CACHE command supported 11 1=Device Configuration Overlay supported 10 1=48-bit Address feature set supported 9 1=Automatic Acoustic Management feature set enabled 8 1=SET MAX security extension enabled by SET MAX SET PASSWORD 7 Reserved 6 1=SET FEATURES subcommand required to spin-up after power-up 5 1=Power-Up In Standby feature set enabled 4 1=Removable Media Status Notification feature set enabled 3 1=Advanced Power Management feature set enabled 2 1=CFA feature set enabled 1 1=READ / WRITE DMA QUEUED supported 0 1=DOWNLOAD MICROCODE command supported	XX0X
87	Command set/feature default 15 0 (Fixed) 14 1 (Fixed) 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12-9 Reserved 8 1= 64-bit World wide name supported 7 Reserved 6 1=Write DMA FUA EXT and Write Multiple FUA EXT commands supported 5 1=General Purpose Logging feature set supported 4 Reserved 3 1=Media Card Pass Through Command feature set enabled 2 1=Media serial number is valid 1 1=SMART self-test supported 0 1=SMART error logging supported	6163

Table 10.7-5 Identify Information (Continued)

WORD	DESCRIPTION	Hex.
88	15-8 Ultra DMA transfer mode selected 7-0 Ultra DMA transfer modes supported	XX3F
89	Time required for security erase unit completion	00XX
90	Time required for Enhanced Security erase completion	00XX
91	Current Advanced Power Management setting 15-8 Reserved 7-0 Current Advanced Power Management setting set by Set Features Command	00XX
92	Master Password Revision Code	XXXX
93	Hardware reset result of P-ATA specification. No specification for Serial ATA.	0000
94	Current automatic acoustic management value 15-8 Vendor's recommended acoustic management value 7-0 Current automatic acoustic management value	0000
95-99	Reserved	0000
100-103	Maximum user LBA for 48-bit Address feature set	[5*]
104-105	Reserved	0000
106	Physical sector size / Logical Sector Size 15 0 (Fixed) 14 1 (Fixed) 13 1 = Device has multiple logical sectors per physical sector 12 1= Device Logical Sector Longer than 256 Words 11-4 Reserved 3-0 2^X logical sectors per physical sector	4000
107	Reserved	0000
108	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)	XXXX
109	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)	XXXX
110	15-0 Unique ID (31:16)	XXXX
111	15-0 Unique ID (15:0)	XXXX
112-116	Reserved	0000
117-118	Words per Logical Sector	00000000
119	Commands and feature sets supported 15 0 (Fixed) 14 1 (Fixed) 13-7 Reserved 6 1= Extended Status Reporting feature set is supported 5 1= The Free-fall Control feature set is supported 4 1= The DOWNLOAD MICROCODE command with mode 3 is supported 3 1= The READ LOG DMA EXT and WRITE LOG DMA EXT command are supported 2 1= The WRITE UNCORRECTABLE EXT command is supported 1 1= The Write-Read-Verify feature set is supported 0 Reserved for DDT	4018
120	Commands and feature sets supported or enabled 15 0 (Fixed) 14 1 (Fixed) 13-7 Reserved 6 1= Extended Status Reporting feature set is supported 5 1= The Free-fall Control feature set is enabled 4 1= The DOWNLOAD MICROCODE command with mode 3 is supported 3 1= The READ LOG DMA EXT and WRITE LOG DMA EXT command are supported 2 1= The WRITE UNCORRECTABLE EXT command is supported 1 1= The Write-Read-Verify feature set is enabled 0 Reserved for DDT	4018
121-126	Reserved	0000

Table 10.7-6 Identify Information (Continued)

WORD	DESCRIPTION	Hex.
127	Removable Media Status Notification feature set supported 15-2 Reserved 1-0 00=Removable Media Status Notification feature set not supported 01=Removable Media Status Notification feature set supported 10=Reserved 11=Reserved	0000
128	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-6 Reserved 5 1=Enhanced security erase supported 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported	0XXX
129-159	Reserved	0000
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000
161-167	Reserved	0000
168	Device Nominal Form Factor 15-4 Reserved 3-0 Device Nominal Form Factor	0003
169-175		0000
176-205	Current media serial number	0000
206	SCT Command Transport 15-12 Vendor Specific 11-6 Reserved 5 1 = SCT Command Transport Data Tables supported 4 1 = SCT Command Transport Feature Control supported 3 1 = SCT Command Transport Error Recovery Control supported 2 1 = SCT Command Transport Write Same supported 1 1 = SCT Command Transport Long Sector Access supported 0 1 = SCT Command Transport supported	003D
207-216	Reserved	0000
217	Nominal media rotation rate	1518
218-221	Reserved	0000
222	Transport major version number. 0000h or FFFFh = device does not report version 15:12 Transport Type – 0 = Parallel, 1 = Serial, 2-15 = Reserved Parallel Serial 11:5 Reserved Reserved 4 Reserved SATA Rev 2.6 3 Reserved SATA Rev 2.5 2 Reserved SATA II: Extensions 1 Reserved SATA 1.0a 0 ATA8-APT ATA8-AST	101F
223-233	Reserved	0000
234	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	0001
235	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	0080
236-254	Reserved	0000
255	Integrity word 15-8 Checksum 7-0 Signature	XXA5

Word descriptions:

WORD 0: General configuration
bit 15 0=ATA
bit 14-8 Reserved
bit 7 1=Removable cartridge
bit 6 1=Fixed disk drive
bit 5-3 Reserved
bit 2 Response incomplete
bit 1-0 Reserved

The value for this WORD is 0040h.
WORD 1: Logical cylinder number that user can access (in default mode) [*1]

WORD 2: Specific configuration
"37C8" : Drive requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is incomplete.
"738C" : Drive requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is complete.
"8C73" : Drive does not requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is incomplete.
"C837" : Drive does not requires SET FEATURES subcommand to spin-up after power-up and IDENTIFY DEVICE response is complete.
"All other values" : Reserved
Power-up in Standby feature set is not supported.
The value for this WORD is C837h.

WORD 3: Logical head number that user can access (in default mode) [*2]

WORD 4-5: Reserved

WORD 6: The number of logical sector per track (in default mode) [*3]

Default Values : [*1],[*2],[*3]

Drive Type	[*1] : Word 1	[*2] : Word 3	[*3] : Word 6
MK6476GSX	16383	16	63
MK5076GSX			
MK3276GSX			
MK2576GSX			
MK1676GSX			
MK1276GSX			

WORD 7-9: Reserved

WORD 10-19: Serial number

WORD 20: Reserved

WORD 21: Buffer Size
The value for this WORD is 4000h.
WORD 22: Reserved

WORD 23-26: Firmware revision (8 ASCII characters)

WORD 27-46: Model name (40 ASCII characters)

Drive Type	
MK6476GSX	TOSHIBA_**MK6476GSX**_..._
MK5076GSX	TOSHIBA_**MK5076GSX**_..._
MK3276GSX	TOSHIBA_**MK3276GSX**_..._
MK2576GSX	TOSHIBA_**MK2576GSX**_..._
MK1676GSX	TOSHIBA_**MK1676GSX**_..._
MK1276GSX	TOSHIBA_**MK1276GSX**_..._

"_" indicates ASCII space code.

WORD 47:

bit 15 - 8 shall be set to 80h
bit 7 - 0 Maximum number of sectors that can be transferred per interrupt on READ/WRITE MULTIPLE commands.

The default value for this WORD is 8010h.

WORD 48: Reserved

WORD 49: Capabilities

bit 15-14 0=Reserved
bit 13 1=Standby timer value shall be as specified in ATA-/ ATAPI-6 specification
0=Standby timer value are vendor specific
bit 12 Reserved (For advanced PIO mode support)
bit 11 1=IORDY is supported.
bit 10 1=IORDY function can be disabled.
bit 9 1=LBA supported
bit 8 1=DMA supported
bit 7- 0 Reserved

The value for this WORD is 2F00h.

WORD 50: Capabilities

bit 15 0 (Fixed)
bit 14 1 (Fixed)
bit 13-1 Reserved
bit 0 1=drive has a minimum Standby timer value that is drive specific.

Standby timer value is set to 5 minutes or more. The value for this WORD is 4000h.

WORD 51: PIO data transfer cycle timing mode

bit 15- 8 PIO data transfer cycle timing mode
bit 7- 0 Reserved

The value returned in Bits 15-8 should fall into one of the mode 0 through mode.
Note: For backwards compatibility with BIOS written before Word 64 was defined for advanced modes, a drive reports in Word 51 the highest original PIO mode (i.e. PIO mode 0, 1, or 2) it can support.

The value for this WORD is 0200h.

WORD 52: Reserved

WORD 53:

bit15- 3 Reserved
bit 2 1= the fields reported in word 88 is valid
bit 1 1= the fields reported in words 64～70 are valid
bit 0 1= the fields reported in words 54～58 are valid

If the number of heads and sectors exceed the drive parameter, bit 0 and related WORD 54-58 shall be cleared to 0. The default value for this WORD is 0007h.

WORD 54: Number of current cylinders defined by INITIALIZE DEVICE PARAMETERS command

WORD 55: Number of current heads defined by INITIALIZE DEVICE PARAMETERS command

WORD 56: Number of current sectors/track defined by INITIALIZE DEVICE PARAMETERS command

WORD 57-58: Total number of sectors calculated by word 54 - 56

bit31-24 by word 58 bit 7- 0
bit23-16 by word 58 bit 15- 8
bit15- 8 by word 57 bit 7- 0
bit 7- 0 by word 57 bit 15- 8

The default values for each models are.

Drive Type	[*4] : Word 57 - 58
MK6476GSX	16,514,064 (FBFC10H)
MK5076GSX	16,514,064 (FBFC10H)
MK3276GSX	16,514,064 (FBFC10H)
MK2576GSX	16,514,064 (FBFC10H)
MK1676GSX	16,514,064 (FBFC10H)
MK1276GSX	16,514,064 (FBFC10H)

WORD 59:
bit15- 9 Reserved

bit 8 1=bit 7- 0 shows number of sectors for multiple sector operation (multiple sector operation is enabled by SET MULTIPLE command).
bit 7～0 The number of sectors transferred for XX_H =Write / Read multiple command with 1 Interrupt (Current value shall be set by SET MULTIPLE command. The default value is 16).

The default value for this WORD is 0110h.

WORD 60-61: Maximum number of sectors that user can access in LBA mode
bit27-24 by word 61 bit 3- 0
bit23-16 by word 61 bit 15- 8
bit15- 8 by word 60 bit 7- 0
bit 7- 0 by word 60 bit 15- 8

The maximum value that shall be placed in this field is 0FFFFFFFh.

WORD 62: Reserved

WORD 63: Mode information for multiword DMA
bit15- 8 Active mode
bit 10 1=Mode 2 is active
bit 9 1=Mode 1 is active
bit 8 1=Mode 0 is active
bit 7- 0 Supported mode
bit 2 1=mode 2 is supported
bit 1 1=mode 1 is supported
bit 0 1=mode 0 is supported

Support bit reflects setting by SET FEATURE command.
The default value for this WORD is 0407h and the default figure is mode 2

WORD 64: Mode information for Advanced PIO transfer

bit 7- 0 Supported mode
bit 1 1=mode 4 is supported
bit 0 1=mode 3 is supported

The value for this WORD is 0003h.

WORD 65: Minimum multiword DMA transfer mode cycle time per word (ns)
If this bit is supported, word 53 bit 1 shall be set. The value for this WORD is 0078h (120ns).

WORD 66: Manufacturer recommended multiword DMA transfer cycle time
If the data transfer is requested in a shorter cycle time than this definition, the data transfer may be kept pending with DMARQ low because data is not ready. The value for this WORD is 0078h (120ns).

WORD 67: Minimum PIO transfer cycle time without flow control (ns)

The Drive can guarantee correct data transfer without flow control in this cycle time or longer. If this bit is supported, word 53 bit 1 is to be set. The drives which support PIO mode 3 or higher shall support this field too. This figure shall not be less than 120. The value for this WORD is 0078h (120ns).

WORD 68: Minimum PIO transfer cycle time with IORDY flow control (ns)

If this bit is supported, word 53 bit 1 is to be set. The drive that support PIO mode 3 or higher shall support this field too. This figure shall not be less than 120. The value for this WORD is 0078h (120ns).

WORD 69-74: Reserved

WORD 75: Queue depth

This word is as defined in the ATA reference. The native command queuing scheme supports at most 32 queued commands, which coincides with the reporting capabilities of the ATA specification. In the native command queuing scheme, the host is required to issue only unique tag values for queued commands that have a value less than or equal to the value reflected in this field (i.e. for the drive reporting a value in this field of 15, corresponding to a maximum of 16 outstanding commands, the host shall never use a tag value greater than 15 when issuing native queued commands).

Word 75 shall be 001Fh.

WORD 76: Serial ATA capabilities

If not 0000h or FFFFh, the drive claims compliance with the Serial ATA specification and supports the signaling rate indicated in bits 1-3. Since Serial ATA will supports generational compatibility, multiple bits may be set. Bit 0 is reserved and shall be set to zero (thus a Serial ATA drive has at least one bit cleared this field and at least one bit set providing clear differentiation). If this field is not 0000h or FFFFh, words 77 through 79 shall be valid. If this field is 0000h or FFFFh the drive does not claim compliance with the Serial ATA specification and words 76 through 79 are not valid and shall be ignored.

bit 15-12	Reserved
bit 11	Supports Unload while NCQ commands outstanding.
bit 10	Phy event counters supported.
bit 9	Partial and Slumber interface power management states initiated by the host supported.
bit 8	Native command queuing scheme supported.
bit 7-3	Reserved.
bit 2	Gen-2 signaling rate supported.
bit 1	Gen-1 signaling rate supported
bit 0	Reserved

Word 76 shall be 0F06h.

WORD 77: Serial ATA Additional capabilities

Word 77 reports additional optional capabilities supported by the device. Support for this word is optional and if not supported, the word shall be zero indicating the device has no support for additional Serial ATA capabilities.

bit 15-6	Reserved
bit 5	NCQ QUEUE MANAGEMENT supported
bit 4	NCQ Streaming supported
bit 3-1	Coded value indicating current negotiated Serial ATA signal speed

Coded Values			Description
bit 3	bit 2	bit 1	
0	0	0	Signaling speed is not reported
0	0	1	Gen1 signaling speed of 1.5 Gbps
0	1	0	Gen2 signaling speed of 3.0 Gbps
0	1	1	Gen3 signaling speed of 6.0 Gbps
All Non-Defined Values			Reserved for future Serial ATA signaling speeds

bit 0 Reserved

The default value of Word 77 is 0002h when current negotiated speed is 1.5Gbps

The default value of Word 77 is 0004h when current negotiated speed is 3.0Gbps

WORD 78: Serial ATA features supported

If word 76 is not 0000h or FFFFh, word 78 reports the optional features supported by the drive.

bit 15-7	Reserved
bit 6	Software setting preservation supported
bit 5	Reserved
bit 4	Guaranteed in-order data delivery supported
bit 3	Device initiating power management requests to the host supported.
bit 2	DMA Setup FIS Auto Activate optimization supported.
bit 1	Non-zero buffer offsets in the DMA Setup FIS supported.
bit 0	Reserved

Word 78 shall be 004Ch.

WORD 79: Serial ATA features enabled

If word 76 is not 0000h or FFFFh, word 79 reports the optional features supported by the drive are enabled.

bit 15-7	Reserved
bit 6	Software setting preservation enabled
bit 5	Reserved
bit 4	Guaranteed in-order data delivery enabled
bit 3	Device initiating power management requests to the host enabled.
bit 2	DMA Setup FIS Auto Activate optimization enabled.
bit 1	Non-zero buffer offsets in the DMA Setup FIS enabled.
bit 0	Reserved

The default value of Word 79 shall be 0040h

WORD 80: Major version number

If not 0000h or FFFFh, the drive claims compliance with the major version(s) as indicated by bits 1 - 8 being equal to one. Values other than 0000h and FFFFh are bit significant. Since the ATA standards maintain downward compatibility, a drive may set more than one bit .

WORD 81: Minor version number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to this revision of the standard, Word 81 shall be 0000h or FFFFh.

WORD 82: Command sets supported

bit 15	Reserved
bit 14	NOP command supported
bit 13	READ BUFFER command supported
bit 12	WRITE BUFFER command supported
bit 11	Reserved
bit 10	Host Protected Area feature set supported
bit 9	DEVICE RESET command supported
bit 8	SERVICE interrupt supported
bit 7	Release Interrupt supported
bit 6	Look Ahead supported
bit 5	Write Cache supported
bit 4	PACKET feature set supported
bit 3	The Power Management feature set is supported
bit 2	The Removable feature set is supported
bit 1	The security feature set is supported
bit 0	The SMART feature set is supported

The value for this WORD is 746Bh.

WORD 83: Features/Command sets supported

bit 15	0 (Fixed)
bit 14	1 (Fixed)
bit 13	1=FLUSH CACHE EXT command supported
bit 12	1=FLUSH CACHE command supported
bit 11	1=Device Configuration Overlay supported
bit 10	1=48-bit Address feature set supported
bit 9	1=Automatic Acoustic Management feature set supported
bit 8	1=Set MAX security extension supported
bit 7	Reserved
bit 6	1=SET FEATURES subcommand required to spin up after power-up
bit 5	1=Power-Up in Standby feature set supported
bit 4	1=Removable Media Status Notification feature set supported
bit 3	Advanced Power Management feature set supported
bit 2	1=CFA feature set supported
bit 1	1=READ / WRITE DMA QUEUED supported
bit 0	1=DOWNLOAD MICROCODE command supported

The value for this WORD is 7D09h.

WORD 84: Features / Command sets supported

bit 15	0 (Fixed)
bit 14	1 (Fixed)
bit 13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
bit 12-9	Reserved
bit 8	1= 64-bit World wide name supported
bit 7	Reserved
bit 6	1=Write DMA FUA EXT and Write Multiple FUA EXT commands supported
bit 5	1=General Purpose Logging feature set supported
bit 4	Reserved
bit 3	1=Media Card Pass Through command feature set supported
bit 2	1=Media serial number supported
bit 1	1=SMART self-test supported
bit 0	1=SMART error logging supported

The value for this WORD is 6163h.

WORD 85: Features / Command sets enable

bit 15	Reserved
bit 14	NOP command enabled
bit 13	READ BUFFER command enabled
bit 12	WRITE BUFFER command enabled
bit 11	Reserved
bit 10	Host Protected Area feature set enabled
bit 9	DEVICE RESET command enabled
bit 8	SERVICE interrupt enabled
bit 7	Release Interrupt enabled
bit 6	Look Ahead enabled
bit 5	Write Cache enabled
bit 4	PACKET feature set supported
bit 3	The Power Management feature set is enabled
bit 2	The Removable feature set is enabled
bit 1	The security feature set is enabled
bit 0	The SMART feature set is enabled

The default value for this WORD is 7468h

WORD 86: Features / Command sets enabled

bit 15	1=WORDS 119 and 120 are valid
bit 14	Reserved
bit 13	1=FLUCH CACHE EXT command supported
bit 12	1=FLUSH CACHE command supported
bit 11	1=Device Configuration Overlay supported
bit10	1=48-bit Address feature set supported

bit 9 1=Automatic Acoustic Management feature set enabled
bit 8 1=SET MAX security extension enabled by SET MAX SET PASSWORD
bit 7 Reserved
bit 6 1=SET FEATURES subcommand required to spin-up after power-up
bit 5 1=Power-Up In Standby feature set enabled
bit 4 Removable Media Status Notification feature set enabled
bit 3 Advanced power Management feature set enabled
bit 2 CFA feature set enabled
bit 1 WRITE / READ DMA QUEUED command supported
bit 0 DOWNLOAD MICROCODE supported

The default value for this WORD is BC09h.

WORD 87: Features / Command sets enabled
bit 15 0 (Fixed)
bit 14 1 (Fixed)
bit 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
bit 12-9 Reserved
bit 8 1= 64-bit World wide name supported
bit 7 Reserved
bit 6 1=Write DMA FUA EXT and Write Multiple FUA EXT commands supported
bit 5 1=General Purpose Logging feature set supported
bit 4 Reserved
bit 3 1=Media Card Pass Through command feature set enabled
bit 2 1=Media serial number is valid
bit 1 1=SMART self-test supported
bit 0 1=SMART error logging supported

The value for this WORD is 6163h.

WORD 88: Mode information for Ultra DMA
The active mode reflects the command change.

bit 15-8 Active transfer mode
bit 13 1=Mode 5 is active
bit 12 1=Mode 4 is active
bit 11 1=Mode 3 is active
bit 10 1=Mode 2 is active
bit 9 1=Mode 1 is active
bit 8 1=Mode 0 is active
bit 7-0 Supported mode
bit 5 1=Mode 5 is supported
bit 4 1=Mode 4 is supported
bit 3 1=Mode 3 is supported
bit 2 1=Mode 2 is supported
bit 1 1=Mode 1 is supported
bit 0 1=Mode 0 is supported

The default value for this WORD is 003Fh

WORD 89: The time period for Security Erase Unit command completion shall be set.

TIMER	ACTUAL VALUE
0	Not specified
1-254	(Timer ×2) minutes
255	> 508 minutes

WORD 90: Time required for Enhanced Security erase completion

WORD 91: Current Advanced Power Management setting
bit 15-8 Reserved
bit 7-0 Current Advanced Power Management setting set by Set Features Command.

The default value for this WORD is0080h.

WORD 92: Master Password Revision Code
the value of the Master Password Revision Code set when the Master Password was last change. Valid values are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision is not supported.

WORD 93: Hardware configuration test results
Specification is for P-ATA. No specification for S-ATA. The value for this WORD is 0000h.

WORD 94: Current automatic acoustic management value
bit 15-8 Vendor's recommended acoustic management value
bit 7-0 Current automatic acoustic management value

This function is not supported. The value for this WORD is 0000h.

WORD 95-99: Reserved

WORD 100-103: Maximum User LBA for 48-bit Address feature set
The default values for each models are.

Drive Type	[*5] : Word 100 – 103
MK6476GSX	1,250,263,728 (4A8582B0h)
MK5076GSX	976,773,168 (3A386030h)
MK3276GSX	625,142,448 (2542EAB0h)
MK2576GSX	488,397,168 (1D1C5970h)
MK1676GSX	312,581,808 (12A19EB0h)
MK1276GSX	234,441,648 (DF94BB0h)

WORD 104-105: Reserved

WORD 106: Physical sector size / Logical Sector Size
bit 15 0 (Fixed)
bit 14 1 (Fixed)
bit 13 1= the device has more than one logical sector per physical sector
bit 12 1= the device has been formatted with a logical sector size larger than 256 words
bit 11-4 Reserved
bit 3-0 the size of the device physical sectors in power of two logical sectors
(0 → 2^0 = 1 logical sector per physical sector)

The value for this WORD is 4000h.

WORD 107: Reserved

WORD 108-111: World Wide Name
Words 108-111 contain a mandatory World Wide Name (WWN) in the NAA IEEE Registered identifier format.
Word 108 bits 15-12 shall contain 5h, indicating that the naming authority is IEEE.All other values are reserved.
Words 108 bits 11-0 and word 109 bits (15:4) shall contain the Organization Unique Identifier (OUI) (i.e.,company ID) for the device manufacturer assigned by the IEEE.
Word 109 bits (3:0), word 110, and word 111 shall contain a value assigned by the vendor that is unique for the device in the OUI domain.

WORD 112-116: Reserved

WORD 117-118 Logical Sector Size in Word

WORD 119: Commands and feature sets supported
bit 15 0 (Fixed)
bit 14 1 (Fixed)
bit 13-7 Reserved
bit 6 1=Extended Status Reporting feature set is supported
bit 5 1=Free-fall Control feature set is supported
bit 4 1=DOWNLOAD MICROCODE command requesting the offset transfer method is supported
bit 3 1=READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
bit 2 1=WRITE UNCORRECTABLE EXT command is supported
bit 1 1=Write-Read-Verify feature set is supported
bit 0 Reserved for DDT

The value for this WORD is 4018h.

WORD 120: Commands and feature sets supported or enabled
bit 15 0 (Fixed)
bit 14 1 (Fixed)
bit 13-7 Reserved
bit 6 1=Extended Status Reporting feature set is enabled
bit 5 1=Free-fall Control feature set is enabled
bit 4 1=DOWNLOAD MICROCODE command requesting the offset transfer method is supported
bit 3 1=READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
bit 2 1=WRITE UNCORRECTABLE EXT command is supported
bit 1 1=Write-Read-Verify feature set is supported
bit 0 Reserved for DDT

The value for this WORD is 4018h.

WORD 121-126: Reserved

WORD 127: Removable Media Status Notification feature set supported
This function is not supported. The value for this WORD is 0000h.

WORD 128: Security status
bit 15-9 Reserved
bit 8 the security level.
1=the security level is maximum
0=the security level is high
bit 5 1=the Enhanced security erase unit feature supported
bit 4 the security count has expired.
1=the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are aborted until receiving a power-on reset or hard reset.
bit 3 security frozen.
1=the drive is in security frozen mode.
bit 2 security locked.
1=the drive is in security locked mode.
bit 1 security enabled.
1=the security is enabled.
bit 0 security supported.
1=security is supported.

WORD 129-159: Reserved

WORD 160: CFA power mode
bit 15 Word 160 supported
bit 14 Reserved
bit 13 CFA power mode 1 is required for one or more commands implemented by the drive
bit 12 CFA power mode 1 disabled
bit 11-0 Maximum current in ma

This function is not supported. The value for this WORD is 0000h.

WORD 161-167: Reserved

WORD 168: Device Nominal Form Factor

Bits(3:0) of Word 168 indicate the nominal form factor of the device and is defined in table.

Value	Description
0h	Nominal form factor not reported
1h	5.25 type nominal form factor
2h	3.5 type nominal form factor
3h	2.5 type nominal form factor
4h	1.8 type nominal form factor
5h	Less than 1.8 type nominal form factor
6h-Fh	Reserved

The value for this WORD is 0003h.

WORD 169-175: Reserved

WORD 176-205: Current media serial number

This function is not supported. The value for this WORD is 0000h.

WORD 206: SCT Command Transport

15-12 Vendor Specific
11-6 Reserved
5 1 = SCT Command Transport Data Tables supported
4 1 = SCT Command Transport Feature Control supported
3 1 = SCT Command Transport Error Recovery Control supported
2 1 = SCT Command Transport Write Same supported
1 1 = SCT Command Transport Long Sector Access supported
0 1 = SCT Command Transport supported

The value for this WORD is 003Dh.

WORD 207-216: Reserved

WORD 217: Nominal media rotation rate

Value	Description
0000h	Rate not reported
0001h	Non-rotating media (e.g., solid state device)
0002h-0400h	Reserved
0401h-FFFEh	Nominal media rotation rate in rotations per minute (rpm) (e.g., 7200rpm = 1C20h)
FFFFh	Reserved

The value for this WORD is 1518h.

WORD 218-221: Reserved

WORD 222: Transport major version number

If not FFFFh, the device claims compliance with the Transport Standard major version(s) as indicated by bits (6:3) being set to one. Values other than 0000h and FFFFh are bit significant. Since ATA standards maintain downward compatibility, a device may set more than one bit.

The value for this WORD is 101Fh.

WORD 223-233: Reserved

WORD 234: Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command mode 03h

Word 234 contains the minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command that the ATA device accepts when using the offset transfer method.

This word is valid if bit 0 of word 83, bit 0 of word 86, and bit 4 of word 120 are set to one, indicating that the DOWNLOAD MICROCODE command using the offset transfer method is supported.

The values 0000h and FFFFh indicate no minimum is specified (i.e., that there is no minimum number of blocks).

The value for this WORD is 0001h.

WORD 235: Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command mode 03h

Word 234 contains the maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command that the ATA device shall accept when using the offset transfer method.

This word is valid if bit 0 of word 83, bit 0 of word 86, and bit 4 of word 120 are set to one, indicating that the DOWNLOAD MICROCODE command using the offset transfer method is supported.

The values 0000h and FFFFh indicate no maximum is specified (i.e., that there is no maximum number of blocks)

The value for this WORD is 0080h.

WORD 236-254: Reserved

WORD 255: Integrity word

The data structure checksum is the two s complement of the sum of all bytes in words 0 through 254 and the byte consisting of bits 7:0 in word 255. Each byte shall be added with unsigned arismetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct.

10.7.34 SET MAX (F9h)

Individual SET MAX commands are identified by the value placed in the Features register. Table 10.7-7 shows these Features register values. But regardless of Feature register value, the case this command is immediately proceded by a Read Native Max ADRESS comamnd, it is interpreted as a Set Max ADDRESS command.

Table 10.7-7 SET MAX Features register values

Value	Command
00h	Obsolete
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
05h-FFh	Reserved

10.7.34.1 Set Max Address

COMMAND CODE	1 1 1 1 1 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	Max. cylinder number	no change
HD	Max. head number	no change
SN	Max. sector number	no change
SC	00_H / 01_H (BITO: reserved bit)	na
FT	na	na
LBA	Max. LBA	no change

This command specifies the the maximum address in a range of actual drive capacity. The values set in CY, HD, SN registers indicate the maximum address that can be accessed. In CHS mode, the value of Read Native Max Address command should be set in HD, SN register. Otherwise, the value shall be ignored and the value of Read Max Address command will be used. If an LBA bit (DRV / HD register bit 6) is set, the value in LBA mode shall be set. If the address exceeding the set value is accessed , " ABORT ERROR " error will be reported. This set value affects the values of WORD 1, 54, 57, 58, 60, 61, 100-103 of IDENTIFY DEVICE command.

This command shall be immediately preceded by Read Native Max Address command. Otherwise, it will be terminated with " ABORT ERROR " .

If this command is issued twice with a volatile bit set to 1 after power-up or hardware reset, "ID Not Found error" will be reported.

If a host protected area has been established by a SET MAX ADDRESS EXT command, this command will be terminated with " ABORT ERROR " .

Volatile bit (SC register bit 0) :
If this command is issued with a volatile bit set to 1, the set value of this command is valid after power-up or hardware reset.
If this command is issued with a volatile bit cleared to 0, the set value of this command shall be cleared after hard reset or power-on and the maximam value shall be the last value with a volatile bit set to 1.

10.7.34.2 Set Max Set Password

F9h with the content of the Features register equal to 01h.

COMMAND CODE	1 1 1 1 1 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	01_H	na
LBA	na	na

This command is not immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.
This command requests a transfer of a single sector of data from the host. Table 10.7-8 defines the content of this sector of information. The password is retained by the drive until the next power cycle. When the drive accepts this command the drive is in Set_Max_Unlocked state.

Table 10.7-8 SET MAX SET PASSWORD data content

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

10.7.34.3 Set Max Lock

F9h with the content of the Features register equal to 02h.

COMMAND CODE	1 1 1 1 1 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	02_H	na
LBA	na	na

This command is not immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.
The SET MAX LOCK command sets the drive into Set_Max_Locked state. After this command is completed any other SET MAX commands except SET MAX UNLOCK and SET MAX FREEZE LOCK are rejected. The drive remains in this state until a power cycle or the acceptance of a SET MAX UNLOCK or SET MAX FREEZE LOCK command.

10.7.34.4 Set Max Unlock

F9h with the content of the Features register equal to 03h.

COMMAND CODE	1 1 1 1 1 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	03_H	na
LBA	na	na

This command is not immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it shall be interpreted as a SET MAX ADDRESS command.
This command requests a transfer of a single sector of data from the hostTable 10.7-8 defines the content of this sector of information.

The password supplied in the sector of data transferred shall be compared with the stored SET MAX password.

If the password compare fails, then the drive returns command aborted and decrements the unlock counter. On the acceptance of the SET MAX LOCK command, this counter is set to a value of five and shall be decremented for each password mismatch when SET MAX UNLOCK is issued and the drive is locked. When this counter reaches zero, then the SET MAX UNLOCK command shall return command aborted until a power cycle.

If the password compare matches, then the drive shall make a transition to the Set_Max_Unlocked state and all SET MAX commands shall be accepted.

10.7.34.5 Set Max Freeze Lock

F9h with the content of the Features register equal to 04h

COMMAND CODE	1 1 1 1 1 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	04_H	na
LBA	na	na

A SET MAX SET PASSWORD command shall previously have been successfully completed. This command is not immediately preceded by a READ NATIVE MAX ADDRESS command. If this command is immediately preceded by a READ NATIVE MAX ADDRESS command, it is interpreted as a SET MAX ADDRESS command. The SET MAX FREEZE LOCK command sets the drive to Set_Max_Frozen state. After command completion any subsequent SET MAX commands are rejected.

Commands disabled by SET MAX FREEZE LOCK are:

- SET MAX ADDRESS
- SET MAX SET PASSWORD
- SET MAX LOCK
- SET MAX UNLOCK

10.7.35 SET MAX ADDRESS EXT (37h)

COMMAND CODE	0 0 1 1 0 1 1 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	LBA(7:0)	last address
LBA Low(exp)	LBA(31:24)	last address
LBA Mid	LBA(15:8)	last address
LBA Mid(exp)	LBA(39:32)	last address
LBA High	LBA(23:16)	last address
LBA High(exp)	LBA(47:40)	last address
SC	00_H / 01_H	reserved
SC(exp)	reserved	reserved
FT	reserved	na
FT(exp)	reserved	na

This command specifies the the maximum address in a range of actual drive capacity. If the address exceeding the set value is accessed , " ABORT ERROR " error will be reported. This set value affects the values of WORD 60, 61, 100-103 of IDENTIFY DEVICE command.

This command shall be immediately preceded by Read Native Max Address EXT command. Otherwise, it will be terminated with " ABORT ERROR " .

If this command is issued twice with a volatile bit set to 1 after power-up or hardware reset, "ID Not Found error" will be reported.

If a host protected area has been established by a SET MAX ADDRESS command, this command will be terminated with " ABORT ERROR " .

Volatile bit (SC register bit 0) :
If this command is issued with a volatile bit set to 1, the set value of this command is valid after power-up or hardware reset.
If this command is issued with a volatile bit cleared to 0, the set value of this command shall be cleared after hard reset or power-on and the maximam value shall be the last value with a volatile bit set to 1.

10.7.36 Read Native Max Address (F8h)

COMMAND CODE	1 1 1 1 1 0 0 0	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	maximum cylinder number
HD	na	maximum head number
SN	na	maximum sector number
LBA	na	maximum LBA

This command sets the maximum address in CY, HD, SN register. If LBA (DRV / HD register bit6) is set to 1, the maximum address shall be LBA value.

If the 48-bit native max address is greater than 268,435,455, the Read Native Max Address command shall return a maximum value of 268,435,454.

10.7.37 Read Native Max Address EXT (27h)

COMMAND CODE	0 0 1 1 0 1 1 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	Reserved	last address
LBA Low(exp)	Reserved	last address
LBA Mid	Reserved	last address
LBA Mid(exp)	Reserved	last address
LBA High	Reserved	last address
LBA High(exp)	Reserved	last address
SC	Reserved	Reserved
SC(exp)	Reserved	Reserved
FT	Reserved	na
FT(exp)	Reserved	na

This command sets the maximum address (LBA value).

10.7.38 Set Features (EFh)

COMMAND CODE	1 1 1 0 1 1 1 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	Subcommand specific	na
HD	na	na
SN	Subcommand specific	na
SC	Mode Selection for Data Transfer(*2)	na
FT	Features(*1)	na

(*1) Features: FT register defines following selections.

02H	Enable write cache feature
03H	Select data transfer mode
05H	Enable advanced power management
10H	Enable use of Serial ATA feature(*3)
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults by soft reset
82H	Disable write cache feature
85H	Disable advanced power management
90H	Disable use of Serial ATA feature(*3)
AAH	Enable read look-ahead feature
CCH	Enable reverting to power on defaults by soft reset
others	Invalid (reporting with Aborted Command Error)

(*2)Mode selection for data transfer is specified in sector count register. Upper 5 bits show transfer mode and lower 3 bits show mode figure.

PIO default transfer mode	00000 000
PIO default transfer mode, disable IORDY	00000 001
PIO flow control transfer mode nnn	00001 nnn
Multiword DMA mode nnn	00100 nnn
Ultra DMA mode nnn	01000 nnn
Reserved	10000 nnn

PIO default mode is mode 4 flow control. DMA default mode is Multiword DMA mode 2.

The level of Advanced Power Management function is set in Sector count register.

C0h-FEh ····· Mode0 (Power save up to Low Power Idle)
80h-BFh ····· Mode1 (Power save up to Low Power Idle)
01h-7Fh ····· Mode2 (Power save up to Standby)
00h,FFh ····· Aborted

Transition time of power save is changed dynamically in Mode1 and Mode2 due to Adaptive power control function. The function level is set to Mode1 when Advanced Power Management function is disabled.

If FT register has any other value, the drive rejects the command with Abort Command error.

Default settings after power on or hard reset are:

Data transfer mode of Multiword DMA mode 2, PIO mode 4 flow control,
4 bytes ECC, look-ahead read enabled, write cache enabled, advanced power management enabled,
READ/WRITE Multiple command enabled (16 sectors)
and reverting to power on defaults by soft reset disabled.

(*3)The Sector Count register contains the specific Serial ATA feature to enable or disable. The specific Serial ATA features are defined as below.

Sector Count Value	Description
01h	Non-Zero buffer offset in DMA Setup FIS (*4)
02h	DMA Setup FIS Auto-Activate optimization (*6)
03h	Device-Initiated interface power state transitions (*7)
04h	Guaranteed In-Order Data delivery (*4)
05h	Asynchronous Notification (*5)
06h	Software Settings Preservation (*8)

(*4) Command reports Command Aborted because of not supported function.

(*5) Command reports no error but do nothing.

(*6) Disabled when power on. The enable/disable state for DMA Setup FIS Auto-Activate optimization will be preserved across software reset. The enable/disable state for Auto-Activate optimization will be reset to default state upon COMRESET.

(*7) Disabled when power on. The enable/disable state for device initiated power management will persist across software reset. The enable/disable state shall be reset to default disabled state upon COMRESET.

(*8) Enabled when power on.

The software setting that shall be preserved across COMRESET is below when the function enabled.

Command	Description
Initialize Device Parameters	Drive settings established with the Initialize Device Parameter commands
Power Management Feature Set Standby Timer	The Standby timer used in the Power Management feature set.
Security mode state	The security mode state established by Security Mode feature set commands. The drive will not transition to a different security mode state based on a COMRESET.
Security Freeze Lock	The Frozen mode setting established by the Security Freeze Lock command
Security Unlock	The unlock counter that is decremented as part of a failed Security Unlock command attempt.
Set Address Max (EXT)	The maximum LBA specified in Set Address Max od Set Address Max Ext.
Set Features (Write Cache Enable/Disable)	The write cache enable/disable setting established by the Set Features command with subcommand code of 02h and 82h.
Set Features (Set Transfer Mode)	PIO, Multiword and UDMA transfer mode setting established by the Set Features command with subcommand code of 03h.
Ser Features (Advanced Power Management Enable/Disable)	The advanced power management enable/disable setting established by the Set Feature command with subcommand code of 05h or 85h. The advanced power management level established in the Sector Count register when advanced power management is enabled will also be preserved.
Set Features (Read Look-Ahead)	The read look-ahead enable/disable setting established by the Set Features command with subcommand code of 55h or AAh
Set Multiple Mode	The block size established with the Set Multiple Mode command.
Set Features(Reverting to Defaults)	The reverting to power-on defaults enable/disable setting established by the SET FEATURES command with a subcommand code of CCh or 66h

10.7.39 SECURITY SET PASSWORD (F1h)

COMMAND CODE	1 1 1 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command requests a transfer of a sector of data from the host including the information specified in the table below. The function of this command is decided by the transferred data.
The revision code field is returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicated that the Master Password Revision Code is not supported.

Security Set Password information

Word	Content
0	Control word Bits 15-9 Reserved Bits 8 Security level 0=High 1=Maximum Bits 7-1 Reserved Bit 0 Identifier 0=set user password 1=set master password
1-16	Password (32 bytes)
17	Master Password Revision Code (valid if word 0 bit 0 = 1)
18-255	Reserved

The settings of the identifier and security level bits interact as shown in the table below.

Identifier and security level

Identifier	Level	Command result
User	High	The password supplied with the command will be saved as the new user password. The lock function will be enabled by the next power-on. The drive can then be unlocked by either the user password or the previously set master password.
Master	High	This combination will set a master password but will not enable the lock function. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.
User	Maximum	The password supplied with the command will be saved as the new user password. The lock function will be enabled by the next power-on. The drive can only be unlocked by the user password. The master password previously set is still stored in the drive but will not be used to unlock the drive.
Master	Maximum	This combination will set a master password but will not enable the lock function. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

10.7.40 SECURITY UNLOCK (F2h)

COMMAND CODE	1 1 1 1 0 0 1 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command requests the host to transfer a sector of data including ones described in the table below .

Security Unlock Information

Word	Content
0	Control word Bit 15-1 Reserved Bit 0 Identifier 0=compare user password 1=compare master password
1-16	Password (32 bytes)
17-255	Reserved

If the Identifier bit is set to master and the drive is in high security level, then the supplied password will be compared with the stored master password. If the drive is in maximum security level, then the SECURITY UNLOCK command will be rejected.

If the Identifier bit is set to user, the drive compares the supplied password with the stored user password. If the drive fails in comparing passwords, then the drive returns an abort error to the host and decrements the unlock counter. This counter is initially set to five and will be decremented for each mismatched passwords when SECURITY UNLOCK is issued and the drive is locked. When this counter is zero, SECURITY UNLOCK and SECURITY ERASE UNIT commands are aborted until the next power-on reset or hard reset. SECURITY UNLOCK commands issued when the drive is unlocked have no effect on the unlock counter.

10.7.41 SECURITY ERASE PREPARE (F3h)

COMMAND CODE	1 1 1 1 0 0 1 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

The SECURITY ERASE PREPARE command must be issued immediately before the SECURITY ERASE UNIT command to enable the drive erase and unlock. This command can prevent accidental erasure of the drive.

10.7.42 SECURITY ERASE UNIT (F4h)

COMMAND CODE	1 1 1 1 0 1 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command must be issued immediately after the SECURITY ERASE PREPARE command.

This command requests to transfer a sector of data from the host including the data specified in the following table. If the password does not match, the drive rejects the command with an Aborted command error.

Security Erase Unit Information

Word	Content
0	Control word Bit 15-2 Reserved Bit 1 Erase Mode 0=Normal Erase 1=Enhanced Erase Bit 0 Identifier 0=compare user password 1=compare master password
1-16	Password (32 bytes)
17-255	Reserved

The SECURITY ERASE UNIT command erases all user data. The SECURITY ERASE PREPARE command must be completed immediately prior to the SECURITY ERASE UNIT command, otherwise, the SECURITY ERASE UNIT command shall be aborted..

When Normal Erase mode isspecified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. When Enhanced Erase mode isspecified, the device shall write predetermined data patterns to all user data areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command disables the drive lock function, however, the master password is still stored internally within the drive and may be reactivated later when a new user password is set.

10.7.43 SECURITY FREEZE LOCK (F5h)

COMMAND CODE	1 1 1 1 0 1 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

The SECURITY FREEZE LOCK allows the drive to enter frozen mode. After the completion of this command, any other commands that update the drive lock functions are rejected. The drive recovers from the frozen mode by power-on reset or hard reset. If SECURITY FREEZE LOCK is issued when the drive is in frozen mode, the drive executes the command and remains in frozen mode.

Following commands are rejected when the drive is in SECURITY FREEZE LOCK mode.

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

10.7.44 SECURITY DISABLE PASSWORD (F6h)

COMMAND CODE	1 1 1 1 0 1 1 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	na	na

This command can be executed only when the drive is in unlocked mode. When the drive is in locked mode, the drive rejects the command with an Aborted command error.
The SECURITY DISABLE PASSWORD command requests a transfer of a single sector of data from the host including the information specified in the following table. Then the drive checks the transferred password. If the user password or the Master password match the given password, the drive disables the lock function. This command does not change the Master password which may be reactivated later by setting a user password.

Security Disable Information

Word	Content
0	Control word Bit 15-1 Reserved Bit 0 Identifier 0=compare user password 1=compare master password
1-16	Password (32 bytes)
17-255	Reserved

10.7.45 SMART Function Set (B0h)

This command has a number of separate functions which can be selected via the Feature Register when the command is issued. The subcommands and their respective codes are listed below.

Subcommand	Code
SMART READ ATTRIBUTE VALUES	D0h
SMART READ ATTRIBUTE THRESHOLDS	D1h
SMART ENABLE/DISABLE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
SMART READ LOG SECTOR	D5h
SMART WRITE LOG SECTOR	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh
SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	DBh

10.7.45.1 SMART Read Attribute values

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	na	na
FT	D0h	na

This command transfers SMART data as 512 byte data. Upon receipt of this command, the drive sets BSY, sets the SMART data on the buffer. Then, it sets DRQ, resets BSY, issue an interrupt to report that the drive is ready to transfer data.

Byte	Description
0-1	Data structure revision number
2-361	1st-30th Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364-365	Total time in seconds to complete off-line data collection activity
366	Reserved
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability 7=1 Reserved 0 1= Device error logging supported
371	Self-test Failure Checkpoint
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374-510	Reserved
511	Data structure Checksum

BYTE 0-1: Data structure revision number
0010h is set

BYTE 2-361: Individual attribute data

The following table defines 12BYTE data for each Attribue data.

Byte	Description
0	Attribute ID number 01 - FFh
1-2	Status flag bit 0 (pre-failure/advisory bit) bit 0 = 0: If attribute value is less than the threshold, the drive is in advisory condition. Product life period may expired. bit 0 = 1: If attribute value is less than the threshold, the drive is in pre-failure condition. The drive may have failure. bit 1 (on-line data collection bit) bit 1= 0: Attribute value will be changed during off-line data collection operation. bit 1= 1: Attribute value will be changed during normal operation. bit 2 (Performance Attribute bit) bit 3 (Error rate attribute bit) bit 4 (Event Count Attribute bit) bit 5 (Self-Preserving Attribute bit) bit 6-15 Reserved
3	Attribute value 01h-FDh *1 00h, FEh, FFh = Not in use 01h = Minimum value 64h = Initial value Fdh = Maximum value
4	Worst Ever normalized Attribute Value (valid values from 01h-FEh)
5-10	Raw Attribute Value Attribute specific raw data (FFFFFFFFh - reserved as saturated value)
11	Reserved (00h)

*1 For ID=199 CRC Error Count
Initial value = C8h

ID	Attribute Name
0	Indicates that entry in the data structure is not used
1	Read Error Rate
2	Throughput Performance
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time performance
9	Power-On hours Count
10	Spin Retry Count
12	Drive Power Cycle Count
191	Shock Sense Count
192	Power-off Retract Count
193	Load Cycle Count
194	Temperature
196	Re-allocated Sector Event
197	Current Pending sector Count
198	Off-Line Scan Uncorrectable Sector Count
199	CRC Error Count
220	Disk Shift
222	Loaded Hours
223	Load Retry Count
224	Load Friction
226	Load in Time
240	Write Head

BYTE 362: Off-line data collection status

Value	Definition
00h or 80h	Off-line data collection activity was never started.
01h	Reserved
02h or 82h	Off-line data collection activity was completed without error.
03h or 83h	Off-line activity in progress.
04h or 84h	Off-line data collection activity was suspended by an interrupting command from host.
05h or 85h	Off-line data collection activity was aborted by an interrupting command from host.
06h or 86h	Off-line data collection activity was aborted by the drive with a fatal error.
07h-FFh	Reserved

BYTE 363: Self-test execution status

The self-test execution status byte reports the execution status of the self-test routine.

Bits 0-3 (Percent Self-Test Remaining) The value in these bits indicates an approximation of the percent of the self-test routine remaining until completion in ten percent increments. Valid values are 0 through 9. A value of 0 indicates the self-test routine is complete. A value of 9 indicates 90% of total test time remaining.

Bits 4-7 (Self-test Execution Status) The value in these bits indicates the current Self-test Execution Status .

Self-test execution status values

Value	Description
0	The previous self-test routine completed without error or no self-test has ever been run
1	The self-test routine was aborted by the host
2	The self-test routine was interrupted by the host with a hard or soft reset
3	A fatal error or unknown test error occurred while the drive was executing its self-test routine and the drive was unable to complete the self-test routine.
4	The previous self-test completed having a test element that failed and the test element that failed is not known.
5	The previous self-test completed having the write element or the electrical element of the test failed.
6	The previous self-test completed having the servo (and/or seek) test element of the test failed.
7	The previous self-test completed having the read element of the test failed.
8-14	Reserved.
15	Self-test routine in progress.

BYTE 364-365: Total time

The time for off-line data collection operation (sec.)

BYTE 366: Reserve

BYTE 367: Off-line data collection capability

bit 0 (Execute off-line immediate implemented bit)
bit0 = 1 SMART EXECUTE OFF-LINE IMMEDIATE command supported.
bit0 = 0 SMART EXECUTE OFF-LINE IMMEDIATE command NOT supported
This bit is set to 1
bit 1 (enable/disable automatic off-line implemented bit)
bit0 = 1 SMART ENABLE/DISABLE AUTOMATIC OFF-LINE command supported.
bit0 = 0 SMART ENABLE/DISABLE AUTOMATIC OFF-LINE command NOT supported
This bit is set to 1
bit 2 (abort/restart off-line by host)
bit2 = 1 If another command is issued, off-line data collection operation is aborted.
bit2 = 0 If another command is issued, off-line data collection operation is interrupted and then the operation will be continued.

bit 3 (off-line read scanning implemented bit)
If this bit is cleared to zero, the drive does not support off-line read scanning. If this bit is set to one, the drive supports off-line read scanning. This bit is set to 1.
bit 4 (self-test implemented bit)
If this bit is cleared to zero, the drive does not implement the Short and Extended self-test routines. If this bit is set to one, the drive implements the Short and Extended self-test routines. This bit is set to 1.
bits 5 (reserved).
This bit is set to 0.
bits 6 (Selective self-test implemented bit)
If this bit is cleared to zero, the drive does not implement the Selective self-test routine. If this bit is set to one, the drive implements the Selective self-test routine. This bit is set to 1.
bits 7 (reserved).
This bit is set to 0.

BYTE 368-369: SMART capability
bit 0 (power mode SMART data saving capabilities bit)
bit0 = 1 SMART data is saved before Power save mode changes.
bit0 = 0 SMART data is NOT saved before Power save mode changes.
This bit is set to 1
bit 1 (SMART data autosave after event capability bit)
This bit is fixed to 1
bit 2-15 Reserved

BYTE 370 Error logging capability
BYTE 371 Self-test Failure Checkpoint
This byte reports the checkpoint when previos self-test failed.
BYTE 372-373: Self-test routine recommended polling time
The self-test routine recommended polling time is equal to the number of minutes that is the minimum recommended time before which the host should first poll for test completion status. Actual test time could be several times this value. Polling before this time could extend the self-test execution time or abort the test depending on the state of bit 2 of the off-line data capability bits.

BYTE 374-510: Reserved
BYTE 511: Data structure checksum
Checksum of the first 511 byte

10.7.45.2 SMART Read Attribute thresholds

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	na	na
FT	D1h	na

This command transfers attribute thresholds of the drive as 512 byte data.
Upon receipt of the command, the drive sets BSY, sets SMART data on the buffer, then, sets DRQ, resets BSY and issues an interrupt to report to the host that data transfer is ready.

Byte	Descriptions
0-1	Data structure revision number
2-361	1st-30th Individual attribute threshold data
362-510	Reserved
511	Data structure checksum

BYTE 0-1: Data structure revision number
The value for this byte is 0010h.

BYTE 2-361: Individual attribute threshold data
Individual attribute threshold data consists of 12 byte data. (See the following fig.)

Byte	Description
0	Attribute ID number 01h - FFh
1	Attribute Threshold 00h= Always passed 01h= Minimum value FDh= Maximum value FEh, FFh= Not in use
2-11	Reserved

BYTE 362-510: Reserved
BYTE 511: Data structure checksum
The checksum of the first 511 byte.

10.7.45.3 SMART Enable Disable Attribute Autosave

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	00h/F1h	na
FT	D2h	na

This command enables and disables the attribute autosave function within the drive. This command allow the drive to automatically save its updated attribute values to the attribute data sector at mode transition or cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) will be preserved by the drive across power cycles.

A value of zero written by the host into the drive's Sector Count register before issuing this command may disable this function. Disabling this feature does not preclude the drive from saving attribute values to the attribute data sector during other normal save operations.

A value of F1h written by the host into the drive's Sector Count register before issuing this command will cause this function to be enabled. Any other non-zero value written by the host into this register before issuing this command will not change the state of the attribute autosave feature.

Upon receipt of the command from the host, the drive sets BSY, enables or disables the autosave function , clears BSY and asserts INTRQ.

10.7.45.4 SMART Save Attribute Values

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	na	na
FT	D3h	na

This command immediately saves changed attribute values. Upon receipt of the command, the drive sets BSY, saves the attribute values, clears BSY and issues an interrupt.

10.7.45.5 SMART Execute Off-line Immediate

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	no change
HD	Na	na
SN	Subcommand specific	na
SC	Na	na
FT	D4h	na

This command causes the drive to immediately initiate the activities that collect SMART data in an off-line mode and then save this data to the drive 's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.
The sector Number register will be set to specify the operation to be executed.

SMART EXECUTE OFF-LINE IMMEDIATE Sector Number register values

Value	Description of subcommand to be executed
0	Execute SMART off-line routine immediately in off-line mode
1	Execute SMART Short self-test routine immediately in off-line mode
2	Execute SMART Extended self-test routine immediately in off-line mode
3	Reserved
4	Execute SMART Selective self-test routine immediately in off-line mode
5-126	Reserved
127	Abort off-line mode self-test routine
128	Reserved
129	Execute SMART Short self-test routine immediately in captive mode
130	Execute SMART Extended self-test routine immediately in captive mode
131	Reserved
132	Execute SMART Selective self-test routine immediately in captive mode
133-255	Reserved

10.7.45.5.1 Off-line mode

The following describes the protocol for executing a SMART EXECUTE OFF-LINE IMMEDIATE subcommand routine (including a self-test routine) in the off-line mode.

a) The drive executes command completion before executing the subcommand routine.
b) After clearing BSY to zero and setting DRDY to one after receiving the command, the drive will not set BSY nor clear DRDY during execution of the subcommand routine.
c) If the drive is in the process of performing the subcommand routine and is interrupted by any new command from the host except a SLEEP, SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE, STANDBY IMMEDIATE or IDLE IMMEDIATE command, the drive suspends or aborts the subcommand routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command from the host the drive may re-initiate or resume the subcommand routine without any additional commands from the host.
d) If the drive is in the process of performing a subcommand routine and is interrupted by a SLEEP command from the host, the drive will suspend or abort the subcommand routine and execute the SLEEP command. If the drive is in the process of performing any self-test routine and is interrupted by a SLEEP command from the host, the drive will abort the subcommand routine and execute the SLEEP command.
e) If the drive is in the process of performing the subcommand routine and is interrupted by a SMART DISABLE OPERATIONS command from the host, the drive will abort the subcommand routine and service the host within two seconds after receipt of the command.
f) If the drive is in the process of performing the subcommand routine and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the drive will abort the subcommand routine and service the host within two seconds after receipt of the command. The drive will then service the new SMART EXECUTE OFF-LINE IMMEDIATE subcommand.

g) If the drive is in the process of performing the subcommand routine and is interrupted by a STANDBY IMMEDIATE or IDLE IMMEDIATE command from the host, the drive will suspend or abort the subcommand routine, and service the host within two seconds after receipt of the command. After receiving a new command that causes the drive to exit a power saving mode, the drive will initiate or resume the subcommand routine without any additional commands from the host unless these activities were aborted by the host.
h) While the drive is performing the subcommand routine it will not automatically change power states (e.g., as a result of its Standby timer expiring).

If an error occurs while a drive is performing a self-test routine the drive may discontinue the testing and place the test results in the Self-test execution status byte.

10.7.45.5.2 Captive mode

When executing a self-test in captive mode, the drive sets BSY to one and executes the self-test routine after receipt of the command. At the end of the routine the drive places the results of this routine in the Self-test execution status byte and executes command completion. If an error occurs while a drive is performing the routine the drive may discontinue its testing, place the results of this routine in the Self-test execution status byte, and complete the command.

10.7.45.5.3 SMART off-line routine

This routine will only be performed in the off-line mode. The results of this routine are placed in the Off-line data collection status byte.

10.7.45.5.4 SMART Short self-test routine

Depending on the value in the Sector Number register, this self-test routine may be performed in either the captive or the off-line mode. This self-test routine should take on the order of ones of minutes to complete.

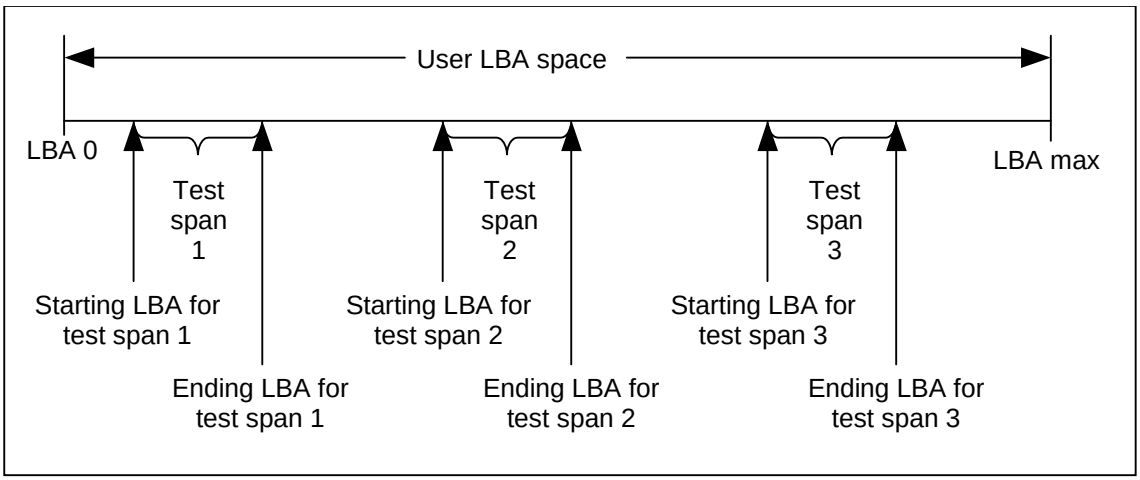
10.7.45.5.5 SMART Extended self-test routine

Depending on the value in the Sector Number register, this self-test routine may be performed in either the captive or the off-line or mode. This self-test routine should take on the order of tens of minutes to complete.

10.7.45.5.6 SMART Selective self-test routine

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This self-test routine shall include the initial tests performed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress.

The user may choose to do read scan only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. The following figure shows an example of a Selective self-test definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.



Selective self-test test span example

After the scan of the selected spans described above, a user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the drive shall then set the off-line scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall completed as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the drive is powered-down before the off-line scan is completed, the off-line scan shall resume when the drive is again powered up. From power-up, the resumption of the scan shall be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion.

During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log.

A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log (see 10.7.45.6.5). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the drive is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

10.7.45.6 SMART Read Log Sector

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	Log Sector Address	na
SC	Number of sectors to read	na
FT	D5h	na

This command returns the indicated log sector contents to the host.
Sector count -specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log, regardless of the sector count requested.
Sector number indicates the log sector to be returned as described in the following Table.

Log Sector

Log sector address	Content	R/W
00h	Log directory	RO
01h	SMART error log	RO
02h	Comprehensive SMART error log	RO
03h	Extended comprehensive SMART error log	See Note
04h-05h	Reserved	RO
06h	SMART self-test log	RO
07h	Extended SMART self-test log	See Note
08h	Reserved	RO
09h	Selective self-test log	RO
0Ah-7Fh	Reserved	RO
80h-9Fh	Host vendor specific	R/W
A0h-FFh	Reserved	VS

Key –
RO –Log is read only by the host.
R/W –Log is read or written by the host.
VS –Log is vendor specific thus read/write ability is vendor specific.

NOTE - Log addresses 03hand 07h are used by the READ LOG EXT and WRITE LOG EXT commands. If these log addresses are used with the SMART READ LOG command, the drive shall return command aborted.

10.7.45.6.1 SMART log directory

The following table defines the 512 bytes that make up the SMART Log Directory.The SMART Log Directory is SMART Log address zero, and is defined as one sector long.

SMART Log Directory

Byte	Descriptions
0-1	SMART Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
…	…
510	Number of sectors in the log at log address 255
511	Reserved

The value of the SMART Logging Version word is set to 01h. Then the drive supports multi-sector SMART logs. In addition, if the drive supports multi-sector logs, then the logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

10.7.45.6.2 Summary error log sector

The following Table defines the 512 bytes that make up the SMART summary error log sector.

SMART summary error log sector

Byte	Descriptions
0	SMART error log version
1	Error log index
2-91	First error log data structure
92-181	Second error log data structure
182-271	Third error log data structure
272-361	Fourth error log data structure
362-451	Fifth error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

10.7.45.6.2.1 Error log version

The value of the SMART error log version byte is set to 01h.

10.7.45.6.2.2 Error log data structure

An error log data structure will be presented for each of the last five errors reported by the drive. These error log data structure entries are viewed as a circular buffer. That is, the first error will create the first error log data structure; the second error, the second error log structure; etc. The sixth error will create an error log data structure that replaces the first error log data structure; the seventh error replaces the second error log structure, etc. The error log pointer indicates the most recent error log structure. If fewer than five errors have occurred, the unused error log structure entries will be zero filled. The following table describes the content of a valid error log data structure.

Error log data structure

Byte	Descriptions
n –n+11	First command data structure
N+12 –n+23	Second command data structure
N+24 –n+35	Third command data structure
N+36 – n+47	Fourth command data structure
N+48 – n+59	Fifth command data structure
N+60 – n+89	Error data structure

10.7.45.6.2.3 Command data structure

The fifth command data structure will contain the command or reset for which the error is being reported. The fourth command data structure should contain the command or reset that preceded the command or reset for which the error is being reported, the third command data structure should contain the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures will be zero filled, for example, if only three commands and resets preceded the command or reset for which the error is being reported, the first command data structure will be zero filled. In some drive s, the hardware implementation may preclude the drive from reporting the commands that preceded the command for which the error is being reported or that preceded a reset. In this case, the command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure will be as shown in the following Table.

Command data structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
n+1	Content of the Features register when the Command register was written.
n+2	Content of the Sector Count register when the Command register was written.
n+3	Content of the Sector Number register when the Command register was written.
n+4	Content of the Cylinder Low register when the Command register was written.
n+5	Content of the Cylinder High register when the Command register was written.
n+6	Content of the Device/Head register when the Command register was written.
n+7	Content written to the Command register.
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

10.7.45.6.2.4 Error data structure

The error data structure will contain the error description of the command for which an error was reported as described in the following table.

Error data structure

Byte	Descriptions
N	Reserved
n+1	Content of the Error register after command completion occurred.
n+2	Content of the Sector Count register after command completion occurred.
n+3	Content of the Sector Number register after command completion occurred.
n+4	Content of the Cylinder Low register after command completion occurred.
n+5	Content of the Cylinder High register after command completion occurred.
n+6	Content of the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 - n+26	Extended error information
n+27	State
n+28	Life timestamp (least significant byte)
n+29	Life timestamp (most significant byte)

Extended error information will be vendor specific.

State will contain a value indicating the state of the drive when command was written to the Command register or the reset occurred as described in the following Table.

State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique
The value of x is vendor specific and may be different for each state.	

Sleep indicates the reset for which the error is being reported was received when the drive was in the Sleep mode.

Standby indicates the command or reset for which the error is being reported was received when the drive was in the Standby mode.

Active/Idle with BSY cleared to zero indicates the command or reset for which the error is being reported was received when the drive was in the Active or Idle mode and BSY was cleared to zero.

Executing SMART off-line or self-test indicates the command or reset for which the error is being reported was received when the device was in the process of executing a SMART off-line or self-test.

Life timestamp will contain the power-on lifetime of the drive in hours when command completion occurred.

10.7.45.6.2.5 Device error count

The device error count field will contain the total number of errors attributable to the drive that have been reported by the drive during the life of the drive. These errors will include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count will not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the drive or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count will remain at the maximum value when additional errors are encountered and logged.

10.7.45.6.2.6 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte will be added with unsigned arithmetic, and overflow will be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

10.7.45.6.3 Comprehensive error log

The following defines the format of each of the sectors that comprise the SMART comprehensive error log. The SMART Comprehensive error log provides logging for 28-bit addressing only. For 48-bit addressing see 10.7.47.2 . The size of the SMART comprehensive error log is 51 sectors. All multi-byte fields shown in this structure follow the byte ordering described in 10.7.45.6.2.3 and 10.7.45.6.2.4. The comprehensive error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Comprehensive error log data structures shall not include errors attributed to the receipt of faulty commands such as command codes not supported by the drive or requests with invalid parameters or invalid addresses.

Comprehensive error log

Byte	First sector	Subsequent sectors
0	SMART error log version	Reserved
1	Error log index	Reserved
2-91	First error log data structure	Data structure 5n+1
92-181	Second error log data structure	Data structure 5n+2
182-271	Third error log data structure	Data structure 5n+3
272-361	Fourth error log data structure	Data structure 5n+4
362-451	Fifth error log data structure	Data structure 5n+5
452-453	Device error count	Reserved
454-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

10.7.45.6.3.1 Error log version

The value of the error log version byte shall be set to 01h.

10.7.45.6.3.2 Error log index

The error log index indicates the error log data structure representing the most recent error. If there have been no error log entries, the error log index is set to zero. Valid values for the error log index are zero to 255.

10.7.45.6.3.3 Error log data structure

The error log is viewed as a circular buffer. The drive may support from two to 51 error log sectors. When the last supported error log sector has been filled, the next error shall create an error log data structure that replaces the first error log data structure in sector zero. The next error after that shall create an error log data structure that replaces the second error log data structure in sector zero. The sixth error after the log has filled shall replace the first error log data structure in sector one, and so on.

The error log index indicates the most recent error log data structure. Unused error log data structures shall be filled with zeros.

The content of the error log data structure entries is defined in 10.7.45.6.2.2.

10.7.45.6.3.4 Device error count

The device error count field is defined in 10.7.45.6.2.5.

10.7.45.6.3.5 Data structure checksum

The data structure checksum is defined in 10.7.45.6.2.6.

10.7.45.6.4 Self-test log sector

The following Table defines the 512 bytes that make up the SMART self-test log sector.

Self-test log data structure

Byte	Descriptions
0-1	Self-test log data structure revision number
2-25	First descriptor entry
26-49	Second descriptor entry
.....	.....
482-505	Twenty-first descriptor entry
506-507	Vendor specific
508	Self-test index
509-510	Reserved
511	Data structure checksum

10.7.45.6.4.1 Self-test log data structure revision number

The value of the self-test log data structure revision number is set to 0001h.

10.7.45.6.4.2 Self-test log descriptor entry

This log is viewed as a circular buffer. The first entry will begin at byte 2, the second entry will begin at byte 26, and so on until the twenty-second entry, that will replace the first entry. Then, the twenty-third entry will replace the second entry, and so on. If fewer than 21 self-tests have been performed by the drive, the unused descriptor entries will be filled with zeroes.

The content of the self-test descriptor entry is shown in the following Table.

Self-test log descriptor entry

Byte	Descriptions
n	Content of the Sector Number
n+1	Content of the self-test execution status
n+2	Life timestamp (least significant byte).
n+3	Life timestamp (most significant byte).
n+4	Content of the self-test failure checkpoint
n+5	Failing LBA(least significant byte).
n+6	Failing LBA(next least significant byte).
n+7	Failing LBA(next most significant byte).
n+8	Failing LBA(most significant byte).
n+9 - n+23	Vendor specific.

Content of the Sector Number register will be the content of the Sector Number register when the nth self-test subcommand was issued.

Content of the self-test execution status byte will be the content of the self-test execution status byte when the nth self-test was completed

Life timestamp will contain the power-on lifetime of the drive in hours when the nth self-test subcommand was completed.

Content of the self-test failure checkpoint byte will be the content of the self-test failure checkpoint byte when the nth self-test was completed.

The failing LBA will be the LBA of the uncorrectable sector that caused the test to fail. If the drive encountered more than one uncorrectable sector during the test, this field will indicate the LBA of the first uncorrectable sector encountered. If the test passed or the test failed for some reason other than an uncorrectable sector, the value of this field is undefined.

10.7.45.6.4.3 Self-test index

The self-test index will point to the most recent entry. Initially, when the log is empty, the index will be set to zero. It will be set to one when the first entry is made, two for the second entry, etc., until the 22nd entry, when the index will be reset to one.

10.7.45.6.4.4 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte will be added with unsigned arithmetic, and overflow will be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

10.7.45.6.5 Selective self-test log

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the content of the Selective self-test log.

Selective self-test log

Byte	Description	Read/write
0-1	Data structure revision number	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags	R/W
504-507	Vendor specific	Vendor specific
508-509	Selective self-test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

10.7.45.6.5.1 Data structure revision number

The value of the data structure revision number filed shall be 01h. This value shall be written by the host and returned unmodified by the drive.

10.7.45.6.5.2 Test span definition

The Selective self-test log provides for the definition of up to five test spans. The starting LBA for each test span is the LBA of the first sector tested in the test span and the ending LBA for each test span is the last LBA tested in the test span. If the starting and ending LBA values for a test span are both zero, a test span is not defined and not tested. These values shall be written by the host and returned unmodified by the drive.

10.7.45.6.5.3 Current LBA under test

The Current LBA under test field shall be written with a value of zero by the host. As the self-test progresses, the drive shall modify this value to contain the beginning LBA of the 65,536 sector block currently being tested. When the self-test including the off-line scan between test spans has been completed, a zero value is placed in this field.

10.7.45.6.5.4 Current span under test

The Current span under test field shall be written with a value of zero by the host. As the self-test progresses, the drive shall modify this value to contain the test span number of the current span being tested. If an off-line scan between test spans is selected, a value greater then five is placed in this field during the off-line scan. When the self-test including the off-line scan between test spans has been completed, a zero value is placed in this field.

10.7.45.6.5.5 Feature flags

The Feature flags define the features of Selective self-test to be executed (see following table).

Selective self-test feature flags

Bit	Description
0	Vendor specific
1	When set to one, perform off-line scan after selective test.
2	Vendor specific
3	When set to one, off-line scan after selective test is pending.
4	When set to one, off-line scan after selective test is active.
5-15	Reserved.

Bit (1) shall be written by the host and returned unmodified by the drive. Bits (4:3) shall be written as zeros by the host and the drive shall modify them as the test progresses.

10.7.45.6.5.6 Selective self-test pending time

The selective self-test pending time is the time in minutes from power-on to the resumption of the off-line testing if the pending bit is set. At the expiration of this time, sets the active bit to one, and resumes the off-line scan that had begun before power-down.

10.7.45.6.5.7 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte will be added with unsigned arithmetic, and overflow will be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

10.7.45.7 SMART Write Log Sector

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	Log Sector Address	na
SC	Number of sectors to write	na
FT	D6h	na

This command writes an indicated number of 512 byte data sectors to the indicated log.

10.7.45.8 SMART Enable Operations

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	na	na
FT	D8h	na

This command enables access to all SMART capabilities of the drive. Prior to receipt of this command, Parameters for drive failure prediction are neither monitored nor saved by the drive. The state of SMART (either enabled or disabled) will be preserved by the drive across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands don't affect any of the parameters for drive failure prediction.

Upon receipt of this command from the host, the drive sets BSY, enables SMART capabilities and functions, clears BSY and asserts INTRQ.

10.7.45.9 SMART Disable Operations

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	na	na
FT	D9h	na

This command disables all SMART capabilities within the drive including any and all timer functions related exclusively to this function. After receipt of this command the drive may disable all SMART operations. Parameters for drive failure prediction will no longer be monitored or saved by the drive. The state of SMART (either enabled or disabled) will be preserved by the drive across power cycles.

Upon receipt of the SMART DISABLE OPERATIONS command from the host, the drive sets BSY, disables SMART capabilities and functions, clears BSY and asserts INTRQ.

After receipt of this command by the drive, all other SMART commands, except for SMART ENABLE OPERATIONS, are disabled and invalid and will be aborted by the drive (including SMART DISABLE OPERATIONS commands) with an Aborted command error.

10.7.45.10 SMART Return Status

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	C24Fh/2CF4h
HD	na	na
SN	na	na
SC	na	na
FT	DAh	na

If an impending failure is not predicted, the drive sets the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If an impending failure is predicted, the drive sets the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

This command is used to communicate the reliability status of the drive to the host's request. Upon receipt of this command the drive sets BSY, saves any parameters monitored by the drive to non-volatile memory and checks the drive condition.

10.7.45.11 SMART Enable/Disable Automatic Off-line

COMMAND CODE	1 0 1 1 0 0 0 0	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	C24Fh	na
HD	na	na
SN	na	na
SC	00h/F8h	na
FT	DBh	na

This subcommand enables and disables the optional feature that causes the drive to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the drive's non-volatile memory. This subcommand may either cause the drive automatically initiate or resume performance of its off-line data collection activities; or this command may cause the automatic off-line data collection feature to be disabled.

A value of zero written by the host into the drive's Sector Count register before issuing this subcommand will cause the feature to be disabled. Disabling this feature does not preclude the drive from saving attribute values to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the drive's Sector Count register before issuing this command will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific.

Automatic off-line data collection is executed every 24 power-on hours.

10.7.46 Read Log EXT (2Fh)

10.7.47 Read Log DMA EXT (47h)

COMMAND CODE	0 0 1 0 1 1 1 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	Log address	Reserved
LBA Low(exp)	reserved	Reserved
LBA Mid	Sector Offset(7:0)	Reserved
LBA Mid(exp)	Sector Offset(15:8)	Reserved
LBA High	reserved	Reserved
LBA High(exp)	reserved	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	Reserved	na
FT(exp)	Reserved	na

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred.

Sector Count - Specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.

LBA Low - Specifies the log to be returned as described in the following Table.

LBA Mid - Specifies the first sector of the log to be read.

Log Sector

Log sector address	Content	R/W
00h	Log directory	RO
01h	SMART error log	See Note
02h	Comprehensive SMART error log	See Note
03h	Extended comprehensive SMART error log	RO
04h-05h	Reserved	-
06h	SMART self-test log	See Note
07h	Extended SMART self-test log	RO
08h	Reserved	-
09h	Selective self-test log	See Note
0Ah-0Fh	Reserved	-
10h	Native Command Queue error log	RO
11h	Phy Event Counters	RO
12h-7Fh	Reserved	-
80h-9Fh	Host vendor specific	R/W
A0h-FFh	Reserved	-

Key –
RO –Log is read only by the host.
R/W –Log is read or written by the host.

NOTE - Log addresses 01h,02,,06h and 09h are used by the SMART READ LOG command commands. If these log addresses are used with the READ LOG EXT command, the drive shall return command aborted.

10.7.47.1 General Purpose Log Directory

The following table defines the 512 bytes that make up the General Purpose Log Directory.

General Purpose Log Directory

Byte	Descriptions
0-1	General Purpose Logging Version
2	Number of sectors in the log at log address 01h (7:0)
3	Number of sectors in the log at log address 01h (15:8)
4	Number of sectors in the log at log address 02h (7:0)
5	Number of sectors in the log at log address 02h (15:8)
…	
32	1 if Native Command Queuing is supported. 0 if Native Command Queuing is not supported.
33	0
34	1 if Phy Event Counters are supported. 0 if Phy Event Counters are not supported.
35	0
….	
256	10h sectors in the log at log address 80h
257	00h sectors in the log at log address 80h
…	
510-511	Number of sectors in the log at log address FFh

The value of the General Purpose Logging Version word is 0001h.

The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

10.7.47.2 Extended Comprehensive SMART Error log

The fpllowing table defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. The size of the Extended Comprehensive SMART error log is 64 sectors. Error log data structures shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. Error log data structures shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the drive or requests with invalid parameters or invalid addresses.

All 28-bit entries contained in the Comprehensive SMART log, defined under section 10.7.45.6.5, shall also be included in the Extended Comprehensive SMART error log with the 48-bit entries.

Extended Comprehensive SMART error log

Byte	First sector	Subsequent sectors
0	SMART error log version	Reserved
1	Reserved	Reserved
2	Error log index (7:0)	Reserved
3	Error log index (15:8)	Reserved
4-127	First error log data structure	Data structure 4n+1
128-251	Second error log data structure	Data structure 4n+2
252-375	Third error log data structure	Data structure 4n+3
376-499	Fourth error log data structure	Data structure 4n+4
500-501	Device error count	Reserved
502-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

10.7.47.2.1 Error log version

The value of the SMART error log version byte is 01h.

10.7.47.2.2 Error log index

The error log index indicates the error log data structure representing the most recent error. If there have been no error log entries, the error log index is cleared to zero. Valid values for the error log index are zero to 255.

10.7.47.2.3 Extended Error log data structure

The error log is viewed as a circular buffer. When the last supported error log sector has been filled, the next error shall create an error log data structure that replaces the first error log data structure in sector zero. The next error after that shall create an error log data structure that replaces the second error log data structure in sector zero. The fifth error after the log has filled shall replace the first error log data structure in sector one, and so on.

The error log index indicates the most recent error log data structure. Unused error log data structures shall be filled with zeros.

The content of the error log data structure entries is defined in the following table.

Extended Error log data structure

Byte	Descriptions
n thru n+17	First command data structure
n+18 thru n+35	Second command data structure
n+36 thru n+53	Third command data structure
n+54 thru n+71	Fourth command data structure
n+72 thru n+89	Fifth command data structure
n+90 thru n+123	Error data structure

10.7.47.2.3.1 Command data structure

The fifth command data structure shall contain the command or reset for which the error is being reported. The fourth command data structure should contain the command or reset that preceded the command or reset for which the error is being reported, the third command data structure should contain the command or reset preceding the one in the fourth command data structure, etc. If fewer than four commands and resets preceded the command or reset for which the error is being reported, the unused command data structures shall be zero filled, for example, if only three commands and resets preceded the command or reset for which the error is being reported, the first command data structure shall be zero filled. In some drive, the hardware implementation may preclude the drive from reporting the commands that preceded the command for which the error is being reported or that preceded a reset. In this case, the command data structures are zero filled.

If the command data structure represents a command or software reset, the content of the command data structure shall be as shown in the following table. If the command data structure represents a hardware reset, the content of byte n shall be FFh, the content of bytes n+1 through n+13 are vendor specific, and the content of bytes n+14 through n+17 shall contain the timestamp.

Command data structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written.
N+1	Content of the Features register (7:0) when the Command register was written. (see note)
n+2	Content of the Features register (15:8) when the Command register was written.
N+3	Content of the Sector Count register (7:0) when the Command register was written.
N+4	Content of the Sector Count register (15:8) when the Command register was written.
N+5	Content of the LBA Low register (7:0) when the Command register was written.
N+6	Content of the LBA Lowregister (15:8) when the Command register was written.
N+7	Content of the LBA Mid register (7:0) when the Command register was written.
N+8	Content of the LBA Mid register (15:8) when the Command register was written.
N+9	Content of the LBA High register (7:0) when the Command register was written.
N+10	Content of the LBA High register (15:8) when the Command register was written.
N+11	Content of the Device/Head register when the Command register was written.
N+12	Content written to the Command register.
N+13	Reserved
n+14	Timestamp (least significant byte)
n+15	Timestamp (next least significant byte)
n+16	Timestamp (next most significant byte)
n+17	Timestamp (most significant byte)
NOTE - bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register.	

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

10.7.47.2.3.2 Error data structure

The error data structure shall contain the error description of the command for which an error was reported as described in the following table. If the error was logged for a hardware reset, the content of bytes n+1 through n+11 shall be vendor specific and the remaining bytes shall be as defined in the following table.

Error data structure

Byte	Descriptions
n	Reserved
n+1	Content of the Error register after command completion occurred.
N+2	Content of the Sector Count register (7:0) after command completion occurred. (see note)
n+3	Content of the Sector Count register (15:8) after command completion occurred. (see note)
n+4	Content of the LBA Low register (7:0) after command completion occurred.
N+5	Content of the LBA Low register (15:8) after command completion occurred.
N+6	Content of the LBA Mid register (7:0) after command completion occurred.
N+7	Content of the LBA Mid register (15:8) after command completion occurred.
N+8	Content of the LBA High register (7:0) after command completion occurred.
N+9	Content of the LBA High register (15:8) after command completion occurred.
N+10	Content of the Device/Head register after command completion occurred.
N+11	Content written to the Status register after command completion occurred.
N+12 through n+30	Extended error information
n+31	State
n+32	Life timestamp (least significant byte)
n+33	Life timestamp (most significant byte)
NOTE - bits (7:0) refer to the contents if the register were read with bit 7 of the Device Control register cleared to zero. Bits (15:8) refer to the contents if the register were read with bit 7 of the Device Control register set to one.	

State shall contain a value indicating the state of the drive when the command was written to the Command register or the reset occurred as described in the following table.

State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xFh	Reserved
The value of x is vendor specific and may be different for each state.	

Sleep indicates the reset for which the error is being reported was received when the drive was in the Sleep mode.

Standby indicates the command or reset for which the error is being reported was received when the drive was in the Standby mode.

Active/Idle with BSY cleared to zero indicates the command or reset for which the error is being reported was received when the drive was in the Active or Idle mode and BSY was cleared to zero.

Executing SMART off-line or self-test indicates the command or reset for which the error is being reported was received when the drive was in the process of executing a SMART off-line or self-test.

Life timestamp shall contain the power-on lifetime of the drive in hours when command completion occurred.

10.7.47.2.4 Device error count

The device error count field shall contain the total number of errors attributable to the drive that have been reported by the drive during the life of the drive. These errors shall include UNC errors, IDNF errors for which the address requested was valid, servo errors, write fault errors, etc. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the drive or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached, the count shall remain at the maximum value when additional errors are encountered and logged.

10.7.47.2.5 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes will be zero when the checksum is correct. The checksum is placed in byte 511.

10.7.47.3 Extended Self-test log sector

The following table defines the format of each of the sectors that comprise the Extended SMART Self-test log. The size of the self-test log is 1 sectors.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined under section 10.7.45.6.4 shall also be included in the Extended SMART self-test log with all 48-bit entries.

Extended Self-test log data structure

Byte	First sector	Subsequent sectors
0	Self-test log data structure revision number	Reserved
1	Reserved	Reserved
2	Self-test descriptor index (7:0)	Reserved
3	Self-test descriptor index (15:8)	Reserved
4-29	Descriptor entry 1	Descriptor entry 19n+1
30-55	Descriptor entry 2	Descriptor entry 19n+2
….	....	....
472-497	Descriptor entry 19	Descriptor entry 19n+19
498-499	Vendor specific	Vendor specific
500-510	Reserved	Reserved
511	Data structure checksum	Data structure checksum
n is the sector number within the log. The first sector is sector zero		

This log is viewed as a circular buffer. The first entry will begin at byte 4, the second entry will begin at byte 30 and so on until the 20th entry, that will replace the first entry. Then, the 21st entry will replace the second entry, and so on. If fewer than 19 self-tests have been performed by the drive, the unused descriptor entries will be filled with zeroes.

10.7.47.3.1 Self-test descriptor index

The Self-test descriptor index indicates the most recent self-test descriptor. If there have been no self-tests, the Self-test descriptor index is set to zero. Valid values for the Self-test descriptor index are zero to 19.

10.7.47.3.2 Self-test log data structure revision number

The value of the self-test log data structure revision number is 01h.

10.7.47.3.3 Extended Self-test log descriptor entry

The content of the self-test descriptor entry is shown in the following table..

Extended Self-test log descriptor entry

Byte	Descriptions
n	Content of the LBA Low register.
n+1	Content of the self-test execution status byte.
n+2	Life timestamp (least significant byte).
n+3	Life timestamp (most significant byte).
n+4	Content of the self-test failure checkpoint byte.
n+5	Failing LBA (7:0).
n+6	Failing LBA (15:8).
n+7	Failing LBA (23:16).
n+8	Failing LBA (31:24).
n+9	Failing LBA (39:32).
n+10	Failing LBA (47:40).
n+11 - n+25	Vendor specific.

Content of the LBA Low register shall be the content of the LBA Low register when the nth self-test subcommand was issued (see 10.7.45.5).

Content of the self-test execution status byte shall be the content of the self-test execution status byte when the nth self-test was completed (see 10.7.45.5).

Life timestamp shall contain the power-on lifetime of the drive in hours when the nth self-test subcommand was completed.

Content of the self-test failure checkpoint byte may contain additional information about the self-test that failed.

The failing LBA shall be the LBA of the sector that caused the test to fail. If the drive encountered more than one failed sector during the test, this field shall indicate the LBA of the first failed sector encountered. If the test passed or the test failed for some reason other than a failed sector, the value of this field is undefined.

10.7.47.3.4 Data structure checksum

The data structure checksum is the two's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

10.7.47.4 Native Command Queue Error Log

The following table defines the format of the Native Command Queue error log

Byte	7	6	5	4	3	2	1	0
0	NQ	UNL	R	TAG				
1	Reserved							
2	Status							
3	Error							
4	Sector Number							
5	Cylinder Low							
6	Cylinder High							
7	Dev/Head							
8	Sector Number Exp							
9	Cylinder Low Exp							
10	Cylinder High Exp							
11	Reserved							
12	Sector Count							
13	Sector Count Exp							
14	Reserved							
15	Reserved							
16	Reserved							
17	Reserved							
18	Reserved							
19	Reserved							
20-255	Reserved							
256-510	Vender Specific							
511	Data Structure Checksum							

TAG — If the NQ bit is cleared, the TAG field contains the TAG corresponding to the Queued command that failed.

UNL — If set to one indicates that the error condition was a result of receiving an IDLE IMMEDIATE command with the Unload Feature specified. If cleared to zero, the reason for the error was not due to reception of an IDLE IMMEDIATE command with the Unload Feature specified. If the last command received was an Unload Immediate, the device shall not load the heads to the media when executingthe READ LOG EXT command for log page 10h.
If set to one, the NQ bit shall also be set to one to indicate the failure was due to reception of a non-queued command. When set to one, the value of the Status, Error, and LBA Low fields (bytes 3-5) in the log page shall be set as follows:

Status: BSY bit shall be cleared to zero and ERR bit shall be set to one
Error: ABRT bit shall be set to one
LBA Low: Shall be set to C4h if the unload has completed successfully.
Shall be set to 4Ch if the unload was not accepted or has failed.

NQ — If set indicates that the error condition was a result of a non-queued command Having been issued and that the TAG field is therefore not valid. If cleared indicates that the TAG field is valid and that the error condition applies to a queued command.

BYTE 1-19 — An image of a device to host Register FIS is embedded in the data structure. The fields correspond to the Shadow Register Block Registers and are encoded with error information as defined in the ATA/ATAPI-6 standard.

ERROR — The value corresponding to the ATA ERROR register value for the command that failed. The command-specific error condition of invalid tag value shall be handled as an invalid command parameter and shall be reported as such (i.e. ABRT bit

set in the error register and all other bits cleared).

Note that the value returned in the ERROR field of the data structure is separate from the value returned in the Error shadow register when the initial error condition is signed. The Error shadow register value is used for the purpose of signaling a queued command error, while the value in the ERROR field of the data structure provides specific information about the error condition that the specific queued command encountered.

Vender Specific Allocated for vender specific use.

Data Structure Check sum

The data structure check sum is the 2's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

10.7.47.5 Phy Error Counters

The following table defines the format of the Native Command Queue error log

Byte	7	6	5	4	3	2	1	0
0	Reserved							
1	Reserved							
2	Reserved							
3	Reserved							
4	Identifier 001h: Command failed and ICRC error bit set to one in Error resister,							
5	Counter size 32bit : 2001h							
6-9	Counter Identifier 001h, counter value							
10	Identifier 002h: Data FIS R_ERR response for Data FIS.							
11	(transmitted and received) , Counter size 32bit : 2002h							
12-15	Counter Identifier 002h, counter value							
16	Identifier 003h : R_ERR response for Device-to-Host Data FIS,							
17	counter size 32bit : 2003h							
18-21	Counter Identifier 003h, counter value							
22	Identifier 004h : R_ERR response for Host-to-Device Data FIS,							
23	Counter size 32bit : 2004h							
24-27	Counter identifier 004h, counter value							
28	Identifier 005h : R_ERR response for Non-data FIS,							
29	Counter size 32bit : 2005h							
30-33	Counter identifier 005h, counter value							
34	Identifier 006h : R_ERR response for Device-to-Host Non-data FIS,							
35	Counter size 32bit : 2006h							
36-39	Counter identifier 006h, counter value							
40	Identifier 007h : R_ERR response for Host-to-Device Non-data FIS							
41	Counter size 32bit : 2007h							
42-45	Counter identifier 007h, counter value							
46	Identifier 008h : Device-to-host non-data FIS retries,							
47	Counter size 32bit : 2008h							
48-51	Counter identifier 008h, counter value							
52	Identifier 009h : Transitions from drive PhyRdy to drive PhyNRdy							
53	Counter size 32bit : 2009h							
54-57	Counter identifier 009h, counter value							
58	Identifier 00Ah : Device-to-Host Register FISes sent to a COMRESET							
59	Counter size 32bit : 200Ah							
60-63	Counter identifier 00Ah, counter value							
64	Identifier 00Bh : CRC errors within the a Host-to-Device FIS,							
65	Counter size 32bit : 200Bh							
66-69	Counter identifier 00Bh, counter value							
70	Identifier 00Fh : R_ERR response for Host-to-Device Data FIS,							
71	(received) , Counter size 32bit : 200Fh							
72-75	Counter identifier 00Fh, counter value							
76	Identifier 010h : R_ERR response for Host-to-Device Data FIS due to non-CRC errors							
77	(received) , Counter size 32bit : 2010h							
78-81	Counter identifier 010h, counter value							
82	Identifier 012h : R_ERR response for Host-to-Device Data FIS due to CRC errors,							
83	(received) ,Counter size 32bit : 2012h							
84-87	Counter identifier 012h, counter value							
88	Identifier 013h : R_ERR response for Host-to-Device non-data FIS due to non-CRC errors,							
89	(received) , Counter size 32bit : 2013h							
90-93	Counter identifier 013h, counter value							
94	Identifier 000h : No Counter value, marks end of counters in the page							
95	Counter size 32bit : 0200h							
96-99	Counter identifier 0000h, 0000h(end mark)							
100-510	Reserved							
511	Data Structure Checksum							

Counter n Identifier

Phy event counter identifier that corresponds to Counter n Value. Specifies the particular event counter that is being reported. The identifier is 16 bits in length.

Counter n Value

Value of Phy event counter that corresponds to Counter n Identifier. The numebr of significant bits is determined by Counter n Identifier bits 14:12. All counters are specified 32 bits in length. The counter will stop (and not wrap to zero) after reaching its maximum value.

Counter n Length

Size of Phy event counter as defined by bits 14:12 of Counter n identifier. The size of the Phy event counter is a multiple of 16bits. Also, all counters specified 32bits in length.

Data Structure checksum

The data structure check sum is the 2's complement of the sum of the first 511 bytes in the data structure. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct. The checksum is placed in byte 511.

Reserved

All reserved fields are zeros.

Identifier 000h

There is no counter associated with identifier 000h. A counter identifier of 000h indicates that there are no additional counters in the log page.

Identifier 001h

The counter with identifier 001h returns the number of commands that returned an ending status with the ERR bit set to one in the Status register and the ICRC bit set to one in the Error register.

Identifier 002h

The counter with identifier 002h returns the sum of (the number of transmitted Device-to-Host Data FISes to which the host responded with R_ERR) and (the number of received Host-to-Device Data FISes to which the device responded with R_ERR). The count returned for identifier 002h is not required to be equal to the sum of the counters with identifiers 003h and 004h.

Identifier 003h

The counter with identifier 003h returns the number of transmitted Device-to-Host Data FISes to which the host responded with R_ERR.

Identifier 004h

The counter with identifier 004h returns the number of received Host-to-Device Data FISes to which the device responded with R_ERR. The count returned for identifier 004h is not required to be equal to the sum of the counters with identifiers 00Fh and 010h.

Identifier 005h

The counter with identifier 005h returns the sum of (the number of transmitted Device-to-Host non-Data FISes to which the host responded with R_ERR) and (the number of received Host-to-Device non-Data FISes to which the device responded with R_ERR). Retries of non-Data FISes are included in this count.

Identifier 006h

The counter with identifier 006h returns the number of transmitted Device-to-Host non-Data FISes to which the host responded with R_ERR. Retries of non-Data FISes are included in this count.

Identifier 007h

The counter with identifier 007h returns the number of received Host-to-Device non-Data FISes to which the device responded with R_ERR. Retries of non-Data FISes are included in this count.

Identifier 008h

The counter with identifier 008h returns the number of transmitted Device-to-Host non-Data FISes which were retried after which the host responded with R_ERR.

Identifier 009h

The counter with identifier 009h returns the number of times the device transitioned into the PhyNRdy state from the PhyRdy state, including but not limited to asynchronous signal events, power management events, and COMRESET events. If interface power management is enabled, then this counter may be incremented due to interface power management transitions.

Identifier 00Ah

The counter with identifier 00Ah returns the number of transmitted Device-to-Host Register FISes with the device reset signature in response to a COMRESET, which were successfully followed by an R_OK from the host.

Identifier 00Bh

The counter with identifier 00Bh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the device responded with R_ERR due to CRC error. The count returned for identifier 00Bh is not required to be equal to the sum of the counters with identifiers 00Fh and 012h.

Identifier 00Dh

The counter with identifier 00Dh returns the number of received Host-to-Device FISes of all types (Data and non-Data) to which the devices responded with R_ERR for reasons other than CRC error. The count returned for identifier 00Dh is not required to be equal to the sum of the counters with identifiers 010h and 013h.

Identifier 00Fh

The counter with identifier 00Fh returns the number of received Host-to-Device Data FISes to which the device responded with R_ERR due to CRC error.

Identifier 010h

The counter with identifier 010h returns the number of received Host-to-Device Data FISes to which the device responded with R_ERR for reasons other than CRC error.

Identifier 012h

The counter with identifier 012h returns the number of received Host-to-Device non-Data FISes to which the device responded with R_ERR due to CRC error.

Identifier 013h

The counter with identifier 013h returns the number of received Host-to-Device non-Data FISes to which the device responded with R_ERR for reasons other than CRC error.

10.7.47.5.1 Counter Reset Mechanisms

The counter values are not retained across power cycles. The counter values are preserved across COMRESET and software resets. There are two mechanisms by which the host can explicitly cause the Phy counters to be reset. The first mechanism is to issue a BIST Activate FIS to the drive. Upon reception of a BISA Activate FIS the drive will reset all Phy event counters to their reset value. The second mechanism uses the Read LOG EXT command. When the drive receives a READ LOG EXT command for log page 11h and bit 0 in the Features register is set to one, the drive will return the current counter values for the command and then reset all Phy event counter value.

10.7.48 Write Log EXT (3Fh)

10.7.49 Write Log DMA EXT (57h)

COMMAND CODE	0 0 1 1 1 1 1 1	REGISTER
	REGISTER SETTING	NORMAL COMPLETION
DR	drive no.	no change
LBA Low	Log address	Reserved
LBA Low(exp)	Reserved	Reserved
LBA Mid	Sector offset(7:0)	Reserved
LBA Mid(exp)	Sector offset(15:8)	Reserved
LBA High	reserved	Reserved
LBA High(exp)	reserved	Reserved
SC	sector count(7:0)	Reserved
SC(exp)	sector count(15:8)	Reserved
FT	reserved	na
FT(exp)	reserved	na

This command writes a specified number of 512 byte data sectors to the specified log. The device shall interrupt for each DRQ block transferred.

10.7.50 Device Configuration (B1h)

This command has a number of separate functions which can be selected via the Feature Register when the command is issued. The subcommands and their respective codes are listed below.

Subcommand	Feature Register
DEVICE CONFIGURATION RESTORE	C0h
DEVICE CONFIGURATION FREEZE LOCK	C1h
DEVICE CONFIGURATION IDENTIFY	C2h
DEVICE CONFIGURATION SET	C3h

10.7.50.1 Device Configuration Restore

COMMAND CODE	1 0 1 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	C0h	na
LBA	na	na

The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command.

10.7.50.2 Device Configuration Freeze Lock

COMMAND CODE	1 0 1 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	C1h	na
LBA	na	na

The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the drive. The DEVICE CONFIGURATION FREEZE LOCK condition shall be cleared by a power-down. The DEVICE CONFIGURATION FREEZE LOCK condition shall not be cleared by hardware or software reset.

10.7.50.3 Device Configuration Identify

COMMAND CODE	1 0 1 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	C2h	na
LBA	na	na

The DEVICE CONFIGURATION IDENTIFY command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command will reflect the reduced set of capabilities, while the DEVICE CONFIGURATION IDENTIFY command will reflect the entire set of selectable capabilities.

The format of the Device Configuration Overlay data structure is shown in Table 10.7-9.

Table 10.7-9 Device Configuration Identify data stracture

Word	Content	
0	Data structure revision	
1	Multiword DMA modes supported	
	15-3	Reserved
	2	1 = Multiword DMA mode 2 and below are supported
	1	1 = Multiword DMA mode 1 and below are supported
	0	1 = Multiword DMA mode 0 is supported
2	Ultra DMA modes supported	
	15-5	Reserved
	5	1 = Ultra DMA mode 5 and below are supported
	4	1 = Ultra DMA mode 4 and below are supported
	3	1 = Ultra DMA mode 3 and below are supported
	2	1 = Ultra DMA mode 2 and below are supported
	1	1 = Ultra DMA mode 1 and below are supported
	0	1 = Ultra DMA mode 0 is supported
3-6	Maximum LBA address	
7	Command set/feature set supported	
	15-14	Reserved
	13	1 = SMART Conveyance self-test supported
	12	1 = SMART Selective self-test supported
	11	1 = Forced Unit Access supported
	10	Reserved
	9	1 = Streaming feature set supported
	8	1 = 48-bit Addressing feature set supported
	7	1 = Host Protected Area feature set supported
	6	1 = Automatic acoustic management supported
	5	1 = READ/WRITE DMA QUEUED commands supported
	4	1 = Power-up in Standby feature set supported
	3	1 = Security feature set supported
	2	1 = SMART error log supported
	1	1 = SMART self-test supported
	0	1 = SMART feature set supported
8	Serial ATA feature set supported	
	15-5	Reserved (0)
	4	1 = Software Settings Preservation supported
	3	1 = Asynchronous Notification supported
	2	1 = Interface power management supported
	1	1 = Non-zero buffer offsets in DMA Setup FIS supported
	0	1 = Native command queuing supported
9-254	Reserved	
255	Integrity word	
	15-8	Checksum
	7-0	Signature

10.7.50.3.1.1 Word 0: Data structure revision

Word 0 shall contain the value 0002h.

10.7.50.3.1.2 Word 1: Multiword DMA modes supported

Word 2 bits 2-0 contain the same information as contained in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response. Bits 15-3 of word 2 are reserved.

10.7.50.3.1.3 Word 2: Ultra DMA modes supported

Word 3 bits 5-0 contain the same information as contained in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response. Bits 15-6 of word 3 are reserved.

10.7.50.3.1.4 Words 3-6: Maximum LBA address

Words 4 through 7 define the maximum LBA address. This is the highest address accepted by the drive in the factory default condition. If no DEVICE CONFIGURATION SET command has been executed modifying the factory default condition, this is the same value as that returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.

10.7.50.3.1.5 Word 7: Command/features set supported

Word 7 bit 0 if set to one indicates that the drive is capable of supporting the SMART feature set.

Word 7 bit 1 if set to one indicates that the drive is capable of supporting SMART self-test including the self-test log.

Word 7 bit 2 if set to one indicates that the drive is capable of supporting SMART error logging.

Word 7 bit 3 if set to one indicates that the drive is capable of supporting the Security feature set.

Word 7 bit 4 if set to one indicates that the drive is capable of supporting the Power-up in Standby feature set.

Word 7 bit 5 if set to one indicates that the drive is capable of supporting the READ DMA QUEUED and WRITE DMA QUEUED commands.

Word 7 bit 6 if set to one indicates that the drive is capable of supporting the Automatic Acoustic Management feature set.

Word 7 bit 7 if set to one indicates that the drive is capable of supporting the Host Protected Area feature set.

Word 7 bit 8 if set to one indicates that the drive is capable of supporting the 48-bit Addressing feature set.

Word 7 bit 9 if set to one indicates that the drive is capable of supporting the Streaming feature set.

Word 7 bit 10 Reserved.

Word 7 bit 11 if set to one indicates that the drive is capable of supporting the Force Unit Access commands.

Word 7 bit 12 if set to one indicates that the drive is capable of supporting the SMART Selective self-test.

Word 7 bit 13 if set to one indicates that the drive is capable of supporting the SMART Conveyance self-test.

Word 7 bits 14 through 15 are reserved.

10.7.50.3.1.6 Word 8: Serial ATA features set supported

Word 8 bit 0 if set to one indicates that the drive is capable of supporting Native Command Queuing.
Word 8 bit 1 if set to one indicates that the drive is capable of supporting non-zero offsets in the DMA Setup FIS.
Word 8 bit 2 if set to one indicates that the drive is capable of supporting interface power management requests.
Word 8 bit 3 if set to one indicates that the drive is capable of supporting Asynchronous Notification.
Word 8 bit 4 if set to one indicates that the drive is capable of supporting Software Settings Preservation.
Word 7 bits 5 through 15 are reserved.

10.7.50.3.1.7 Words 8-254: Reserved

10.7.50.3.1.8 Word 255: Integrity word

Bits 7:0 of this word shall contain the value A5h. Bits 15:8 of this word shall contain the data structure checksum. The data structure checksum shall be the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7:0 of word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all bytes is zero when the checksum is correct.

10.7.50.4 Device Configuration Set

COMMAND CODE	1 0 1 1 0 0 0 1	REGISTER
REGISTER SETTING		NORMAL COMPLETION
DR	DRIVE No.	no change
CY	na	na
HD	na	na
SN	na	na
SC	na	na
FT	C3h	na
LBA	na	na

10.7.50.4.1 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	Bit location low							
Cylinder Low	Bit location high							
Cylinder High	Word location							
Device/Head	obs	na	obs	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the drive does not support this command, if a DEVICE CONFIGURATION SET command has already modified the original settings as reported by a DEVICE CONFIGURATION IDENTIFY command, if DEVICE CONFIGURATION FREEZE LOCK is set, if any of the bit modification restrictions described in this section are violated, or if a Host Protected Area has been established by the execution of a SET MAX ADDRESS command.

Sector Number –

If the command was aborted because an attempt was made to modify a mode or feature that cannot be modified with the drive in its current state, this register shall contain bits (7:0) set in the bit positions that correspond to the bits in the device configuration overlay data structure words 1, 2, or 7 for each mode or feature that cannot be changed. If not, the value shall be 00h.

Cylinder Low –

If the command was aborted because an attempt was made to modify a mode or feature that cannot be modified with the drive in its current state, this register shall contain bits (15:8) set in the bit positions that correspond to the bits in the device configuration overlay data structure words 1, 2, or 7 for each mode or feature that cannot be changed. If not, the value shall be 00h.

Cylinder High –

If the command was aborted because an attempt was made to modify a bit that cannot be modified with the drive in its current state, this register shall contain the offset of the first word encountered that cannot be changed. If an illegal maximum LBA address is encountered, the offset of word 3 shall be entered. If a checksum error occurred, the value FFh shall be entered. A value of 00h indicates that the Data Structure Revision was invalid.

Device register -

DEV shall indicate the selected device.

Status register -

BSY shall be cleared to zero indicating command completion.
DRDY shall be set to one.
DF (Device Fault) shall be set to one if a device fault has occurred.
DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

10.7.50.4.2 Description

The DEVICE CONFIGURATION SET command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The DEVICE CONFIGURATION SET command transfers an overlay that modifies some of the bits set in words 63, 82, 83, 84, and 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response. When the bits in these words are cleared, the drive shall no longer support the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the drive that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit. Modifying the maximum LBA address of the drive also modifies the address value returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.

The format of the overlay transmitted by the drive is described in Table 10.7-10. The restrictions on changing these bits is described in the text following Table 10.7-10. If any of the bit modification restrictions described are violated, the drive shall return command aborted.

Table 10.7-10 Device Configuration Overlay data stracture

Word	Content	
0	Data structure revision	
1	Multiword DMA modes supported	
	15-3	Reserved
	2	1 = Multiword DMA mode 2 and below are supported
	1	1 = Multiword DMA mode 1 and below are supported
	0	1 = Multiword DMA mode 0 is supported
2	Ultra DMA modes supported	
	15-5	Reserved
	5	1 = Ultra DMA mode 5 and below are supported
	4	1 = Ultra DMA mode 4 and below are supported
	3	1 = Ultra DMA mode 3 and below are supported
	2	1 = Ultra DMA mode 2 and below are supported
	1	1 = Ultra DMA mode 1 and below are supported
	0	1 = Ultra DMA mode 0 is supported
3-6	Maximum LBA address	
7	Command set/feature set supported	
	15-14	Reserved
	13	1 = SMART Conveyance self-test supported
	12	1 = SMART Selective self-test supported
	11	1 = Forced Unit Access supported
	10	Reserved
	9	1 = Streaming feature set supported
	8	1 = 48-bit Addressing feature set supported
	7	1 = Host Protected Area feature set supported
	6	1 = Automatic acoustic management supported
	5	1 = READ/WRITE DMA QUEUED commands supported
	4	1 = Power-up in Standby feature set supported
	3	1 = Security feature set supported
	2	1 = SMART error log supported
	1	1 = SMART self-test supported
	0	1 = SMART feature set supported
8	Serial ATA feature set supported	
	15-5	Reserved (0)
	4	1 = Software Settings preservation supported
	3	1 = Asynchronous Notification supported
	2	1 = Interface power management supported
	1	1 = Non-zero buffer offsets in DMA Setup FIS supported
	0	1 = Native command queuing supported
9-254	Reserved	
255	Integrity word	
	15-8	Checksum
	7-0	Signature

10.7.50.4.2.1 Word 0: Data structure revision

Word 0 shall contain the value 0001h.

10.7.50.4.2.2 Word 1: Multiword DMA modes supported

Word 1 bits 15:3 are reserved.

Word 1 bit 2 is cleared to disable support for Multiword DMA mode 2 and has the effect of clearing bit 2 in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Multiword DMA mode 2 is currently selected.

Word 1 bit 1 is cleared to disable support for Multiword DMA mode 1 and has the effect of clearing bit 1 in word 63 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Multiword DMA mode 2 is supported or Multiword DMA mode 1 or 2 is selected.

Word 1 bit 0 shall not be cleared.

10.7.50.4.2.3 Word 2: Ultra DMA modes supported

Word 2 bits 15:6 are reserved.

Word 2 bit 5 is cleared to disable support for Ultra DMA mode 5 and has the effect of clearing bit 5 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5 is currently selected.

Word 2 bit 4 is cleared to disable support for Ultra DMA mode 4 and has the effect of clearing bit 4 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5 is supported or if Ultra DMA mode 5 or 4 is selected.

Word 2 bit 3 is cleared to disable support for Ultra DMA mode 3 and has the effect of clearing bit 3 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5 or 4 is supported or if Ultra DMA mode 5, 4, or 3 is selected.

Word 2 bit 2 is cleared to disable support for Ultra DMA mode 2 and has the effect of clearing bit 2 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5, 4, or 3 is supported or if Ultra DMA mode 5, 4, 3, or 2 is selected.

Word 2 bit 1 is cleared to disable support for Ultra DMA mode 1 and has the effect of clearing bit 1 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5, 4, 3, or 2 is supported or if Ultra DMA mode 5, 4, 3, 2, or 1 is selected.

Word 2 bit 0 is cleared to disable support for Ultra DMA mode 0 and has the effect of clearing bit 0 in word 88 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. This bit shall not be cleared if Ultra DMA mode 5, 4, 3, 2, or 1 is supported or if Ultra DMA mode 5, 4, 3, 2, 1, or 0 is selected.

10.7.50.4.2.4 Words 3-6: Maximum LBA address

Words 3 through 6 define the maximum LBA address. This shall be the highest address accepted by the drive after execution of the command. When this value is changed, the content of IDENTIFY DEVICE words 60, 61 100, 101, 102, and103 shall be changed as described in the SET MAX ADDRESS and SET MAX ADDRESS EXT command descriptions to reflect the maximum address set with this command. This value shall not be changed and command aborted shall be returned if a Host Protected Area has been established by the execution of a SET MAX ADDRESS or SET MAX ADDRESS EXT command with an address value less than that returned by a READ NATIVE MAX ADDRESS or READ NATIVE MAX ADDRESS EXT command.. Any data contained in the Host Protected Area is not affected.

10.7.50.4.2.5 Word 7: Command/features set supported

Word 7 bits 15:9 are reserved.

Word 7 bit 8 is cleared to disable support for the 48-bit Addressing feature set and has the effect of clearing bit 10 in words 83 and 86 and clearing the value in words 103:100 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 7 is cleared to disable support for the Host Protected Area feature set and has the effect of clearing bit 10 in words 82 and 85 and clearing bit 8 in words 83 and 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If a Host Protected Area has been established by use of the SET MAX ADDRESS command, these bits shall not be cleared and the drive shall return command aborted.

Word 7 bit 6 is cleared to disable for the Automatic Acoustic Management feature set and has the effect of clearing bit 9 in word 83 and word 94 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 5 is cleared to disable support for the READ DMA QUEUED and WRITE DMA QUEUED commands and has the effect of clearing bit 1 in words 83 and 86 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 4 is cleared to disable support for the Power-up in Standby feature set and has the effect of clearing bits 5 and 6 in words 83 and 86 and clearing the value in word 94 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If Power-up in Standby has been enabled by a jumper, these bits shall not be cleared.

Word 7 bit 3 is cleared to disable support for the Security feature set and has the effect of clearing bit 1 in words 82 and 85 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. These bits shall not be cleared if the Security feature set has been enabled.

Word 7 bit 2 is cleared to disable support for the SMART error logging and has the effect of clearing bit 0 in words 84 and 87 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 1 is cleared to disable support for the SMART self-test and has the effect of clearing bit 1 in words 84 and 87 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

Word 7 bit 0 is cleared to disable support for the SMART feature set and has the effect of clearing bit 0 in words 82 and 85 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response. If bits 1 and 2 of word 7 are not cleared to zero or if the SMART feature set has been enabled by use of the SMART ENABLE OPERATIONS command, these bits shall not be cleared and the drive shall return command aborted.

10.7.50.4.2.6 Word 8: Serial ATA feature set supported

Word 8 bit 0 is cleared to disable support for the Native Command Queuing and Word 76 bit 8, Word 78 bit 1, Word 78 bit 2,Word 78 bit 4, Word 79 bit 1, Word 79 bit 2, and Word 79 bit 4 of IDENTIFY device will all be cleared to zero.
Word 8 bit 1 is cleared to disable support for the non-zero offsets in the DMA Setup FIS. But now, non-zero offsets in DMA Setup FIS feature not supported so, no effect happen when change this bit.
Word 8 bit 2 is cleard to disable support for the interface power management requests and Word 76 bit 9, Word 78 bit 3, and Word 79 bit 3 of IDENTIFY DEVICE will all be cleared to zero.
Word 8 bit 3 is cleared to disable support for the Asynchronous Notification. But now, Asynchronous Notification not supported by the drive, this bit does not affect the operation of the drive.
Word 8 bit 4 is cleared to disable support for the Software Settings Preservation and Word 78 bit 6 and Word 79 bit 6 of IDENTIFY DEVICE will be cleared to zero.
Word 8 bits 5 through 15 are reserved and shall be cleared to zero.

10.7.50.4.2.7 Words 9-254: Reserved

10.7.50.4.2.8 Word 255: Integrity word

Bits 7:0 of this word shall contain the value A5h. Bits 15:8 of this word shall contain the data structure checksum. The data structure checksum shall be the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7:0 of word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all bytes is zero when the checksum is correct.

10.8 Security Mode Feature Set

The Security mode features allow the host to implement a security password system to prevent unauthorized access to the disk drive.

- Following Commands are supported for this feature set.
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Parameter word for the Security mode feature set is described in IDENTIFY DEVICE response Word 128.

10.8.1 Security mode default setting

The drive is shipped with the master password set to 20h value (ASCII blanks) and the lock function disabled. The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

If the Master Password Revision Code feature is supported, the Master Password Revision Code is initially set to FFFEh.

10.8.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on.

10.8.3 Security mode operation from power-on

In locked mode, the drive rejects media access commands until a SECURITY UNLOCK command is successfully completed.

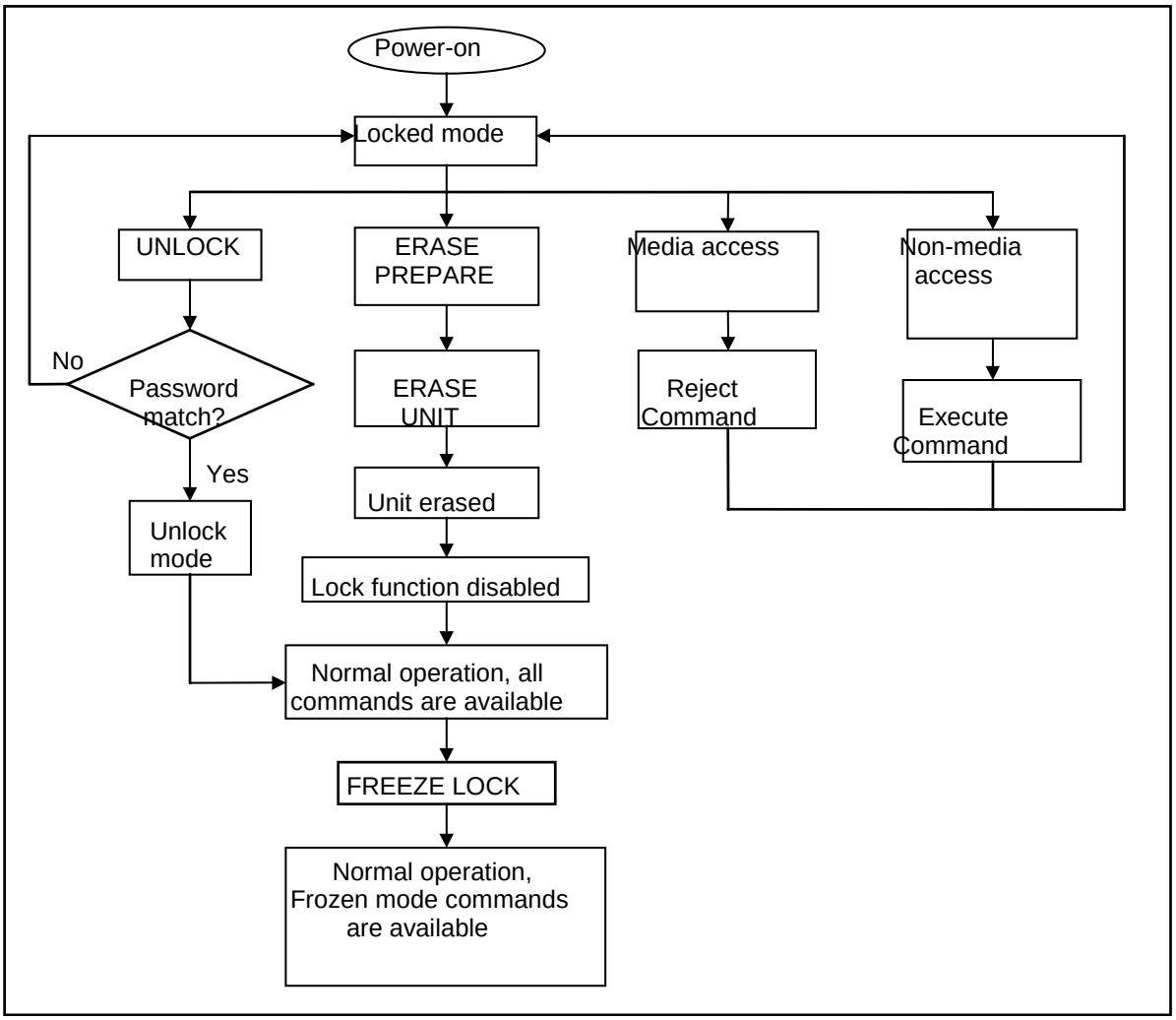


Figure 4 Password set security mode power-on flow

10.8.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data. However, the drive can be unlocked using the master password.

If the user password is lost and Maximum security level is set, it is impossible to access data. However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

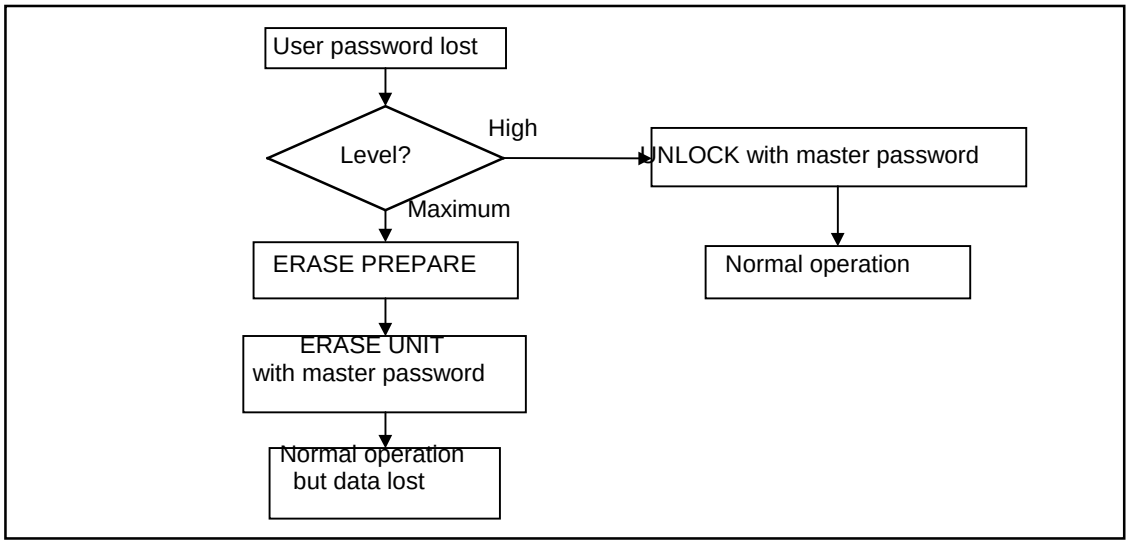


Figure 5 User password lost

If both the user password and the master password are lost, the drive cannot be in normal operation mode.

10.8.5 Command Table

This command table shows the drive's response to commands when the Security Function is enabled.

Table 10.8-1 Security mode command actions

Command	Locked mode	Unlocked mode	Frozen mode
CHECK POWER MODE	O	O	O
EXECUTE DEVICE DIAGNOSTICS	O	O	O
DEVICE CONFIGRATION	X	O	O
DOWNLOAD MICROCODE	O	O	O
FLUSH CACHE (EXT)	X	O	O
IDENTIFY DEVICE	O	O	O
IDLE	O	O	O
IDLE IMMEDIATE	O	O	O
INITIALIZE DEVICE PARAMETERS	O	O	O
NOP	O	O	O
READ BUFFER	O	O	O
READ DMA (EXT)	X	O	O
READ MULTIPLE (EXT)	X	O	O
READ NATIVE MAX ADDRESS (EXT)	O	O	O
READ SECTORS (EXT)	X	O	O
READ VERIFY (EXT)	X	O	O
READ FPDMA QUEUED	X	O	O
READ LOG EXT	O	O	O
READ LOG DMA EXT	O	O	O
RECALIBRATE	O	O	O
SECURITY DISABLE PASSWORD	X	O	X
SECURITY ERASE PREPARE	O	O	O
SECURITY ERASE UNIT	O	O	X
SECURITY FREEZE LOCK	X	O	O
SECURITY SET PASSWORD	X	O	X
SECURITY UNLOCK	O	O	X
SEEK	O	O	O
SET FEATURES	O	O	O
SET MAX (EXT)	X	O	O
SET MULTIPLE MODE	O	O	O
SLEEP	O	O	O
SMART	O	O	O
STANDBY	O	O	O
STANDBY IMMEDIATE	O	O	O
WRITE BUFFER	O	O	O
WRITE DMA (EXT)	X	O	O
WRITE DMA FUA (EXT)	X	O	O
WRITE MULTIPLE (EXT)	X	O	O
WRITE MULTIPLE FUA (EXT)	X	O	O
WRITE SECTORS (EXT)	X	O	O
WRITE VERIFY	X	O	O
WRITE FPDMA QUEUED	X	O	O
WRITE LOG EXT	X	O	O
WRITE LOG DMA EXT	X	O	O

O: Drive executes command normally
X: Drive rejects command with an Aborted command error

10.9 Self-Monitoring, Analysis and Reporting Technology

Self-monitoring, analysis and reporting technology (SMART) is the function to protect user data and to minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the drive. By monitoring and storing the critical performance and calibration parameters, SMART drives attempt to predict the likelihood of near-term degradation or fault condition. The host system warns the user of the impending risk of data loss and advises the user of appropriate action by informing the host system of the negative reliability.

SMART commands use a single command code and are differentiated by the value placed in the Features register.

The Commands supported by this feature set are:

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- SMART READ ATTRIBUTE VALUES
- SMART READ ATTRIBUTE THRESHOLDS
- SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
- SMART SAVE ATTRIBUTE VALUE
- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ LOG SECTOR
- SMART WRITE LOG SECTOR
- SMART ENABLE OPERATIONS
- SMART DISABLE OPERATIONS
- SMART RETURN STATUS
- SMART ENABLE/DISABLE AUTOMATIC OFF-LINE

10.9.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the drive. Attributes are selected by the drive manufacturer based on that attribute's ability to predict degrading or faulty conditions for that particular drive. The specific set of attribute being used and the identity of these attributes is vendor specific and proprietary.

10.9.2 Attributes values

Attribute values are used to measure the relative reliability of individual performance or calibration attributes.

10.9.3 SMART function default setting

The drives are shipped from the drive manufacturer's factory with the SMART feature disabled. SMART feature will be enabled by the system manufacturer or the application.

10.10 SMART COMMAND TRANSPORT(SCT)

The SMART COMMAND TRANSPORT(SCT) feature set is supported. SCT commands are executed by using SMART Read Log and SMART Write Log Command, or Read Log EXT and Write Log EXT command.

Log Address E0h is used to issue commands and return status. Log Address E1h is used to transport data.

Please refer to ATA8-ACS “SCT Command Transport” section for more detail.

SCT command format is below:

Table 10.10-1 SCT Command format

Byte	Field	Words	Description
0-1	Action Code	1	This field specifies the command type and the type of data being accessed, or the action being performed.
2-3	Function Code	1	This field specifies the type of access and varies by command
4-x	Parameter1	Depends on command	Depends on command
x+1-y	Parameter2	Depend on command	Depends on command
・・・	・・・	・・・	・・・
	Total Words	256	

The following SCT Action Codes are supported:

Table 10.10-2 SCT Action Codes Supported

Action Code	Description
0002	SCT Write Same command
0003	SCT Error Recovery Control command
0004	SCT Feature Control command
0005	SCT Data table command

10.11 Adaptive Power Mode Control

Adaptive Power Mode Control is a function to reduce power consumption without performance degradation. The drive supports the following Idle modes of 3 levels. The drive enters into idle mode adaptively in accordance with the command pattern.

10.11.1 Performance Idle

The drive enters Performance Idle mode at the completion of a command from host. In this mode, electric circuit and servo is ready to process the next command without delay.

10.11.2 Active Idle

Some of electric circuit and servo functions are powered off in this mode. The heads are stopped near the disk center. If a shock is detected by Shock Sensor, the drive enters into Performance Idle mode automatically. Power consumption for Active Idle mode is 55%～65% lower than that of Performance Idle mode. Command processing time is approximately 35ms longer than that of Performance Idle mode.

10.11.3 Low Power Idle

In Low Power Idle mode, the heads are unloaded on the ramp and the spindle motor continues normal rotation. Power consumption for Low Power Idle mode is 60%～70% lower than that of Performance Idle mode. Command processing time is approximately 400ms longer than that of Performance Idle mode.

10.11.4 Transition time

The transition time changes dynamically in accordance with the current command pattern.

10.12 Interface Power Management Control

Interface power management Control is a function to reduce power consumption of the interface.. Host can initiate Partial request and Slumber request to reduce power consumption. The interface management can also be initiated by the drive. To enable the device initiating interface power management, host shall enable this feature by SET FEATURE command.

10.12.1 Interface power management modes

Interface power management modes are categolized as Active, Partial and Slumber. Details are as follows

10.12.1.1 Active

Interface is active and communication between host and drive is established.

10.12.1.2 Partial

Interface is in-active and wake up time to Active mode is less than 10 microseconds.
The drive will get enter Partial mode under following situations.

10.12.1.2.1 Host Initiated Partial

1) The drive detect PMREQ_P primitive and the drive accepts the primitive. To indicate the drive acceptance, PMACK primitive will be used.
2) The drive will not accept PMREQ_P when the drive is waiting for command or transmitting/receiving FIS.
3) The drive will wakeup from Partial mode when the drive detects COMWAKE, COMRESET. Also, the drive will wakeup from Partial mode when the drive needs to start transmitting some FIS to the host. In this case, the drive will send COMWAKE to the host.

10.12.1.2.2 Device Initiated Partial

1) The drive will initiate Partial when the drive interface power management feature is enabled.
2) The drive will initiate Partial when predetermined time past after the last command completion. Or, such as long seek is needed during the command execution.
3) While the S-ATA bus condition is in Partial mode, both of the host and the drive can initiate wake up sequence via COMWAKE.

10.12.1.3 Slumber

Interface is in-active and wake up time to Active mode is less than 10 miliseconds.
The drive will get in Slumber mode when following situation happened.

10.12.1.3.1 Host Initiated Slumber

1) The drive detect PMREQ_S primitive and the drive accept its the primitive. To indicate drive acceptance, PMACK primitive will be used.

2) The drive will not accept PMREQ_S when the drive waiting for command or transmitting/receiving FIS.

3) The Drive will wakeup from Slumber mode when the drive detect COMWAKE or COMRESET. Also, the drive will wakeup from Slumber mode when the drive needs to start transmitting some FIS to the host. In this case, the drive will send COMWAKE to the host.

10.12.1.3.2 Device Initiated Slumber

1) The drive will initiate Slumber mode when the drive interface power management feature is enabled.

2) The drive will initiate Slumber mode after STANDBY IMMEDIATE or SLEEP command completion.

3) While the S-ATA bus condition is in Slumber mode, both of host and the drive can initiate wake up sequence via COMWAKE.

10.13 Reset

A RESET condition will change the drive condition to busy, allowing the drive to perform the specified initialization required for normal operation.

A RESET condition can be generated by both COMRESET and software. There are two hardware resets, one is by the COMRESET and the other is by the drive power sense circuitry. These resets will chenge the drive condition to busy when the system and the drive respectively acknowledge specified supply voltage (See 6.1).

The other reset is software generated. The Host can write to the Device Control register and set the reset bit with RegH2D FIS. The host software condition will continue until the reset bit is set to zero.

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Once the reset is negated and the drive is re-enabled, the drive will perform necessary hardware initialization, clear any previously programmed drive parameters and revert to the defaults, load the Shadow Register Block registers with their initial values, and then send RegD2H FIS indicating clear BSY bit.
No interrupt is generated when initialization is complete. The initial values (hex) for the Shadow Register Block registers and other settings when the Software Settings Preservation is disabled and enabled are as follows.

Table 10.13-1 Initialization of Shadow Register Block registers (Power ON and Software Settings Preservation disabled)

REGISTER	POWER ON	COMRESET	SOFTWARE RESET
Data	00	00	00
Error	01	01	01
Sector Count	01	01	01
Sector Number	01	01	01
Cylinder Low	00	00	00
Cylinder High	00	00	00
Device/Head Register	00	00	00
Status/Alternate Status	50 or 52	50 or 52	50 or 52
Device address	7E or FE	7E or FE	7E or FE
ECC Length	0 bytes	0 bytes	no change
Data Buffer	undefined	undefined	no change
Addressing mode	default	Default	no change
Auto stand-by mode	disable	Disable	no change
Read Cache	enable	Enable	no change
Write Cache	enable	Enable	no change
Multiple mode	16 sectors	16 sectors	no change
DMA transfer mode	Ultra DMA mode 5	Ultra DMA mode 5	no change
PIO transfer mode	PIO mode 4 flow control	PIO mode 4 flow control	no change
Security mode state	Depends on setting	Depends on setting	no change
Security Freeze Lock	Depends on setting	Depends on setting	no change
Set Max Address(EXT)	Depends on volatile setting	Depends on volatile setting	no change
Non-zero buffer offset	disable	disable	no change
DMA Setup FIS Auto-Activate optimization	disable	disable	no change
Device Initiated interface power state transitions	disable	disable	no change
Guaranteed In-Order Data delivery	disable	disable	no change
Software Setting Preservation	enable	enable	no change

Table 10.13-2 Initialization of Shadow Register Block registers (Software Settings Preservation enabled)

REGISTER	COMRESET	SOFTWARE RESET
Data	00	00
Error	01	01
Sector Count	01	01
Sector Number	01	01
Cylinder Low	00	00
Cylinder High	00	00
Device/Head Register	00	00
Status/Alternate Status	50 or 52	50 or 52
Device address	7E or FE	7E or FE
ECC Length	0 bytes	no change
Data Buffer	undefined	no change
Addressing mode	no change	no change
Auto stand-by mode	no change	no change
Read Cache	no change	no change
Write Cache	no change	no change
Multiple mode	no change	no change
DMA transfer mode	no change	no change
PIO transfer mode	no change	no change
Security mode state	no change	no change
Security Freeze Lock	no change	no change
Set Max Address(EXT)	no change	no change
Non-zero buffer offset	disable	no change
DMA Setup FIS Auto-Activate optimization	disable	no change
Device Initiated interface power state transitions	disable	no change
Guaranteed In-Order Data delivery	disable	no change
Software Setting Preservation	enable	no change

10.13.1 Cache Operations

(1) READ CACHE OPERATION

Receiving a read command, the data in the buffer memory are sent to the host without access to the disk media as long as the object data reside in the buffer memory and the conditions for the drive's read cache operation are fulfilled.

If any of the conditions of the read cache operation is not fulfilled, the drive carries out read data operation and the object data for the read command is read from the media and kept in the buffer and then the data is transferred from the buffer to the host.

The following data required by the read command may continuously be read by the buffer under the drive's read ahead cache operation until the buffer available for read cache is full or the new command is received.

(2) WRITE CACHE OPERATION

Receiving a write command, the drive continuously receives the write data from the host until all data are transferred or the buffer available for write cache is full, whether the data are written on the media or not. If all data for the command are received, the drive reports completion of the command by RegHD FIS with BSY=0 and I=0.

If the command which follows the write cache command is also a write command for succeeding block address, the drive receives write data from host without waiting for the previously received data to be written on the media. And the drive reports completion of the command when the buffer receives all the data.

During a write cache operation and Activitiy feature (pin 11 of the power segment) used, Activity signal line is kept "on" until all the data in the write buffer are written on the media.

10.13.2 Notes for write cache

(1) Loss of data in write buffer

If write cache is enabled, hard reset or soft reset does not cause data loss. But power off immediate after completion of the command may cause data loss, because actual writing of the data onto the media is not completed at this moment. Therefore, it is recommended that any other command except write or read command is executed and completion of the command is confirmed before powering off the drive. Stand-by command can be helpful for this purpose.

(2) Error report

When write cache is enabled, any unrecoverable error encountered after the report of completion of a command shall be reported by the later command. Actual writing of the data onto the media may not be completed at this moment. In this case, READY bit in the RegDH is negated to show that the error has occurred during the write cache operation previously executed.

Address validity check is performed with actual media access. The error may be reported during the execution of a command or after completion of a write cache command if the address the data has tried to access is non-existent.

10.14 Automatic Write Reallocation

If the drive has difficulty in executing normal write operation due to unrecoverable errors such as ID NOT FOUND, the sectors those show some errors may be reallocated automatically to continue normal operation and secure the write data. This operation is helpful especially in write cache, when the completion of the command is reported before actual writing to media. During write operation including this AWRE function and Activity signal used (pin 11 of the power segment), the Activity signal is kept " on ". This operation takes 20 seconds maximum to be completed; therefore, the time-out period should be set longer than this value. If the next command is a write command, the data of the first block will be transferred without any delay.

11. Command Protocol

Commands can be grouped into different classes according to the protocols used for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks BSY bit and DRDY bit in the Shadow Register Block registers. If BSY ＝1, the host should proceed no further unless and until the BSY＝0, and the DRDY＝1.

Interrupts are cleared when host do predetermined action such as reading Status register in the Shadow Register Block registers, issues a reset, or writes to the Command register in the Shadow Register Block registers.

A command shall only be interrupted with a COMRESET or software reset. The result of writing to the command register while BSY＝1 or DRQ＝1 is unpredictable and may result in data corruption. Therefore, a command should only be interrupted by a reset at times when the host judges that there is a problem, such as receiving no response from the drive. Host programmers should set command time-out periods enough long in order to avoid having effect on the drive's ability to perform level retry and data recovery activities.

Basically for the Serial ATA FIS transaction, FIS is used. For example, non-data command, host will issue only one RegH2D FIS. And when the command is complete, drive will send RegD2H FIS. During command execution, no activity such as re-reading Block register will occur on the Serial ATA bus.

11.1 PIO data In commands

PIO data in commands

Commands for this class are:

- IDENTIFY DEVICE
- READ BUFFER
- READ SECTOR(S) (with and without retry)
- READ SECTOR(S) EXT
- READ MULTIPLE
- READ MULTIPLE EXT
- READ LOG EXT
- SMART Read Attribute Values
- SMART Read Attribute Thresholds
- SMART Read Log Sector
- DEVICE CONFIGRATION IDENTIFY

PIO data in protocol:

a) The host sends the RegHD to the drive including required command parameters.

b) When the drive finishes the preparation of the data to be transferred, the drive will send the PIO Setup FIS to the host.

The PIO Setup FIS includes DRQ bit=1, I bit = 1 and Error(Error Register) = 00h.

c) The drive sends the Data FIS.

d) Continue data transfer from b) until the data transer is complete.

e) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and the Error register with error code.

f) When unrecoverable error happened during data transfer, the PIO Setup FIS contains BSY=0, DRQ=1 and ERR=1. And then start transfer one sector data with Data FIS. When the data transfer finishes, command is completed.

When the command is READ MULTIPLE or READ MULTIPLE EXT, the size the data contains in the Data FIS will become the multiple count * 512 byte set by SET FEATURE command.

Also the SET FEATURE command have some option to change the PIO transfer speed. But it will have no effect for S-ATA data transfer.

Normal Protocol for PIO Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[PIOSU]-[DATA]-[PIOSU][DATA]……[PIOSU]-[DATA]---------

Command Parameter Error protocol for PIO Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(BSY=0, DRQ=0, I=1, Error Reg=Error Code)

Command Data Error protocol for PIO Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[PIOSU]-[Data]…..[PIOSU]-[Data]-------

(ERR=1,BSY=0,DRQ=1, Error Reg=Error Code)

11.2 PIO data out commands

Commands for this class are:

- WRITE BUFFER
- WRITE MULTIPLE
- WRITE MULTIPLE EXT
- WRITE MULTIPLE FUA EXT
- WRITE SECTOR(S) (with and without retry)
- WRITE SECTOR(S) EXT
- WRITE VERIFY
- WRITE LOG EXT
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SET MAX SET PASSWORD
- SMART Write Log Sector
- DOWNLOAD MICROCODE

PIO data out protocol:

a) The host sends the RegHD to the drive including required command parameters.

b) When the drive finishes the preparation of the data to be transferred, the drive will send the PIO Setup FIS to the host.

PIO Setup FIS includes DRQ bit=1, I bit = 1 and Error(Error Register) = 00h.

c) The host send the Data FIS.

d) Continue data transfer from b) until the data transer completed.

e) When the data transfer finished, the drive will send RegDH to the host with BSY=0, I=1 and ERR=0

f) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and the Error register with error code.

g) When unrecoverable error happened during data transfer, the PIO Setup FIS contains BSY=0, DRQ=1 and ERR=1 will send before the last data transfer.with Data FIS. After the data transfer finishes , drive will send the RegDH to the host with BSY=0, DRQ=0, ERR=1 and Error register with error code.

h) The error will sometimes report after data transfer complete. In this case, the error infomation will set by the RegDH to indicate command complete.

When the command is the WRITE MULTIPLE or WRITE MULTIPLE EXT, the size the data contains in the Data FIS will become the multiple count * 512 byte set by SET FEATURE command.

Also the SET FEATURE command have some option to change the PIO transfer speed. But it will have no effect for S-ATA data transfer.

Normal Protocol for PIO Data Out command

Host Tx -----[RegHD]----------[DATA]----------[DATA]……----------[DATA]----------

Drive Tx ----------[PIOSU]----------[PIOSU]----------……[PIOSU]----------[RegDH]---------

(BSY=0,DRQ=0,I=1)

Command Parameter Error protocol for PIO Data Out command

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(BSY=0, DRQ=0, I=1, Error Reg=Error Code)

Command data error protocol for PIO Data Out command(during the data transfer)

Host Tx -----[RegHD]----------[Data]----------[Data]----------

Drive Tx ----------[PIOSU]----------…..[PIOSU]----------[RegDH]-------

(ERR=1,BSY=0,DRQ=1, Error Reg=Error Code)

Command error protocol for DIO Data Out command (error report at the end of the command)

Host Tx -----[RegHD]----------[DATA]----------[DATA]……----------[DATA]----------

Drive Tx ----------[PIOSU]----------[PIOSU]----------……[PIOSU]----------[RegDH]---------

(BSY=0,DRQ=0,I=1,ERR=1)

(Error Reg = Error Code)

11.3 Non-data commands

Commands for this class are:

- CHECK POWER MODE
- EXECUTE DEVICE DIAGNOSTICS
- FLUSH CACHE
- FLUSH CACHE EXT
- IDLE
- IDLE IMMEDIATE
- INITIALIZE DEVICE PARAMETERS
- NOP
- READ VERIFY SECTOR(S)
- READ VERIFY SECTOR(S) EXT
- READ NATIVE MAX ADDRESS
- READ NATIVE MAX ADDRESS EXT
- RECALIBRATE
- SEEK
- SET FEATURES
- SET MULTIPLE MODE
- SLEEP
- STANDBY
- STANDBY IMMEDIATE
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SMART Enable/Disable Attribute Autosave
- SMART Save Attribute Values
- SMART Executive Off-line Immediate
- SMART Enable Operation
- SMART Disable Operation
- SMART Return Status
- SMART Enable/Disable Automatic Off-line
- SET MAX ADDRESS
- SET MAX ADDRESS EXT
- SET MAX LOCK
- SET MAX UNLOCK
- SET MAX FREEZE LOCK
- DEVICE CONFIGRATION RESTORE
- DEVICE CONFIGRATION FREEZE LOCK
- DEVICE CONFIGRATION SET

Non-data command protocol:

a) The host send the RegHD to the drive including required command parameters.

b) When the command finishes, the drive will send RegDH to host with BSY=0, I=1 and ERR=0

c) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and the Error register with error code.

d) When unrecoverable error happened during command execution or the RegHD at a) is not executable, the drive will send the RegDH to host with BSY=0, DRQ=0, ERR=1 and the Error register with error code.

Non-Data command protocol

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(No Error : BSY=0, DRQ=0, I=1, Error Reg=00h)

(Error : BSY=0, DRQ=0, I=1, Error Reg=Error Code)

Note: During command execution of in Parallel ATA, sometimes host will poll the status. For Serial ATA, there are no transaction of FIS during command execution. This means, during command execution, host will see BSY=1 in the Shadow Register Block registers, but the status bits will not update until next RegDH receive.

11.4 DMA data In commands

Commands for this class are:

- READ DMA (with and without retry)
- READ DMA EXT
- READ LOG DMA EXT

DMA data in protocol:

a) The host sends the RegHD to drive including required command parameters.
b) When the dsrive finishes the preparation of the data to be transferred, the drive will start data transfer with Data FIS.
c) Continue data transfer from b) until the data transer complete.
d) When the data transfer finish with no error, the drive will send RegDH to the host.
e) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and the Error register with error code.
f) When unrecoverable error happened during the data transfer, Data FIS transmitting will stop and RegHD will send to the host.

Also the SET FEATURE command have some option to change the DMA/UDMA transfer speed. But it will have no effect for S-ATA data transfer.

Normal Protocol for DMA Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[DATA]-[DATA]…[DATA]-[RegDH]----------

Command Parameter Error protocol for DMA Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(BSY=0, DRQ=0, I=1, Error Reg=Error Code)

Command Data Error protocol for DMA Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[Data]…..-[Data]-[RegDH]----------

(ERR=1,BSY=0,I=1,DRQ=1, Error Reg=Error Code)

11.5 DMA data Out commands

- WRITE DMA (with and without retry)
- WRITE DMA EXT
- WRITE DMA FUA EXT
- WRITE LOG DMA EXT

DMA Data out protocol:

a) The host send the RegHD to the drive including required command parameters.
b) When the drive finishes to accept the data transfer, send DMA Activate FIS(DMACT) to the host.
c) The host sends the data FIS.
d) Continue data transfer from c) until the data transer is complete.
e) When the data transfer is completed with no error, the drive will send RegDH to the host.
f) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and Error register with error code.
g) When unrecoverable error happened during data transfer, RegHD with error information will be send to the host after data transfer completed.

Also the SET FEATURE command have some option to change the DMA/UDMA transfer speed. But it will have no effect for S-ATA data transfer.

Normal Protocol for DMA Data In command

Host Tx -----[RegHD]----------[DATA] [DATA]……----------

DriveTx ----------[DMACT]----------…….[RegDH]----------

Command Parameter Error protocol for DMA Data In command

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(BSY=0, DRQ=0, I=1, Error Reg=Error Code)

Command Data Error protocol for DMA Data In command

Host Tx -----[RegHD]----------[DATA]-[DATA]……[DATA]----------

Drive Tx ----------[RegDH]--

(ERR=1,BSY=0,I=1,DRQ=1, Error Reg=Error Code)

11.6 Native Command Queue commands

Commands for this class are:

- READ FPDMA QUEUED
- WRITE FPDMA QUEUED

11.6.1 Command Issue protocol

The protocol to issue these commands are similar to the Non Data command protocol. But the data transfer following to the command is unque for the NCQ commands.

a) The host sends the RegHD to the drive including required command parameters.
b) When the drive accepts the command , the drive will send RegDH to the host with BSY=0, I=1 and ERR=0
Also, the command will be registerered in the queue table inside the drive.
c) When the RegHD at a) is not executable, the drive will send RegDH with BSY=0, I=1, ERR=1 and the Error register with error code.

Native Command Queue, command issue protocol

Host Tx -----[RegHD]----------

Drive Tx ----------[RegDH]----

(No Error : BSY=0, DRQ=0, I=1, Error Reg=00h)

(Error : BSY=0, DRQ=0, I=1, Error Reg=Error Code)

11.6.2 Data transfer protocol for the READ FPDMA QUEUED

a) When the drive is prepared to send data to the host, the drive will send the DMA Setup FIS with the Tag number as the response to READ FPDMA QUEUED command, D=0, I=0 and A=0.
b) The drive sends data with Data FIS. The data offset and the number of the data to be transfer is described in the previous DMA Setup FIS.
c) Upon successful completion of an outstanding command, the drive will send a Set Drive Bits FIS with bits set in the SActive field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted.

Read FPDMA QUEUED data transfer protocol

Host Tx ----------

Drive Tx -----[DMASU]-[DATA]-[DATA]…[DATA]--[SDB]--------

(No Error : ERR=0, I=1, Error Reg=00h)

11.6.3 Data transfer protocol for the WRITE FPDMA QUEUED

a) When the drive is prepaeed to accept data from the host, the drive will send the DMA Setup FIS with the Tag number as the response to WRITE FPDMA QUEUED command, the offset of the data and the number of the data to be transfered, D=0, I=0 and A=0 and the DMA Activate FIS (when the DMA Auto-activate optimization is disabled)

b) The host send data with Data FIS. The data offset and the number of the data that the host should be transferred is described in the previous DMA Setup FIS.

c) Upon successful completion an outstanding command, the drive will send a Set Drive Bits FIS with bits set in the SActive field corresponding to the bit position for each command TAG that has completed since the last status notification was transmitted.

WRITE FPDMA QUEUED data transfer protocol

Host Tx ----------[DATA]-[DATA]….[DATA]----------

Drive Tx -----[DMASU]-([DMACT])----------[SDB]--------

(No Error : ERR=0, I=1, Error Reg=00h)

11.6.4 Error Reporting for the READ/WRITE FPDMA QUEUED

The drive will report error when NCQ command is in progress.

When unrecoverable error happened during read or write operation, the drive will report the error with Set Device Bit FIS where ERR=1 , ERR Register = error code, I=1 and SActive field = 00000000h. After sending error, the drive will accept only the Read Log EXT command with page 10h , COMRESET or Soft reset with RegHD. If other command issued by the host, the drive will report error with ERR=1, I=1, Error Register = 04h.

When the drive accept the Read Log EXT command with Page 10h, the drive will stop processing queue commands and send SDB with ERR=0, Error Register = 0, I=0 and SActive = FFFFFFFFh. Then the drive send the error log of the Page 10h data to report the error conditon to the host.