Socket AM3 Processor
Functional Data Sheet

Publication # **40778**
Revision: **1.13**
Issue Date: **January 2009**

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Revision History

Date	Revision	Description
January 2009	1.13	Third NDA release. • M_VDDIO_PWRGD changed to not supported. (See Table 3 on page 10.)
June 2008	1.11	Second NDA release. • Added MA/B_EVENT_L pins. • Added NP/VSS and NP/RSVD pins.
August 2007	1.07	Initial NDA release.

1 Pins

1.1 Connection Diagram (Left Half)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VCID	VCID	VSS	VDDNB	DBREQ_L	VDDNB	VSS	CLKIN_H	VSS	TEST25_H	VSS	VDDR	MB_DATA[1]	MB_DATA[6]	MB_DATA[2]	MB_DATA[8]	A
B	VCID	NP/ RSVD	VDD	VSS	VDDNB	DBRDY	VDDNB	CLKIN_L	VSS	TEST25_L	VSS	VDDR	MB_DM[0]	VSS	MB_DATA[7]	VSS	B
C	SVC/ VID[3]	VDD	VSS	VDD	TEST14	VDDNB	RESET_L	VDDNB	PWROK	VDDA	TEST29_H	VDDR	MB_DQS_L[0]	MB_DQS_H[0]	MB_DATA[3]	MB_DATA[13]	C
D	VID[4]	VID[5]	VDD	TEST8	VDD	TEST17	VDDNB	LDTSTOP_L	VDDNB	VDDA	TEST29_L	VDDR	MB_DATA[0]	VSS	MB_DATA[12]	VSS	D
E	VID[0]	PVIEN/ VID[1]	SVD/ VID[2]	VDD	TEST7	VDD	TEST16	VDDNB	TEST18	VDDNB	VSS	VDDR_SENSE	MB_DATA[5]	MA_DATA[1]	MA_DATA[6]	MA_DATA[2]	E
F	PSI_L	RSVD	M_VDDIO_PWRGD	VSS	VDD	TEST9	VDD	TEST15	VDDNB	TEST19	VDDNB	M_VREF	MB_DATA[4]	VSS	MA_DQS_H[0]	VSS	F
G	VDD_FB_L	VDD_FB_H	VDDNB_FB_L	VDDNB_FB_H	CORE_TYPE	VDD	TEST10	VDD	VSS	VDDNB	VSS	VDDNB	MA_DATA[5]	MA_DATA[0]	MA_DQS_L[0]	MA_DATA[7]	G
H	VLDT_B	VLDT_B	VOID	VOID	VLDT_B	VLDT_B	VDD	VSS	TEST28_L	VSS	VDD	VSS	MA_DATA[4]	VSS	MA_DM[0]	VSS	H
J	L0_CADIN_H[1]	L0_CADIN_L[0]	L0_CADIN_H[0]	VSS	VSS	L0_CADIN_H[8]	VSS	VDD	VSS	TEST28_H	VSS	VDD	VSS	VDD	VSS	VDD	J
K	L0_CADIN_L[1]	VSS	VSS	L0_CADIN_H[9]	L0_CADIN_L[9]	L0_CADIN_L[8]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	K
L	L0_CADIN_H[3]	L0_CADIN_L[2]	L0_CADIN_H[2]	VDD	VDD	L0_CADIN_H[10]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L
M	L0_CADIN_L[3]	VDD	VDD	L0_CADIN_H[11]	L0_CADIN_L[11]	L0_CADIN_L[10]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	M
N	L0_CADIN_H[4]	L0_CLKIN_L[0]	L0_CLKIN_H[0]	VSS	VSS	L0_CLKIN_H[1]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	N
P	L0_CADIN_L[4]	VSS	VSS	L0_CADIN_H[12]	L0_CADIN_L[12]	L0_CLKIN_L[1]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	P
R	L0_CADIN_H[6]	L0_CADIN_L[5]	L0_CADIN_H[5]	VDD	VDD	L0_CADIN_H[13]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	R
T	L0_CADIN_L[6]	VDD	VDD	L0_CADIN_H[14]	L0_CADIN_L[14]	L0_CADIN_L[13]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	T
U	L0_CTLIN_H[0]	L0_CADIN_L[7]	L0_CADIN_H[7]	VSS	VSS	L0_CADIN_H[15]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	U
V	L0_CTLIN_L[0]	VSS	VSS	L0_CTLIN_H[1]	L0_CTLIN_L[1]	L0_CADIN_L[15]	HTREF0	HTREF1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	V
W	L0_CADOUT_L[7]	L0_CTLOUT_H[0]	L0_CTLOUT_L[0]	VDD	VDD	L0_CTLOUT_L[1]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	W
Y	L0_CADOUT_H[7]	VDD	VDD	L0_CADOUT_L[15]	L0_CADOUT_H[15]	L0_CTLOUT_H[1]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	Y
AA	L0_CADOUT_L[5]	L0_CADOUT_H[6]	L0_CADOUT_L[6]	VSS	VSS	L0_CADOUT_L[14]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	AA
AB	L0_CADOUT_H[5]	VSS	VSS	L0_CADOUT_L[13]	L0_CADOUT_H[13]	L0_CADOUT_H[14]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	AB
AC	L0_CLKOUT_L[0]	L0_CADOUT_H[4]	L0_CADOUT_L[4]	VDD	VDD	L0_CADOUT_L[12]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	AC
AD	L0_CLKOUT_H[0]	VDD	VDD	L0_CLKOUT_L[1]	L0_CLKOUT_H[1]	L0_CADOUT_H[12]	VDD	VSS	VDD	VSS	VDD	VSS	MA_DATA[59]	VSS	MA_DQS_H[7]	VSS	AD
AE	L0_CADOUT_L[2]	L0_CADOUT_H[3]	L0_CADOUT_L[3]	VSS	VSS	L0_CADOUT_L[11]	NP/ VSS	VOID	VOID	VDD	VSS	VDD	MA_DATA[58]	MA_DATA[63]	MA_DQS_L[7]	MA_DATA[56]	AE
AF	L0_CADOUT_H[2]	VSS	VSS	L0_CADOUT_L[10]	L0_CADOUT_H[10]	L0_CADOUT_H[11]	VDD	VSS	VDD	VSS	VDD	VSS	MB_DATA[59]	VSS	MA_DM[7]	VSS	AF
AG	L0_CADOUT_L[0]	L0_CADOUT_H[1]	L0_CADOUT_L[1]	VDD	VDD	L0_CADOUT_L[9]	VDD	THERMDA	THERMDC	VSS	VSS	VDDR	MB_DATA[58]	MA_DATA[62]	MA_DATA[57]	MA_DATA[61]	AG
AH	L0_CADOUT_H[0]	VDD	VDD	L0_CADOUT_L[8]	L0_CADOUT_H[8]	L0_CADOUT_H[9]	TEST3	TEST23	TEST12	TCK	M_2N	VDDR	MB_DATA[63]	VSS	MB_DATA[51]	VSS	AH
AJ	VLDT_A	VLDT_A	VLDT_A	VLDT_A	TEST6	TEST2	TEST13	TEST20	TEST22	TRST_L	M_2P	VDDR	MB_DQS_L[7]	MB_DM[7]	MB_DATA[60]	MB_DATA[50]	AJ
AK	VCID	VSS	RSVD	SA[0]	TEST26	SID	THERMTRIP_L	TEST24	TEST27	TDO	VDDIO_FB_H	VDDR	MB_DQS_H[7]	VSS	MB_DATA[56]	VSS	AK
AL	VCID	VCID	CPU_PRESENT_L	ALERT_L	VSS	SIC	PROCHOT_L	TEST21	TMS	TDI	VDDIO_FB_L	VDDR	MB_DATA[62]	MB_DATA[57]	MB_DATA[61]	MB_DATA[55]	AL
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 1. Connection Diagram (Left Half)

1.2 Connection Diagram (Right Half)

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
A	MB_DATA[9]	MB_CLK_H[1]	MB_CLK_L[1]	MB_DATA[14]	MB_DATA[10]	MB_DATA[16]	MB_DM[2]	MB_DATA[22]	MB_DATA[23]	MB_DATA[19]	MB_DATA[28]	MB_DATA[24]	MB_DATA[25]	VOID	VOID	A
B	MB_DM[1]	VSS	MB_RESET_L	VSS	MB_DATA[15]	VSS	MB_DATA[17]	VSS	MB_DATA[18]	VSS	MB_DATA[29]	VSS	MA_DM[3]	VSS	VOID	B
C	MB_DQS_L[1]	RSVD	MB_CLK_H[0]	RSVD	MB_DATA[11]	MB_DATA[21]	MB_DQS_L[2]	MB_DQS_H[2]	MA_DQS_H[2]	MA_DATA[18]	MA_DATA[28]	MA_DATA[25]	MA_DQS_L[3]	MB_DM[3]	MB_DQS_L[3]	C
D	MB_DQS_H[1]	VSS	MB_CLK_L[0]	VSS	MB_DATA[20]	VSS	MA_DATA[20]	VSS	MA_DQS_L[2]	VSS	MA_DATA[29]	VSS	MA_DQS_H[3]	VSS	MB_DQS_H[3]	D
E	MA_DATA[8]	MA_DM[1]	MA_DQS_H[1]	MA_RESET_L	MA_DATA[14]	MA_DATA[15]	MA_DATA[21]	MA_DM[2]	MA_DATA[22]	MA_DATA[19]	MA_DATA[24]	MA_DATA[30]	MA_DATA[31]	MB_DATA[30]	MB_DATA[31]	E
F	MA_DATA[13]	VSS	MA_DQS_L[1]	VSS	MA_DATA[10]	VSS	MA_DATA[16]	VSS	MA_DATA[23]	VSS	MA_DATA[26]	VSS	MB_DATA[27]	VSS	MB_DATA[26]	F
G	MA_DATA[12]	MA_DATA[9]	MA_CLK_H[1]	MA_CLK_H[0]	MA_CLK_L[0]	MA_DATA[11]	MA_DATA[17]	RSVD	RSVD	MA_DATA[27]	MA_CHECK[4]	MA_CHECK[5]	MB_CHECK[4]	MB_CHECK[5]	MB_CHECK[0]	G
H	MA_DATA[3]	VSS	MA_CLK_L[1]	NP/ VSS	VOID	VOID	VDD	VSS	RSVD	VSS	MA_CHECK[0]	VSS	MA_CHECK[1]	VSS	MB_CHECK[1]	H
J	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	MA_DM[8]	MA_CHECK[6]	MA_DQS_L[8]	MA_DQS_H[8]	MB_DM[8]	MB_DQS_L[8]	MB_DQS_H[8]	J
K	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CHECK[7]	VSS	MA_CHECK[2]	VSS	MB_CHECK[7]	VSS	MB_CHECK[6]	K
L	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CHECK[3]	RSVD	RSVD	MA_CKE[1]	MB_CHECK[2]	MB_CHECK[3]	RSVD	RSVD	L
M	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_CKE[0]	VDDIO	MA_ADD[15]	VDDIO	MB_CKE[0]	VDDIO	MB_CKE[1]	M
N	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[14]	MA_BANK[2]	MA_ADD[12]	MA_ADD[9]	MB_ADD[15]	MB_ADD[14]	MB_ADD[12]	MB_BANK[2]	N
P	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[11]	VDDIO	MA_ADD[7]	VDDIO	MB_ADD[11]	VDDIO	MB_ADD[9]	P
R	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[8]	MA_ADD[6]	MA_ADD[5]	MA_ADD[4]	MB_ADD[7]	MB_ADD[8]	MB_ADD[5]	MB_ADD[6]	R
T	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[3]	VDDIO	MA_ADD[1]	VDDIO	MB_ADD[3]	VDDIO	MB_ADD[4]	T
U	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CLK_H[2]	MA_ADD[2]	MA_CLK_L[5]	MA_CLK_H[5]	MB_ADD[1]	MB_ADD[2]	MB_CLK_L[5]	MB_CLK_H[5]	U
V	VDD	VSS	VDD	VSS	VDD	VSS	VDD	MA_CLK_L[2]	VDDIO	VDDIO	MA_CLK_H[4]	VDDIO	MB_EVENT_L	VDDIO	MB_CLK_H[2]	V
W	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[0]	MA_CLK_L[3]	MA_CLK_H[3]	MA_CLK_L[4]	MB_CLK_L[4]	MB_CLK_H[4]	MA_EVENT_L	MB_CLK_L[2]	W
Y	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[10]	VDDIO	MA_BANK[1]	VDDIO	VDDIO	MB_CLK_L[3]	MB_CLK_H[3]	Y
AA	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA0_CS_L[0]	MA1_CS_L[0]	MA_RAS_L	MA_BANK[0]	MB_BANK[0]	MB_ADD[10]	MB_ADD[0]	MB_BANK[1]	AA
AB	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_CAS_L	VDDIO	MA_WE_L	VDDIO	MB_RAS_L	VDDIO	MB1_CS_L[0]	AB
AC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	MA0_CS_L[1]	MA_ADD[13]	MA1_ODT[0]	MA0_ODT[0]	MB_CAS_L	MB_WE_L	MB0_CS_L[0]	AC
AD	MA_DATA[60]	VOID	VOID	VSS	MA_DATA[53]	VSS	VDD	VSS	RSVD	VDDIO	MA1_CS_L[1]	VDDIO	MB0_ODT[0]	VDDIO	MB1_ODT[0]	AD
AE	MA_DATA[51]	MA_DATA[54]	MA_CLK_L[6]	MA_CLK_H[6]	MA_DATA[48]	MA_DATA[43]	MA_DATA[46]	RSVD	RSVD	MA_DATA[36]	MA1_ODT[1]	MA0_ODT[1]	MB1_CS_L[1]	MB0_CS_L[1]	MB_ADD[13]	AE
AF	MA_DATA[50]	VSS	MA_DM[6]	VSS	MA_DATA[49]	VSS	MA_DATA[47]	VSS	MA_DATA[40]	VSS	MA_DATA[32]	VSS	MA_DATA[37]	VDDIO	MB0_ODT[1]	AF
AG	MA_DATA[55]	MA_DQS_H[6]	MA_DQS_L[6]	MA_CLK_L[7]	MA_CLK_H[7]	MA_DATA[52]	MA_DATA[42]	MA_DQS_H[5]	MA_DQS_L[5]	MA_DATA[44]	MA_DQS_H[4]	MA_DQS_L[4]	MA_DATA[33]	MB_DATA[36]	MB1_ODT[1]	AG
AH	MB_DM[6]	VSS	MB_DATA[49]	VSS	MB_DATA[42]	VSS	MB_DATA[41]	VSS	MA_DATA[41]	VSS	MA_DATA[34]	VSS	MA_DM[4]	VSS	MB_DATA[37]	AH
AJ	MB_DQS_L[6]	RSVD	MB_CLK_H[7]	RSVD	MB_DATA[43]	MB_DATA[47]	MB_DM[5]	MB_DATA[40]	MA_DM[5]	MA_DATA[45]	MA_DATA[35]	MA_DATA[39]	MA_DATA[38]	MB_DATA[33]	MB_DATA[32]	AJ
AK	MB_DQS_H[6]	VSS	MB_CLK_L[7]	VSS	MB_DATA[53]	VSS	MB_DQS_H[5]	VSS	MB_DATA[44]	VSS	MB_DATA[38]	VSS	MB_DM[4]	VSS	VOID	AK
AL	MB_DATA[54]	MB_CLK_L[6]	MB_CLK_H[6]	MB_DATA[48]	MB_DATA[52]	MB_DATA[46]	MB_DQS_L[5]	MB_DATA[45]	MB_DATA[35]	MB_DATA[34]	MB_DATA[39]	MB_DQS_H[4]	MB_DQS_L[4]	VOID	VOID	AL
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 2. Connection Diagram (Right Half)

1.3 Pin Types

Table 1. Pin Types

Pin Types	
I-HT-D	Input, HyperTransport™ Technology, Differential
O-HT-D	Output, HyperTransport Technology, Differential
B-IO-S	Bidirectional, VDDIO, Single-Ended
B-IO-OD	Bidirectional, VDDIO, Open Drain
B-IO-D	Bidirectional, VDDIO, Differential
I-IO-S	Input, VDDIO, Single-Ended
I-IO-D	Input, VDDIO, Differential
O-IO-D	Output, VDDIO, Differential
O-IO-S	Output, VDDIO, Single-Ended
O-IO-OD	Output, VDDIO, Open Drain
A	Analog
S	Supply Voltage
VREF	Voltage Reference

1.4 Pin Descriptions

Table 2. HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT-D	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT-D	Link 0 Control Input
L0_CADIN_H/L[15:0]	I-HT-D	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT-D	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT-D	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT-D	Link 0 Command/Address/Data Outputs
HTREF1	A	Compensation Resistor to VLDT
HTREF0	A	Compensation Resistor to VSS

Table 3. DDR2 SDRAM Memory Interface Pin Descriptions (Supports DDR2 and DDR3)[1]

Signal Name	Type	Description
MA_CLK_H/L[7:0], MB_CLK_H/L[7:0]	O-IO-D	DRAM Differential Clock
MA0_CS_L[1:0], MA1_CS_L[1:0], MB0_CS_L[1:0], MB1_CS_L[1:0]	O-IO-S	DRAM Chip Selects
MA0_ODT[1:0], MA1_ODT[1:0], MB0_ODT[1:0], MB1_ODT[1:0]	O-IO-S	DRAM Enable Pin for On Die Termination
MA_CKE[1:0], MB_CKE[1:0]	O-IO-S	DRAM Clock Enable
MA_DQS_H/L[8:0], MB_DQS_H/L[8:0]	B-IO-D	DRAM Differential Data Strobe
MA_DATA[63:0], MB_DATA[63:0]	B-IO-S	DRAM Interface Data Bus
MA_DM[8:0], MB_DM[8:0]	O-IO-S	DRAM Data Mask Bits
MA_CHECK[7:0], MB_CHECK[7:0]	B-IO-S	DRAM Interface ECC Check Bits
MA_RAS_L, MB_RAS_L	O-IO-S	DRAM Row Address Strobe
MA_CAS_L, MB_CAS_L	O-IO-S	DRAM Column Address Strobe
MA_WE_L, MB_WE_L	O-IO-S	DRAM Write Enable
MA_ADD[15:0], MB_ADD[15:0]	O-IO-S	DRAM Column/Row Address
MA_BANK[2:0], MB_BANK[2:0]	O-IO-S	DRAM Bank Address
MA_RESET_L, MB_RESET_L	O-IO-S	DRAM Reset Pin for Suspend-to-RAM Power Management Mode
MA_EVENT_L, MB_EVENT_L	I-IO-S	DRAM Thermal Event Status
M_VREF	VREF	DRAM Interface Voltage Reference
M_ZP	A	Compensation Resistor to VSS
M_ZN	A	Compensation Resistor to VDDIO
M_VDDIO_PWRGD	I-IO-S	Not Supported

Note:

1. Support for DDR2 or DDR3 depends on platform implementation.

Table 4. Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IO-D	200-MHz PLL Reference Clock

Table 5. Thermal Observation/Control Pin Descriptions

Signal Name	Type	Description
PROCHOT_L	B-IO-OD	Asserted as an input to force the processor into the HTC-active state or becomes asserted as an output to indicate when the processor has entered the HTC-active state.
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output
SIC	I-IO-S	Sideband-Temperature Sensor Interface Clock
SID	B-IO-OD	Sideband-Temperature Sensor Interface Data
ALERT_L	O-IO-S	Programmable pin that can indicate different events, including a Sideband-Temperature Sensor Interface interrupt.
SA[0]	I-IO-S	Sideband interface address

Table 6. Power Supply/Voltage Regulator Interface Pin Descriptions

Signal Name	Type	Notes	Description
PSI_L	O-IO-S		Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve efficiency when the processor is in low power states.
VDD_FB_H/L	A		Differential feedback for VDD power supply
VDDNB_FB_H/L	A		Differential feedback for VDDNB power supply
VDDIO_FB_H/L	A		Differential feedback for VDDIO power supply
VDDA	S		Filtered PLL supply voltage
VDD	S		Core power supply
VDDNB	S		Northbridge power supply
VDDIO	S		DDR SDRAM I/O ring power supply
VLDT_A, VLDT_B	S		HyperTransport™ I/O ring power supply
VDDR	S		VDDR power supply
VDDR_SENSE	A		VDDR voltage monitor pin
VSS	S		Ground
PVIEN/VID[1]	B-IO-OD	1	Prior to PWROK assertion, PVIEN/VID[1] signals to the processor whether the platform supports PVI or SVI operation. After PWROK assertion, on a platform that implements the parallel VID interface, this pin is bit 1 of the VID interface. This pin is not used after PWROK assertion on platforms that implement the serial VID interface.
SVD/VID[2]	B-IO-OD	1	In platforms supporting SVI, this signal is the serial VID interface data. In platforms supporting PVI, this signal is bit 2 of the parallel voltage ID to the regulator.
SVC/VID[3]	O-IO-S	1	In platforms supporting SVI, this signal is the serial VID interface clock. In platforms supporting PVI, this signal is bit 3 of the parallel voltage ID to the regulator.
VID[5:4], VID[0]	O-IO-S	1	Voltage ID pins to the regulator

Note:

1. The function of this pin is platform implementation dependant. For information on how to connect this pin, please refer to the appropriate motherboard design guide.

Table 7. JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IO-S	JTAG Clock
TMS	I-IO-S	JTAG Mode Select
TRST_L	I-IO-S	JTAG Reset
TDI	I-IO-S	JTAG Data Input
TDO	O-IO-S	JTAG Data Output

Table 8. Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IO-S	Debug Request
DBRDY	O-IO-S	Debug Ready

Table 9. Miscellaneous Pin Descriptions

Signal Name	Type	Description
CPU_PRESENT_L	O-IO-S	Indicates a processor is present for a socket. Shorted to VSS on the package.
RESET_L	I-IO-S	Processor Reset
PWROK	I-IO-S	Indicates that voltages and input CLKIN have reached specified operation.
LDTSTOP_L	I-IO-S	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
CORE_TYPE	O-IO-S	Indicates that the processor is capable of split Northbridge and core voltage plane operation. If open, the processor requires a unified core and Northbridge voltage plane. If shorted to VSS, split core and Northbridge voltage plan operation is supported.
VOID	Missing pins on package and socket used for mechanical keying.	
RSVD	Reserved pins that should remain unconnected.	
NP/VSS	Pin is not populated on the package but socket hole connects to ground.	
NP/RSVD	Pin is not populated on the package but socket contains a hole that should remain unconnected.	
TEST*	Refer to *Socket AM3 Motherboard Design Guide*, order #40837	

1.5 Alphabetical Pin List

Name	Pin	Name	Pin	Name	Pin	Name	Pin
ALERT_L	AL4	L0_CADOUT_H[3]	AE2	MA_ADD[14]	N24	MA_DATA[18]	C26
CLKIN_H	A8	L0_CADOUT_H[4]	AC2	MA_ADD[15]	M27	MA_DATA[19]	E26
CLKIN_L	B8	L0_CADOUT_H[5]	AB1	MA_ADD[2]	U25	MA_DATA[2]	E16
CORE_TYPE	G5	L0_CADOUT_H[6]	AA2	MA_ADD[3]	T25	MA_DATA[20]	D23
CPU_PRESENT_L	AL3	L0_CADOUT_H[7]	Y1	MA_ADD[4]	R27	MA_DATA[21]	E23
DBRDY	B6	L0_CADOUT_H[8]	AH5	MA_ADD[5]	R26	MA_DATA[22]	E25
DBREQ_L	A5	L0_CADOUT_H[9]	AH6	MA_ADD[6]	R25	MA_DATA[23]	F25
HTREF0	V7	L0_CADOUT_L[0]	AG1	MA_ADD[7]	P27	MA_DATA[24]	E27
HTREF1	V8	L0_CADOUT_L[1]	AG3	MA_ADD[8]	R24	MA_DATA[25]	C28
L0_CADIN_H[0]	J3	L0_CADOUT_L[10]	AF4	MA_ADD[9]	N27	MA_DATA[26]	F27
L0_CADIN_H[1]	J1	L0_CADOUT_L[11]	AE6	MA_BANK[0]	AA27	MA_DATA[27]	G26
L0_CADIN_H[10]	L6	L0_CADOUT_L[12]	AC6	MA_BANK[1]	Y27	MA_DATA[28]	C27
L0_CADIN_H[11]	M4	L0_CADOUT_L[13]	AB4	MA_BANK[2]	N25	MA_DATA[29]	D27
L0_CADIN_H[12]	P4	L0_CADOUT_L[14]	AA6	MA_CAS_L	AB25	MA_DATA[3]	H17
L0_CADIN_H[13]	R6	L0_CADOUT_L[15]	Y4	MA_CHECK[0]	H27	MA_DATA[30]	E28
L0_CADIN_H[14]	T4	L0_CADOUT_L[2]	AE1	MA_CHECK[1]	H29	MA_DATA[31]	E29
L0_CADIN_H[15]	U6	L0_CADOUT_L[3]	AE3	MA_CHECK[2]	K27	MA_DATA[32]	AF27
L0_CADIN_H[2]	L3	L0_CADOUT_L[4]	AC3	MA_CHECK[3]	L24	MA_DATA[33]	AG29
L0_CADIN_H[3]	L1	L0_CADOUT_L[5]	AA1	MA_CHECK[4]	G27	MA_DATA[34]	AH27
L0_CADIN_H[4]	N1	L0_CADOUT_L[6]	AA3	MA_CHECK[5]	G28	MA_DATA[35]	AJ27
L0_CADIN_H[5]	R3	L0_CADOUT_L[7]	W1	MA_CHECK[6]	J26	MA_DATA[36]	AE26
L0_CADIN_H[6]	R1	L0_CADOUT_L[8]	AH4	MA_CHECK[7]	K25	MA_DATA[37]	AF29
L0_CADIN_H[7]	U3	L0_CADOUT_L[9]	AG6	MA_CKE[0]	M25	MA_DATA[38]	AJ29
L0_CADIN_H[8]	J6	L0_CLKIN_H[0]	N3	MA_CKE[1]	L27	MA_DATA[39]	AJ28
L0_CADIN_H[9]	K4	L0_CLKIN_H[1]	N6	MA_CLK_H[0]	G20	MA_DATA[4]	H13
L0_CADIN_L[0]	J2	L0_CLKIN_L[0]	N2	MA_CLK_H[1]	G19	MA_DATA[40]	AF25
L0_CADIN_L[1]	K1	L0_CLKIN_L[1]	P6	MA_CLK_H[2]	U24	MA_DATA[41]	AH25
L0_CADIN_L[10]	M6	L0_CLKOUT_H[0]	AD1	MA_CLK_H[3]	W26	MA_DATA[42]	AG23
L0_CADIN_L[11]	M5	L0_CLKOUT_H[1]	AD5	MA_CLK_H[4]	V27	MA_DATA[43]	AE22
L0_CADIN_L[12]	P5	L0_CLKOUT_L[0]	AC1	MA_CLK_H[5]	U27	MA_DATA[44]	AG26
L0_CADIN_L[13]	T6	L0_CLKOUT_L[1]	AD4	MA_CLK_H[6]	AE20	MA_DATA[45]	AJ26
L0_CADIN_L[14]	T5	L0_CTLIN_H[0]	U1	MA_CLK_H[7]	AG21	MA_DATA[46]	AE23
L0_CADIN_L[15]	V6	L0_CTLIN_H[1]	V4	MA_CLK_L[0]	G21	MA_DATA[47]	AF23
L0_CADIN_L[2]	L2	L0_CTLIN_L[0]	V1	MA_CLK_L[1]	H19	MA_DATA[48]	AE21
L0_CADIN_L[3]	M1	L0_CTLIN_L[1]	V5	MA_CLK_L[2]	V24	MA_DATA[49]	AF21
L0_CADIN_L[4]	P1	L0_CTLOUT_H[0]	W2	MA_CLK_L[3]	W25	MA_DATA[5]	G13
L0_CADIN_L[5]	R2	L0_CTLOUT_H[1]	Y6	MA_CLK_L[4]	W27	MA_DATA[50]	AF17
L0_CADIN_L[6]	T1	L0_CTLOUT_L[0]	W3	MA_CLK_L[5]	U26	MA_DATA[51]	AE17
L0_CADIN_L[7]	U2	L0_CTLOUT_L[1]	W6	MA_CLK_L[6]	AE19	MA_DATA[52]	AG22
L0_CADIN_L[8]	K6	LDTSTOP_L	D8	MA_CLK_L[7]	AG20	MA_DATA[53]	AD21
L0_CADIN_L[9]	K5	M_VDDIO_PWRGD	F3	MA_DATA[0]	G14	MA_DATA[54]	AE18
L0_CADOUT_H[0]	AH1	M_VREF	F12	MA_DATA[1]	E14	MA_DATA[55]	AG17
L0_CADOUT_H[1]	AG2	M_ZN	AH11	MA_DATA[10]	F21	MA_DATA[56]	AE16
L0_CADOUT_H[10]	AF5	M_ZP	AJ11	MA_DATA[11]	G22	MA_DATA[57]	AG15
L0_CADOUT_H[11]	AF6	MA_ADD[0]	W24	MA_DATA[12]	G17	MA_DATA[58]	AE13
L0_CADOUT_H[12]	AD6	MA_ADD[1]	T27	MA_DATA[13]	F17	MA_DATA[59]	AD13
L0_CADOUT_H[13]	AB5	MA_ADD[10]	Y25	MA_DATA[14]	E21	MA_DATA[6]	E15
L0_CADOUT_H[14]	AB6	MA_ADD[11]	P25	MA_DATA[15]	E22	MA_DATA[60]	AD17
L0_CADOUT_H[15]	Y5	MA_ADD[12]	N26	MA_DATA[16]	F23	MA_DATA[61]	AG16
L0_CADOUT_H[2]	AF1	MA_ADD[13]	AC26	MA_DATA[17]	G23	MA_DATA[62]	AG14

Name	Pin	Name	Pin	Name	Pin	Name	Pin
MA_DATA[63]	AE14	MB_ADD[15]	N28	MB_DATA[19]	A26	MB_DATA[7]	B15
MA_DATA[7]	G16	MB_ADD[2]	U29	MB_DATA[2]	A15	MB_DATA[8]	A16
MA_DATA[8]	E17	MB_ADD[3]	T29	MB_DATA[20]	D21	MB_DATA[9]	A17
MA_DATA[9]	G18	MB_ADD[4]	T31	MB_DATA[21]	C22	MB_DM[0]	B13
MA_DM[0]	H15	MB_ADD[5]	R30	MB_DATA[22]	A24	MB_DM[1]	B17
MA_DM[1]	E18	MB_ADD[6]	R31	MB_DATA[23]	A25	MB_DM[2]	A23
MA_DM[2]	E24	MB_ADD[7]	R28	MB_DATA[24]	A28	MB_DM[3]	C30
MA_DM[3]	B29	MB_ADD[8]	R29	MB_DATA[25]	A29	MB_DM[4]	AK29
MA_DM[4]	AH29	MB_ADD[9]	P31	MB_DATA[26]	F31	MB_DM[5]	AJ23
MA_DM[5]	AJ25	MB_BANK[0]	AA28	MB_DATA[27]	F29	MB_DM[6]	AH17
MA_DM[6]	AF19	MB_BANK[1]	AA31	MB_DATA[28]	A27	MB_DM[7]	AJ14
MA_DM[7]	AF15	MB_BANK[2]	N31	MB_DATA[29]	B27	MB_DM[8]	J29
MA_DM[8]	J25	MB_CAS_L	AC29	MB_DATA[3]	C15	MB_DQS_H[0]	C14
MA_DQS_H[0]	F15	MB_CHECK[0]	G31	MB_DATA[30]	E30	MB_DQS_H[1]	D17
MA_DQS_H[1]	E19	MB_CHECK[1]	H31	MB_DATA[31]	E31	MB_DQS_H[2]	C24
MA_DQS_H[2]	C25	MB_CHECK[2]	L28	MB_DATA[32]	AJ31	MB_DQS_H[3]	D31
MA_DQS_H[3]	D29	MB_CHECK[3]	L29	MB_DATA[33]	AJ30	MB_DQS_H[4]	AL28
MA_DQS_H[4]	AG27	MB_CHECK[4]	G29	MB_DATA[34]	AL26	MB_DQS_H[5]	AK23
MA_DQS_H[5]	AG24	MB_CHECK[5]	G30	MB_DATA[35]	AL25	MB_DQS_H[6]	AK17
MA_DQS_H[6]	AG18	MB_CHECK[6]	K31	MB_DATA[36]	AG30	MB_DQS_H[7]	AK13
MA_DQS_H[7]	AD15	MB_CHECK[7]	K29	MB_DATA[37]	AH31	MB_DQS_H[8]	J31
MA_DQS_H[8]	J28	MB_CKE[0]	M29	MB_DATA[38]	AK27	MB_DQS_L[0]	C13
MA_DQS_L[0]	G15	MB_CKE[1]	M31	MB_DATA[39]	AL27	MB_DQS_L[1]	C17
MA_DQS_L[1]	F19	MB_CLK_H[0]	C19	MB_DATA[4]	F13	MB_DQS_L[2]	C23
MA_DQS_L[2]	D25	MB_CLK_H[1]	A18	MB_DATA[40]	AJ24	MB_DQS_L[3]	C31
MA_DQS_L[3]	C29	MB_CLK_H[2]	V31	MB_DATA[41]	AH23	MB_DQS_L[4]	AL29
MA_DQS_L[4]	AG28	MB_CLK_H[3]	Y31	MB_DATA[42]	AH21	MB_DQS_L[5]	AL23
MA_DQS_L[5]	AG25	MB_CLK_H[4]	W29	MB_DATA[43]	AJ21	MB_DQS_L[6]	AJ17
MA_DQS_L[6]	AG19	MB_CLK_H[5]	U31	MB_DATA[44]	AK25	MB_DQS_L[7]	AJ13
MA_DQS_L[7]	AE15	MB_CLK_H[6]	AL19	MB_DATA[45]	AL24	MB_DQS_L[8]	J30
MA_DQS_L[8]	J27	MB_CLK_H[7]	AJ19	MB_DATA[46]	AL22	MB_EVENT_L	V29
MA_EVENT_L	W30	MB_CLK_L[0]	D19	MB_DATA[47]	AJ22	MB_RAS_L	AB29
MA_RAS_L	AA26	MB_CLK_L[1]	A19	MB_DATA[48]	AL20	MB_RESET_L	B19
MA_RESET_L	E20	MB_CLK_L[2]	W31	MB_DATA[49]	AH19	MB_WE_L	AC30
MA_WE_L	AB27	MB_CLK_L[3]	Y30	MB_DATA[5]	E13	MB0_CS_L[0]	AC31
MA0_CS_L[0]	AA24	MB_CLK_L[4]	W28	MB_DATA[50]	AJ16	MB0_CS_L[1]	AE30
MA0_CS_L[1]	AC25	MB_CLK_L[5]	U30	MB_DATA[51]	AH15	MB0_ODT[0]	AD29
MA0_ODT[0]	AC28	MB_CLK_L[6]	AL18	MB_DATA[52]	AL21	MB0_ODT[1]	AF31
MA0_ODT[1]	AE28	MB_CLK_L[7]	AK19	MB_DATA[53]	AK21	MB1_CS_L[0]	AB31
MA1_CS_L[0]	AA25	MB_DATA[0]	D13	MB_DATA[54]	AL17	MB1_CS_L[1]	AE29
MA1_CS_L[1]	AD27	MB_DATA[1]	A13	MB_DATA[55]	AL16	MB1_ODT[0]	AD31
MA1_ODT[0]	AC27	MB_DATA[10]	A21	MB_DATA[56]	AK15	MB1_ODT[1]	AG31
MA1_ODT[1]	AE27	MB_DATA[11]	C21	MB_DATA[57]	AL14	NP/RSVD	B2
MB_ADD[0]	AA30	MB_DATA[12]	D15	MB_DATA[58]	AG13	NP/VSS	AE7
MB_ADD[1]	U28	MB_DATA[13]	C16	MB_DATA[59]	AF13	NP/VSS	H20
MB_ADD[10]	AA29	MB_DATA[14]	A20	MB_DATA[6]	A14	PROCHOT_L	AL7
MB_ADD[11]	P29	MB_DATA[15]	B21	MB_DATA[60]	AJ15	PSI_L	F1
MB_ADD[12]	N30	MB_DATA[16]	A22	MB_DATA[61]	AL15	PVIEN/VID[1]	E2
MB_ADD[13]	AE31	MB_DATA[17]	B23	MB_DATA[62]	AL13	PWROK	C9
MB_ADD[14]	N29	MB_DATA[18]	B25	MB_DATA[63]	AH13	RESET_L	C7

Name	Pin	Name	Pin	Name	Pin	Name	Pin
RSVD	AD25	TEST8	D4	VDD	B3	VDD	M7
RSVD	AE24	TEST9	F6	VDD	C2	VDD	M9
RSVD	AE25	THERMDA	AG8	VDD	C4	VDD	N10
RSVD	AJ18	THERMDC	AG9	VDD	D3	VDD	N12
RSVD	AJ20	THERMTRIP_L	AK7	VDD	D5	VDD	N14
RSVD	AK3	TMS	AL9	VDD	E4	VDD	N16
RSVD	C18	TRST_L	AJ10	VDD	E6	VDD	N18
RSVD	C20	VDD	AA10	VDD	F5	VDD	N20
RSVD	F2	VDD	AA12	VDD	F7	VDD	N22
RSVD	G24	VDD	AA14	VDD	G6	VDD	N8
RSVD	G25	VDD	AA16	VDD	G8	VDD	P11
RSVD	H25	VDD	AA18	VDD	H11	VDD	P13
RSVD	L25	VDD	AA20	VDD	H23	VDD	P15
RSVD	L26	VDD	AA22	VDD	H7	VDD	P17
RSVD	L30	VDD	AA8	VDD	J12	VDD	P19
RSVD	L31	VDD	AB11	VDD	J14	VDD	P21
SA[0]	AK4	VDD	AB13	VDD	J16	VDD	P23
SIC	AL6	VDD	AB15	VDD	J18	VDD	P7
SID	AK6	VDD	AB17	VDD	J20	VDD	P9
SVC/VID[3]	C1	VDD	AB19	VDD	J22	VDD	R10
SVD/VID[2]	E3	VDD	AB21	VDD	J24	VDD	R12
TCK	AH10	VDD	AB23	VDD	J8	VDD	R14
TDI	AL10	VDD	AB7	VDD	K11	VDD	R16
TDO	AK10	VDD	AB9	VDD	K13	VDD	R18
TEST10	G7	VDD	AC10	VDD	K15	VDD	R20
TEST12	AH9	VDD	AC12	VDD	K17	VDD	R22
TEST13	AJ7	VDD	AC14	VDD	K19	VDD	R4
TEST14	C5	VDD	AC16	VDD	K21	VDD	R5
TEST15	F8	VDD	AC18	VDD	K23	VDD	R8
TEST16	E7	VDD	AC20	VDD	K7	VDD	T11
TEST17	D6	VDD	AC22	VDD	K9	VDD	T13
TEST18	E9	VDD	AC4	VDD	L10	VDD	T15
TEST19	F10	VDD	AC5	VDD	L12	VDD	T17
TEST2	AJ6	VDD	AC8	VDD	L14	VDD	T19
TEST20	AJ8	VDD	AD11	VDD	L16	VDD	T2
TEST21	AL8	VDD	AD2	VDD	L18	VDD	T21
TEST22	AJ9	VDD	AD23	VDD	L20	VDD	T23
TEST23	AH8	VDD	AD3	VDD	L22	VDD	T3
TEST24	AK8	VDD	AD7	VDD	L4	VDD	T7
TEST25_H	A10	VDD	AD9	VDD	L5	VDD	T9
TEST25_L	B10	VDD	AE10	VDD	L8	VDD	U10
TEST26	AK5	VDD	AE12	VDD	M11	VDD	U12
TEST27	AK9	VDD	AF11	VDD	M13	VDD	U14
TEST28_H	J10	VDD	AF7	VDD	M15	VDD	U16
TEST28_L	H9	VDD	AF9	VDD	M17	VDD	U18
TEST29_H	C11	VDD	AG4	VDD	M19	VDD	U20
TEST29_L	D11	VDD	AG5	VDD	M2	VDD	U22
TEST3	AH7	VDD	AG7	VDD	M21	VDD	U8
TEST6	AJ5	VDD	AH2	VDD	M23	VDD	V11
TEST7	E5	VDD	AH3	VDD	M3	VDD	V13

Name	Pin	Name	Pin	Name	Pin	Name	Pin
VDD	V15	VDDIO	T28	VOID	A2	VSS	AC23
VDD	V17	VDDIO	T30	VOID	A30	VSS	AC7
VDD	V19	VDDIO	V25	VOID	A31	VSS	AC9
VDD	V21	VDDIO	V26	VOID	AD18	VSS	AD10
VDD	V23	VDDIO	V28	VOID	AD19	VSS	AD12
VDD	V9	VDDIO	V30	VOID	AE8	VSS	AD14
VDD	W10	VDDIO	Y24	VOID	AE9	VSS	AD16
VDD	W12	VDDIO	Y26	VOID	AK1	VSS	AD20
VDD	W14	VDDIO	Y28	VOID	AK31	VSS	AD22
VDD	W16	VDDIO	Y29	VOID	AL1	VSS	AD24
VDD	W18	VDDIO_FB_H	AK11	VOID	AL2	VSS	AD8
VDD	W20	VDDIO_FB_L	AL11	VOID	AL30	VSS	AE11
VDD	W22	VDDNB	A4	VOID	AL31	VSS	AE4
VDD	W4	VDDNB	A6	VOID	B1	VSS	AE5
VDD	W5	VDDNB	B5	VOID	B31	VSS	AF10
VDD	W8	VDDNB	B7	VOID	H21	VSS	AF12
VDD	Y11	VDDNB	C6	VOID	H22	VSS	AF14
VDD	Y13	VDDNB	C8	VOID	H3	VSS	AF16
VDD	Y15	VDDNB	D7	VOID	H4	VSS	AF18
VDD	Y17	VDDNB	D9	VSS	A11	VSS	AF2
VDD	Y19	VDDNB	E10	VSS	A3	VSS	AF20
VDD	Y2	VDDNB	E8	VSS	A7	VSS	AF22
VDD	Y21	VDDNB	F11	VSS	A9	VSS	AF24
VDD	Y23	VDDNB	F9	VSS	AA11	VSS	AF26
VDD	Y3	VDDNB	G10	VSS	AA13	VSS	AF28
VDD	Y7	VDDNB	G12	VSS	AA15	VSS	AF3
VDD	Y9	VDDNB_FB_H	G4	VSS	AA17	VSS	AF8
VDD_FB_H	G2	VDDNB_FB_L	G3	VSS	AA19	VSS	AG10
VDD_FB_L	G1	VDDR	A12	VSS	AA21	VSS	AG11
VDDA	C10	VDDR	AG12	VSS	AA23	VSS	AH14
VDDA	D10	VDDR	AH12	VSS	AA4	VSS	AH16
VDDIO	AB24	VDDR	AJ12	VSS	AA5	VSS	AH18
VDDIO	AB26	VDDR	AK12	VSS	AA7	VSS	AH20
VDDIO	AB28	VDDR	AL12	VSS	AA9	VSS	AH22
VDDIO	AB30	VDDR	B12	VSS	AB10	VSS	AH24
VDDIO	AC24	VDDR	C12	VSS	AB12	VSS	AH26
VDDIO	AD26	VDDR	D12	VSS	AB14	VSS	AH28
VDDIO	AD28	VDDR_SENSE	E12	VSS	AB16	VSS	AH30
VDDIO	AD30	VID[0]	E1	VSS	AB18	VSS	AK14
VDDIO	AF30	VID[4]	D1	VSS	AB2	VSS	AK16
VDDIO	M24	VID[5]	D2	VSS	AB20	VSS	AK18
VDDIO	M26	VLDT_A	AJ1	VSS	AB22	VSS	AK2
VDDIO	M28	VLDT_A	AJ2	VSS	AB3	VSS	AK20
VDDIO	M30	VLDT_A	AJ3	VSS	AB8	VSS	AK22
VDDIO	P24	VLDT_A	AJ4	VSS	AC11	VSS	AK24
VDDIO	P26	VLDT_B	H1	VSS	AC13	VSS	AK26
VDDIO	P28	VLDT_B	H2	VSS	AC15	VSS	AK28
VDDIO	P30	VLDT_B	H5	VSS	AC17	VSS	AK30
VDDIO	T24	VLDT_B	H6	VSS	AC19	VSS	AL5
VDDIO	T26	VOID	A1	VSS	AC21	VSS	B11

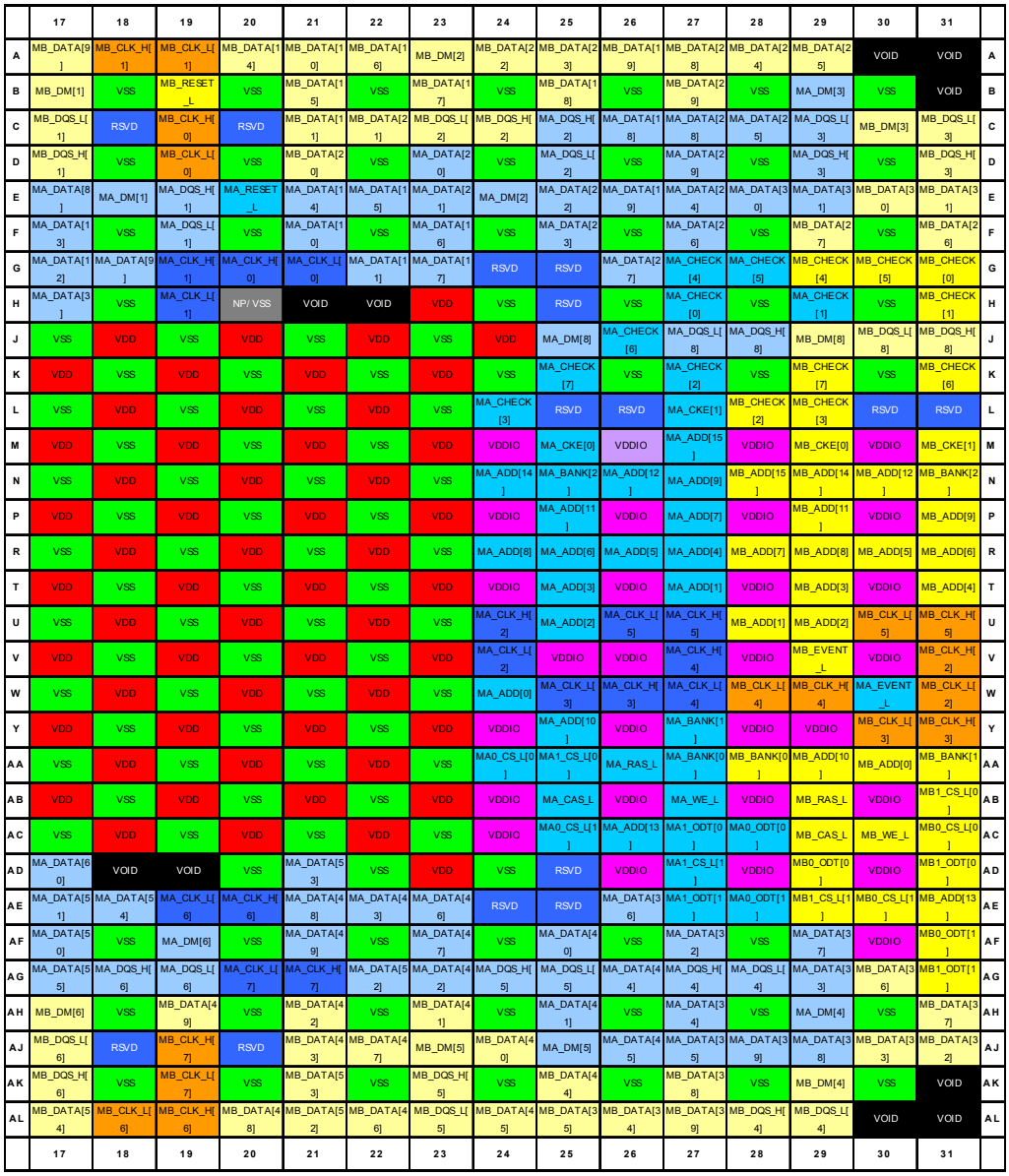
Name	Pin	Name	Pin	Name	Pin	Name	Pin
VSS	B14	VSS	H28	VSS	M18	VSS	T8
VSS	B16	VSS	H30	VSS	M20	VSS	U11
VSS	B18	VSS	H8	VSS	M22	VSS	U13
VSS	B20	VSS	J11	VSS	M8	VSS	U15
VSS	B22	VSS	J13	VSS	N11	VSS	U17
VSS	B24	VSS	J15	VSS	N13	VSS	U19
VSS	B26	VSS	J17	VSS	N15	VSS	U21
VSS	B28	VSS	J19	VSS	N17	VSS	U23
VSS	B30	VSS	J21	VSS	N19	VSS	U4
VSS	B4	VSS	J23	VSS	N21	VSS	U5
VSS	B9	VSS	J4	VSS	N23	VSS	U7
VSS	C3	VSS	J5	VSS	N4	VSS	U9
VSS	D14	VSS	J7	VSS	N5	VSS	V10
VSS	D16	VSS	J9	VSS	N7	VSS	V12
VSS	D18	VSS	K10	VSS	N9	VSS	V14
VSS	D20	VSS	K12	VSS	P10	VSS	V16
VSS	D22	VSS	K14	VSS	P12	VSS	V18
VSS	D24	VSS	K16	VSS	P14	VSS	V2
VSS	D26	VSS	K18	VSS	P16	VSS	V20
VSS	D28	VSS	K2	VSS	P18	VSS	V22
VSS	D30	VSS	K20	VSS	P2	VSS	V3
VSS	E11	VSS	K22	VSS	P20	VSS	W11
VSS	F14	VSS	K24	VSS	P22	VSS	W13
VSS	F16	VSS	K26	VSS	P3	VSS	W15
VSS	F18	VSS	K28	VSS	P8	VSS	W17
VSS	F20	VSS	K3	VSS	R11	VSS	W19
VSS	F22	VSS	K30	VSS	R13	VSS	W21
VSS	F24	VSS	K8	VSS	R15	VSS	W23
VSS	F26	VSS	L11	VSS	R17	VSS	W7
VSS	F28	VSS	L13	VSS	R19	VSS	W9
VSS	F30	VSS	L15	VSS	R21	VSS	Y10
VSS	F4	VSS	L17	VSS	R23	VSS	Y12
VSS	G11	VSS	L19	VSS	R7	VSS	Y14
VSS	G9	VSS	L21	VSS	R9	VSS	Y16
VSS	H10	VSS	L23	VSS	T10	VSS	Y18
VSS	H12	VSS	L7	VSS	T12	VSS	Y20
VSS	H14	VSS	L9	VSS	T14	VSS	Y22
VSS	H16	VSS	M10	VSS	T16	VSS	Y8
VSS	H18	VSS	M12	VSS	T18		
VSS	H24	VSS	M14	VSS	T20		
VSS	H26	VSS	M16	VSS	T22		

1.6 Color-Coded Connection Diagram (Left Half)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VOID	VOID	VSS	VDDNB	DBREQ_L	VDDNB	VSS	CLKIN_H	VSS	TEST25_H	VSS	VDDR	MB_DATA[11]	MB_DATA[6]	MB_DATA[2]	MB_DATA[8]	A
B	VOID	NP/ RSVD	VDD	VSS	VDDNB	DBRDY	VDDNB	CLKIN_L	VSS	TEST25_L	VSS	VDDR	MB_DM[0]	VSS	MB_DATA[7]	VSS	B
C	SVC/ VID[3]	VDD	VSS	VDD	TEST14	VDDNB	RESET_L	VDDNB	PWROK	VDDA	TEST29_H	VDDR	MB_DQS_L[0]	MB_DQS_H[0]	MB_DATA[3]	MB_DATA[13]	C
D	VID[4]	VID[5]	VDD	TEST8	VDD	TEST17	VDDNB	LDTSTOP_L	VDDNB	VDDA	TEST29_L	VDDR	MB_DATA[0]	VSS	MB_DATA[12]	VSS	D
E	VID[0]	PVIEN/ VID[1]	SVD/ VID[2]	VDD	TEST7	VDD	TEST16	VDDNB	TEST18	VDDNB	VSS	VDDR_SENSE	MB_DATA[5]	MA_DATA[1]	MA_DATA[6]	MA_DATA[2]	E
F	PSI_L	RSVD	M_VDDIO_PWRGD	VSS	VDD	TEST9	VDD	TEST15	VDDNB	TEST19	VDDNB	M_VREF	MB_DATA[4]	VSS	MA_DQS_H[0]	VSS	F
G	VDD_FB_L	VDD_FB_H	VDDNB_FB_L	VDDNB_FB_H	CORE_TYPE	VDD	TEST10	VDD	VSS	VDDNB	VSS	VDDNB	MA_DATA[5]	MA_DATA[0]	MA_DQS_L[0]	MA_DATA[7]	G
H	VLDT_B	VLDT_B	VOID	VOID	VLDT_B	VLDT_B	VDD	VSS	TEST28_L	VSS	VDD	VSS	MA_DATA[4]	VSS	MA_DM[0]	VSS	H
J	L0_CADIN_H[1]	L0_CADIN_L[0]	L0_CADIN_H[0]	VSS	VSS	L0_CADIN_H[8]	VSS	VDD	VSS	TEST28_H	VSS	VDD	VSS	VDD	VSS	VDD	J
K	L0_CADIN_L[1]	VSS	VSS	L0_CADIN_H[9]	L0_CADIN_L[9]	L0_CADIN_L[8]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	K
L	L0_CADIN_H[3]	L0_CADIN_L[2]	L0_CADIN_H[2]	VDD	VDD	L0_CADIN_H[10]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	L
M	L0_CADIN_L[3]	VDD	VDD	L0_CADIN_H[11]	L0_CADIN_L[11]	L0_CADIN_L[10]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	M
N	L0_CADIN_H[4]	L0_CLKIN_L[0]	L0_CLKIN_H[0]	VSS	VSS	L0_CLKIN_H[1]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	N
P	L0_CADIN_L[4]	VSS	VSS	L0_CADIN_H[12]	L0_CADIN_L[12]	L0_CLKIN_L[1]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	P
R	L0_CADIN_H[6]	L0_CADIN_L[5]	L0_CADIN_H[5]	VDD	VDD	L0_CADIN_H[13]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	R
T	L0_CADIN_L[6]	VDD	VDD	L0_CADIN_H[14]	L0_CADIN_L[14]	L0_CADIN_L[13]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	T
U	L0_CTLIN_H[0]	L0_CADIN_L[7]	L0_CADIN_H[7]	VSS	VSS	L0_CADIN_H[15]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	U
V	L0_CTLIN_L[0]	VSS	VSS	L0_CTLIN_H[1]	L0_CTLIN_L[1]	L0_CADIN_L[15]	HTREF0	HTREF1	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	V
W	L0_CADOUT_L[7]	L0_CTLOUT_H[0]	L0_CTLOUT_L[0]	VDD	VDD	L0_CTLOUT_L[1]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	W
Y	L0_CADOUT_H[7]	VDD	VDD	L0_CADOUT_L[15]	L0_CADOUT_H[15]	L0_CTLOUT_H[1]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	Y
AA	L0_CADOUT_L[5]	L0_CADOUT_H[6]	L0_CADOUT_L[6]	VSS	VSS	L0_CADOUT_L[14]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	AA
AB	L0_CADOUT_H[5]	VSS	VSS	L0_CADOUT_L[13]	L0_CADOUT_H[13]	L0_CADOUT_H[14]	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	AB
AC	L0_CLKOUT_L[0]	L0_CADOUT_H[4]	L0_CADOUT_L[4]	VDD	VDD	L0_CADOUT_L[12]	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	AC
AD	L0_CLKOUT_H[0]	VDD	VDD	L0_CLKOUT_L[1]	L0_CLKOUT_H[1]	L0_CADOUT_H[12]	VDD	VSS	VDD	VSS	VDD	VSS	MA_DATA[59]	VSS	MA_DQS_H[7]	VSS	AD
AE	L0_CADOUT_L[2]	L0_CADOUT_H[3]	L0_CADOUT_L[3]	VSS	VSS	L0_CADOUT_L[11]	NP/ VSS	VOID	VOID	VDD	VSS	VDD	MA_DATA[58]	MA_DATA[63]	MA_DQS_L[7]	MA_DATA[56]	AE
AF	L0_CADOUT_H[2]	VSS	VSS	L0_CADOUT_L[10]	L0_CADOUT_H[10]	L0_CADOUT_H[11]	VDD	VSS	VDD	VSS	VDD	VSS	MB_DATA[59]	VSS	MA_DM[7]	VSS	AF
AG	L0_CADOUT_L[0]	L0_CADOUT_H[1]	L0_CADOUT_L[1]	VDD	VDD	L0_CADOUT_L[9]	VDD	THERMDA	THERMDC	VSS	VSS	VDDR	MB_DATA[58]	MA_DATA[62]	MA_DATA[57]	MA_DATA[61]	AG
AH	L0_CADOUT_H[0]	VDD	VDD	L0_CADOUT_L[8]	L0_CADOUT_H[8]	L0_CADOUT_H[9]	TEST3	TEST23	TEST12	TCK	M_ZN	VDDR	MB_DATA[63]	VSS	MB_DATA[51]	VSS	AH
AJ	VLDT_A	VLDT_A	VLDT_A	VLDT_A	TEST6	TEST2	TEST13	TEST20	TEST22	TRST_L	M_ZP	VDDR	MB_DQS_L[7]	MB_DM[7]	MB_DATA[60]	MB_DATA[50]	AJ
AK	VOID	VSS	RSVD	SA[0]	TEST26	SID	THERMTRIP_L	TEST24	TEST27	TDO	VDDIO_FB_H	VDDR	MB_DQS_H[7]	VSS	MB_DATA[56]	VSS	AK
AL	VOID	VOID	CPU_PRESENT_L	ALERT_L	VSS	SIC	PROCHOT_L	TEST21	TMS	TDI	VDDIO_FB_L	VDDR	MB_DATA[62]	MB_DATA[57]	MB_DATA[61]	MB_DATA[55]	AL
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. Color-Coded Connection Diagram (Left Half)

1.7 Color-Coded Connection Diagram (Right Half)



	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
A	MB_DATA[9]	MB_CLK_H[1]	MB_CLK_L[1]	MB_DATA[14]	MB_DATA[10]	MB_DATA[16]	MB_DM[2]	MB_DATA[22]	MB_DATA[23]	MB_DATA[19]	MB_DATA[28]	MB_DATA[24]	MB_DATA[25]	VOID	VOID	A
B	MB_DM[1]	VSS	MB_RESET_L	VSS	MB_DATA[15]	VSS	MB_DATA[17]	VSS	MB_DATA[18]	VSS	MB_DATA[29]	VSS	MA_DM[3]	VSS	VOID	B
C	MB_DQS_L[1]	RSVD	MB_CLK_H[0]	RSVD	MB_DATA[11]	MB_DATA[21]	MB_DQS_L[2]	MB_DQS_H[2]	MA_DQS_H[2]	MA_DATA[18]	MA_DATA[28]	MA_DATA[25]	MA_DQS_L[3]	MB_DM[3]	MB_DQS_L[3]	C
D	MB_DQS_H[1]	VSS	MB_CLK_L[0]	VSS	MB_DATA[20]	VSS	MA_DATA[20]	VSS	MA_DQS_L[2]	VSS	MA_DATA[29]	VSS	MA_DQS_H[3]	VSS	MB_DQS_H[3]	D
E	MA_DATA[8]	MA_DM[1]	MA_DQS_H[1]	MA_RESET_L	MA_DATA[14]	MA_DATA[15]	MA_DATA[21]	MA_DM[2]	MA_DATA[22]	MA_DATA[19]	MA_DATA[24]	MA_DATA[30]	MA_DATA[31]	MB_DATA[30]	MB_DATA[31]	E
F	MA_DATA[13]	VSS	MA_DQS_L[1]	VSS	MA_DATA[10]	VSS	MA_DATA[16]	VSS	MA_DATA[23]	VSS	MA_DATA[26]	VSS	MB_DATA[27]	VSS	MB_DATA[26]	F
G	MA_DATA[12]	MA_DATA[9]	MA_CLK_H[1]	MA_CLK_H[0]	MA_CLK_L[0]	MA_DATA[11]	MA_DATA[17]	RSVD	RSVD	MA_DATA[27]	MA_CHECK[4]	MA_CHECK[5]	MB_CHECK[4]	MB_CHECK[5]	MB_CHECK[0]	G
H	MA_DATA[3]	VSS	MA_CLK_L[1]	NP/ VSS	VOID	VOID	VDD	VSS	RSVD	VSS	MA_CHECK[0]	VSS	MA_CHECK[1]	VSS	MB_CHECK[1]	H
J	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	MA_DM[8]	MA_CHECK[6]	MA_DQS_L[8]	MA_DQS_H[8]	MB_DM[8]	MB_DQS_L[8]	MB_DQS_H[8]	J
K	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CHECK[7]	VSS	MA_CHECK[2]	VSS	MB_CHECK[7]	VSS	MB_CHECK[6]	K
L	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CHECK[3]	RSVD	RSVD	MA_CKE[1]	MB_CHECK[2]	MB_CHECK[3]	RSVD	RSVD	L
M	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_CKE[0]	VDDIO	MA_ADD[15]	VDDIO	MB_CKE[0]	VDDIO	MB_CKE[1]	M
N	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[14]	MA_BANK[2]	MA_ADD[12]	MA_ADD[9]	MB_ADD[15]	MB_ADD[14]	MB_ADD[12]	MB_BANK[2]	N
P	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[11]	VDDIO	MA_ADD[7]	VDDIO	MB_ADD[11]	VDDIO	MB_ADD[9]	P
R	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[8]	MA_ADD[6]	MA_ADD[5]	MA_ADD[4]	MB_ADD[7]	MB_ADD[8]	MB_ADD[5]	MB_ADD[6]	R
T	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[3]	VDDIO	MA_ADD[1]	VDDIO	MB_ADD[3]	VDDIO	MB_ADD[4]	T
U	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_CLK_H[2]	MA_ADD[2]	MA_CLK_L[5]	MA_CLK_H[5]	MB_ADD[1]	MB_ADD[2]	MB_CLK_L[5]	MB_CLK_H[5]	U
V	VDD	VSS	VDD	VSS	VDD	VSS	VDD	MA_CLK_L[2]	VDDIO	VDDIO	MA_CLK_H[4]	VDDIO	MB_EVENT_L	VDDIO	MB_CLK_H[2]	V
W	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA_ADD[0]	MA_CLK_L[3]	MA_CLK_H[3]	MA_CLK_L[4]	MB_CLK_L[4]	MB_CLK_H[4]	MA_EVENT_L	MB_CLK_L[2]	W
Y	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_ADD[10]	VDDIO	MA_BANK[1]	VDDIO	VDDIO	MB_CLK_L[3]	MB_CLK_H[3]	Y
AA	VSS	VDD	VSS	VDD	VSS	VDD	VSS	MA0_CS_L[0]	MA1_CS_L[0]	MA_RAS_L	MA_BANK[0]	MB_BANK[0]	MB_ADD[10]	MB_ADD[0]	MB_BANK[1]	AA
AB	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VDDIO	MA_CAS_L	VDDIO	MA_WE_L	VDDIO	MB_RAS_L	VDDIO	MB1_CS_L[0]	AB
AC	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDDIO	MA0_CS_L[1]	MA_ADD[13]	MA1_ODT[0]	MA0_ODT[0]	MB_CAS_L	MB_WE_L	MB0_CS_L[0]	AC
AD	MA_DATA[60]	VOID	VOID	VSS	MA_DATA[53]	VSS	VDD	VSS	RSVD	VDDIO	MA1_CS_L[1]	VDDIO	MB0_ODT[0]	VDDIO	MB1_ODT[0]	AD
AE	MA_DATA[51]	MA_DATA[54]	MA_CLK_L[6]	MA_CLK_H[6]	MA_DATA[48]	MA_DATA[43]	MA_DATA[46]	RSVD	RSVD	MA_DATA[36]	MA1_ODT[1]	MA0_ODT[1]	MB1_CS_L[1]	MB0_CS_L[1]	MB_ADD[13]	AE
AF	MA_DATA[50]	VSS	MA_DM[6]	VSS	MA_DATA[49]	VSS	MA_DATA[47]	VSS	MA_DATA[40]	VSS	MA_DATA[32]	VSS	MA_DATA[37]	VDDIO	MB0_ODT[1]	AF
AG	MA_DATA[55]	MA_DQS_H[6]	MA_DQS_L[6]	MA_CLK_L[7]	MA_CLK_H[7]	MA_DATA[52]	MA_DATA[42]	MA_DQS_H[5]	MA_DQS_L[5]	MA_DATA[44]	MA_DQS_H[4]	MA_DQS_L[4]	MA_DATA[33]	MB_DATA[36]	MB1_ODT[1]	AG
AH	MB_DM[6]	VSS	MB_DATA[49]	VSS	MB_DATA[42]	VSS	MB_DATA[41]	VSS	MA_DATA[41]	VSS	MA_DATA[34]	VSS	MA_DM[4]	VSS	MB_DATA[37]	AH
AJ	MB_DQS_L[6]	RSVD	MB_CLK_H[7]	RSVD	MB_DATA[43]	MB_DATA[47]	MB_DM[5]	MB_DATA[40]	MA_DM[5]	MA_DATA[45]	MA_DATA[35]	MA_DATA[39]	MA_DATA[38]	MB_DATA[33]	MB_DATA[32]	AJ
AK	MB_DQS_H[6]	VSS	MB_CLK_L[7]	VSS	MB_DATA[53]	VSS	MB_DQS_H[5]	VSS	MB_DATA[44]	VSS	MB_DATA[38]	VSS	MB_DM[4]	VSS	VOID	AK
AL	MB_DATA[54]	MB_CLK_L[6]	MB_CLK_H[6]	MB_DATA[48]	MB_DATA[52]	MB_DATA[46]	MB_DQS_L[5]	MB_DATA[45]	MB_DATA[35]	MB_DATA[34]	MB_DATA[39]	MB_DQS_H[4]	MB_DQS_L[4]	VOID	VOID	AL
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Figure 4. Color-Coded Connection Diagram (Right Half)

2 Package Specifications

2.1 Mechanical Loading for Lidded Parts

Table 10 provides the mechanical loading specification for lidded parts. These specifications should not be exceeded during heat sink installation, system testing, or system shipment.

Table 10. Mechanical Loading for Lidded Parts

Type	Units	Maximum Force	Notes
Static	lbf	100	1, 2
Dynamic	lbf	200	1, 3

Notes:
1. *Load specified for coplanar, uniform contact to lid surface.*
2. *The static specification specifies the allowable range to be applied by the heat sink to the processor package.*
3. *The dynamic specification assumes a dynamic load that includes the static load and is applied at 50 G for 11 ms.*

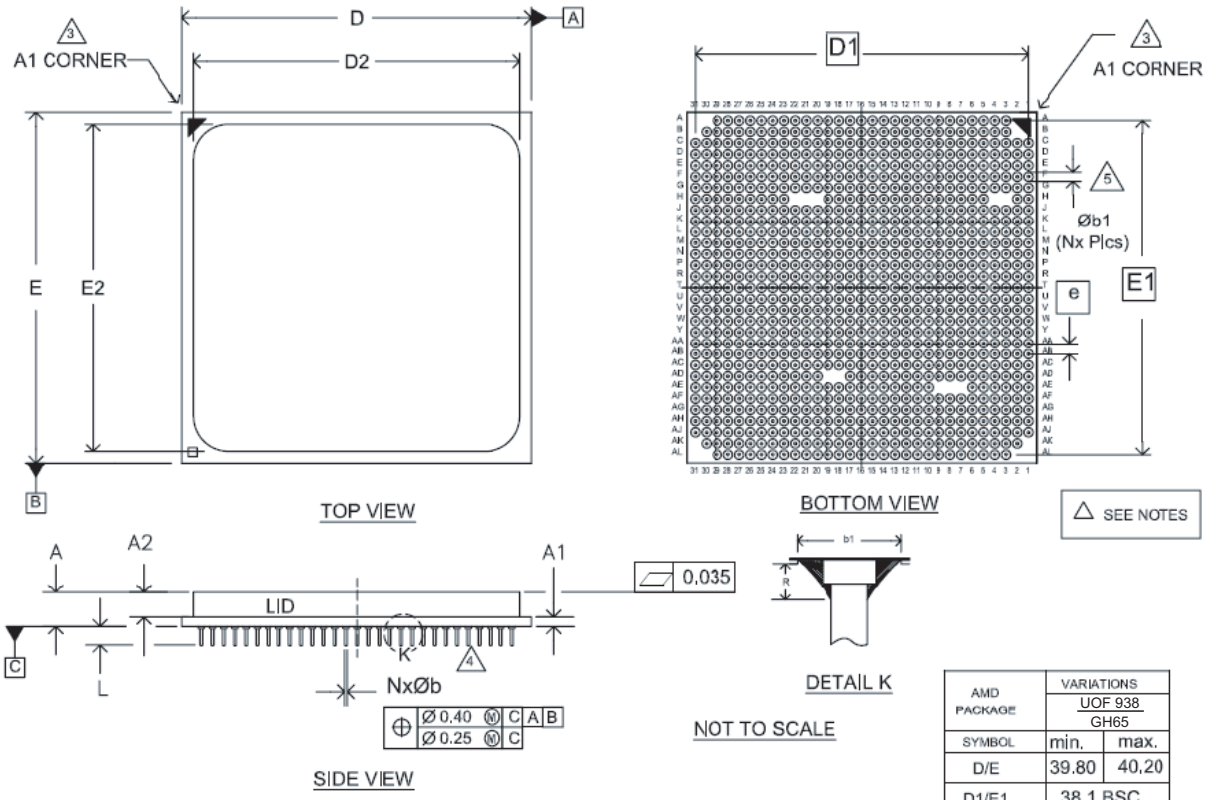
2.2 Package Insertions

Table 11 provides the recommended number of times that the processor package can be inserted and removed from a socket.

Table 11. Recommended Number of Insertions

Package	Number of Insertions
AM3	15

2.3 Package Diagram



AMD PACKAGE	VARIATIONS UOF 938 GH65	
SYMBOL	min.	max.
D/E	39.80	40.20
D1/E1	38.1 BSC	
D2/E2	37.4	37.6
A	4.17	4.81
A1	1.12	1.46
A2	3.05	3.35
e	1.27 BSC	
b	0.275	0.325
b1	0.98	1.08
L	1.95	2.11
M	31	
N	938	
R	0.30 MAX	
WT (gms)	39.275 REF	

GENERAL NOTES

1. **All dimensions are specified in millimeters (mm).**
2. **Dimensioning and tolerancing per ASME-Y14.5M-1994.**
3. **The A1 corner consists of a triangle on both sides of the package that identifies the pin A1 corner and can be used for handling and orientation purposes.**
4. **Pin tips should have radius 0.13.**
5. **Symbol “M” determines pin matrix size and “N” is number of pins.**

Figure 5. Organic Micro Pin Grid Array Package(UOF): Top, Side, and Bottom Views (Lidded)