# TS7KRN30800-6S

## 240Pin DDR3 1600 VLP RDIMM 4GB
## Based on 256Mx8

### Description

DDR3 VLP Registered DIMM is high-speed, low power memory module that use 256Mx8bits DDR3 SDRAM in FBGA package, 1 pcs register in TFBGA package and a 2048 bits serial EEPROM on a 240-pin printed circuit board. DDR3 VLP Registered DIMM is a Dual In-Line Memory Module and is intended for mounting into 240-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

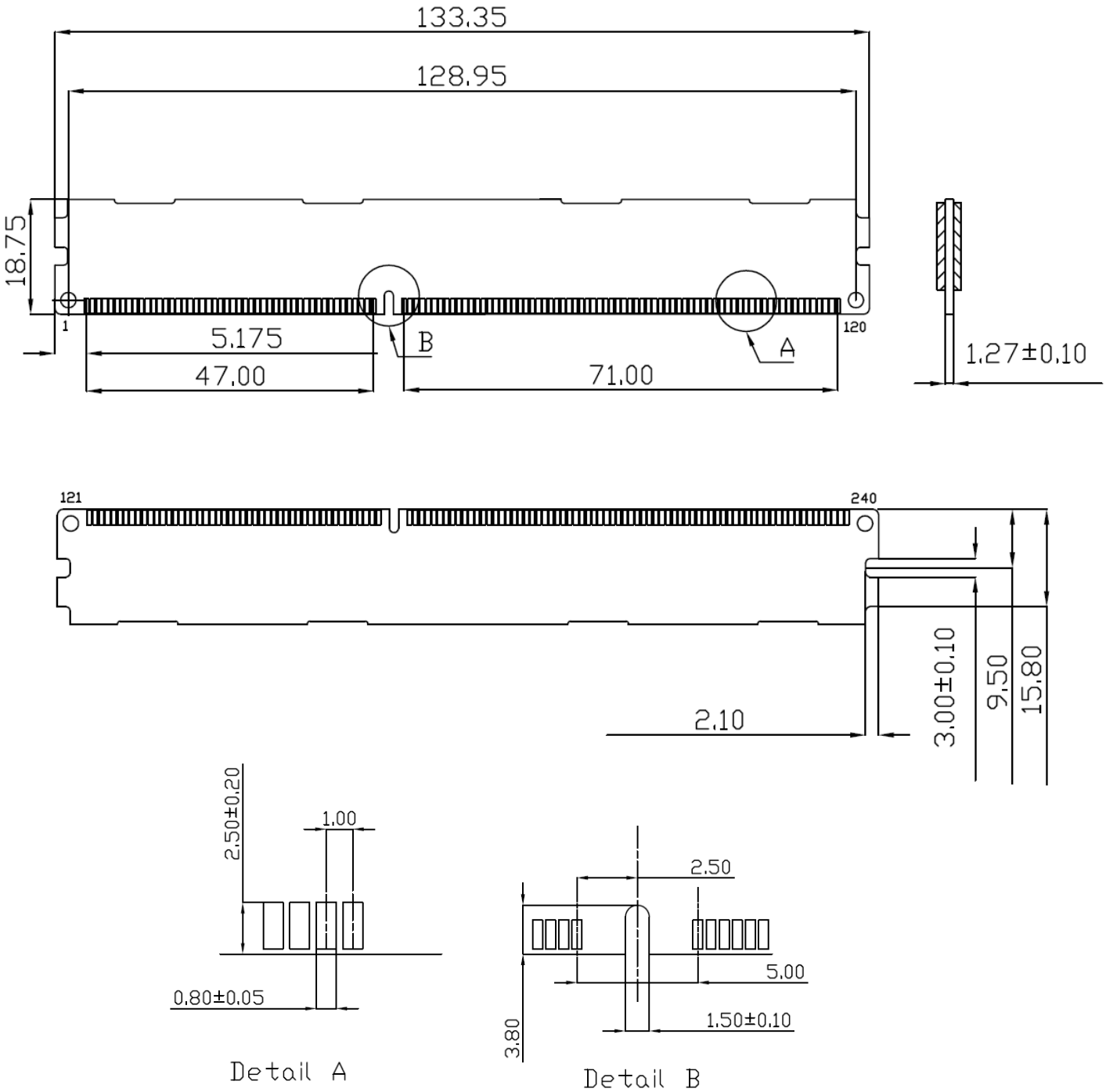
### Features

- RoHS compliant products.
- JEDEC standard 1.5V ± 0.075V Power supply
- VDDQ=1.5V ± 0.075V
- Clock Freq: 667MHZ for 1333Mb/s/Pin.
- Clock Freq: 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9 ,10 ,11
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 7 (DDR3-1333) , 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- On DIMM thermal Sensor

### Pin Identification

| Symbol | Function |
|---|---|
| A0~A14, BA0~BA2 | Address Inputs |
| /RAS | Row Address Strobe |
| /CAS | Column Address Strobe |
| /WE | Write Enable |
| /S0, /S1 | Chip Selects |
| CKE0, CKE1 | Clock Enables |
| ODT0, ODT1 | On-die termination control |
| DQ0~DQ63 | Data Input/Output |
| CB0~CB7 | ECC Check bits |
| DQS0~DQS8<br>/DQS0~/DQS8 | Data Strobe |
| DM0~DM8 | Data Masks |
| CK0, /CK0 | Clocks Input |
| /RESET | Reset Pin |
| /EVENT | Temperature Event Pin |
| /ERROUT | Parity error found on address and control bus |
| Par-In | Parity bit for address and Control bus |
| VDD | Core and I/O Power |
| VSS | Ground |
| VREFDQ, VREFCA | Input/Output Reference |
| VTT | Termination Voltage |
| VDDSPD | SPD Power |
| SCL | SPD Clock Input |
| SDA | SPD Data |
| SA0~SA2 | SPD Address |

### Dimensions (Unit: millimeter)



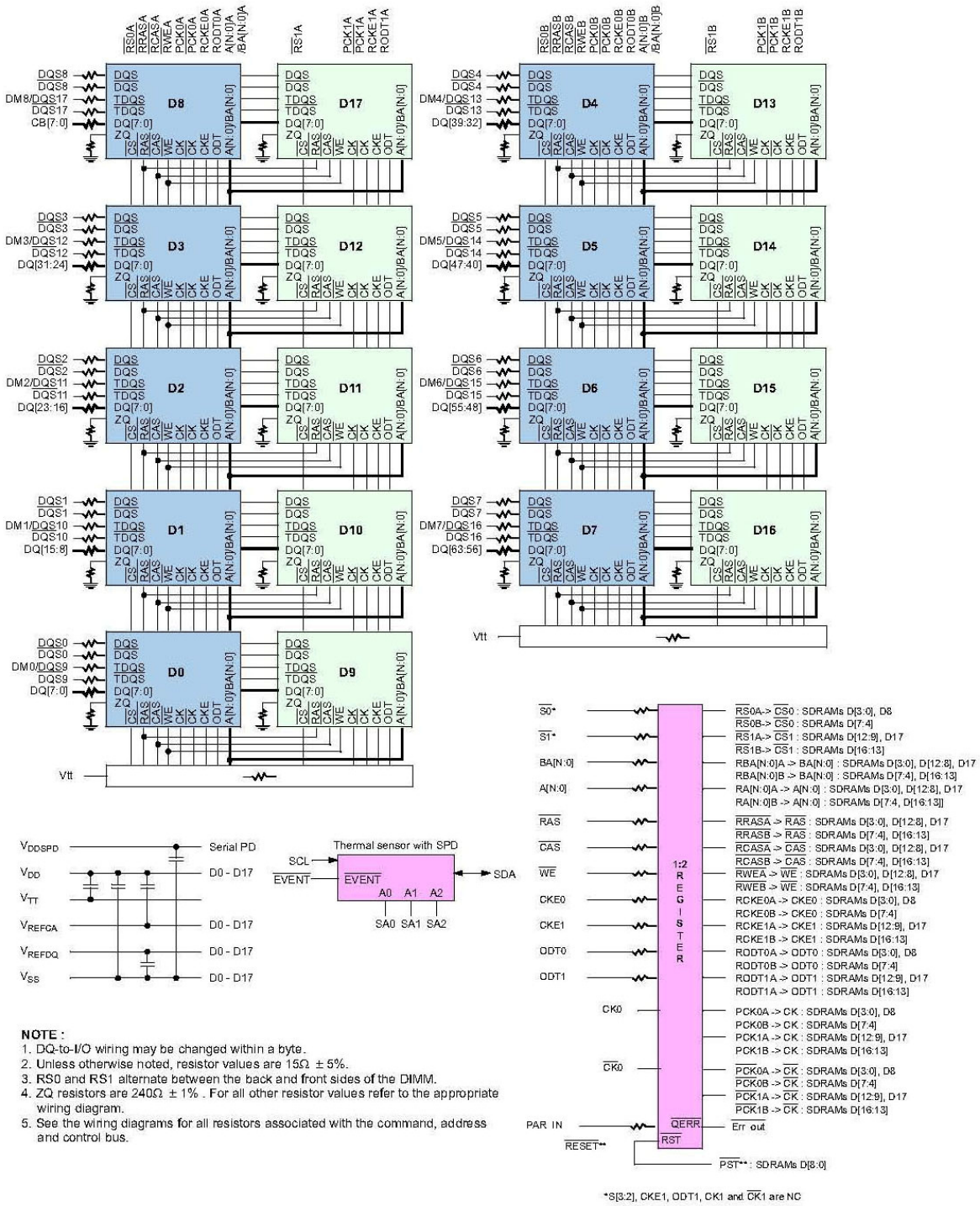

Note:
1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

## Pin Assignments

| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01 | VREFDQ | 41 | VSS | 81 | DQ32 | 121 | VSS | 161 | TDQS17 | 201 | DQ37 |
| 02 | VSS | 42 | /DQS8 | 82 | DQ33 | 122 | DQ4 | 162 | /TDQS17 | 202 | VSS |
| 03 | DQ0 | 43 | DQS8 | 83 | VSS | 123 | DQ5 | 163 | VSS | 203 | TDQS13 |
| 04 | DQ1 | 44 | VSS | 84 | /DQS4 | 124 | VSS | 164 | CB6 | 204 | /TDQS13 |
| 05 | VSS | 45 | CB2 | 85 | DQS4 | 125 | TDQS9 | 165 | CB7 | 205 | VSS |
| 06 | /DQS0 | 46 | CB3 | 86 | VSS | 126 | /TDQS9 | 166 | VSS | 206 | DQ38 |
| 07 | DQS0 | 47 | VSS | 87 | DQ34 | 127 | VSS | 167 | NC | 207 | DQ39 |
| 08 | VSS | 48 | VTT | 88 | DQ35 | 128 | DQ6 | 168 | /RESET | 208 | VSS |
| 09 | DQ2 | 49 | VTT | 89 | VSS | 129 | DQ7 | 169 | CKE1,NC | 209 | DQ44 |
| 10 | DQ3 | 50 | CKE0 | 90 | DQ40 | 130 | VSS | 170 | VDD | 210 | DQ45 |
| 11 | VSS | 51 | VDD | 91 | DQ41 | 131 | DQ12 | 171 | NC | 211 | VSS |
| 12 | DQ8 | 52 | BA2 | 92 | VSS | 132 | DQ13 | 172 | A14 | 212 | TDQS14 |
| 13 | DQ9 | 53 | /Err_Out | 93 | /DQS5 | 133 | VSS | 173 | VDD | 213 | /TQS14 |
| 14 | VSS | 54 | VDD | 94 | DQS5 | 134 | TDQS10 | 174 | A12 | 214 | VSS |
| 15 | /DQS1 | 55 | A11 | 95 | VSS | 135 | /TDQS10 | 175 | A9 | 215 | DQ46 |
| 16 | DQS1 | 56 | A7 | 96 | DQ42 | 136 | VSS | 176 | VDD | 216 | DQ47 |
| 17 | VSS | 57 | VDD | 97 | DQ43 | 137 | DQ14 | 177 | A8 | 217 | VSS |
| 18 | DQ10 | 58 | A5 | 98 | VSS | 138 | DQ15 | 178 | A6 | 218 | DQ52 |
| 19 | DQ11 | 59 | A4 | 99 | DQ48 | 139 | VSS | 179 | VDD | 219 | DQ53 |
| 20 | VSS | 60 | VDD | 100 | DQ49 | 140 | DQ20 | 180 | A3 | 220 | VSS |
| 21 | DQ16 | 61 | A2 | 101 | VSS | 141 | DQ21 | 181 | A1 | 221 | TDQS15 |
| 22 | DQ17 | 62 | VDD | 102 | /DQS6 | 142 | VSS | 182 | VDD | 222 | /TDQS15 |
| 23 | VSS | 63 | NC | 103 | DQS6 | 143 | TDQS11 | 183 | VDD | 223 | VSS |
| 24 | /DQS2 | 64 | NC | 104 | VSS | 144 | /TDQS11 | 184 | CK0 | 224 | DQ54 |
| 25 | DQS2 | 65 | VDD | 105 | DQ50 | 145 | VSS | 185 | /CK0 | 225 | DQ55 |
| 26 | VSS | 66 | VDD | 106 | DQ51 | 146 | DQ22 | 186 | VDD | 226 | VSS |
| 27 | DQ18 | 67 | VREFCA | 107 | VSS | 147 | DQ23 | 187 | /EVENT | 227 | DQ60 |
| 28 | DQ19 | 68 | Par-In | 108 | DQ56 | 148 | VSS | 188 | A0 | 228 | DQ61 |
| 29 | VSS | 69 | VDD | 109 | DQ57 | 149 | DQ28 | 189 | VDD | 229 | VSS |
| 30 | DQ24 | 70 | A10/AP | 110 | VSS | 150 | DQ29 | 190 | BA1 | 230 | TDQS16 |
| 31 | DQ25 | 71 | BA0 | 111 | /DQS7 | 151 | VSS | 191 | VDD | 231 | /TDQS16 |
| 32 | VSS | 72 | VDD | 112 | DQS7 | 152 | TDQS12 | 192 | /RAS | 232 | VSS |
| 33 | /DQS3 | 73 | /WE | 113 | VSS | 153 | /TDQS12 | 193 | /S0 | 233 | DQ62 |
| 34 | DQS3 | 74 | /CAS | 114 | DQ58 | 154 | VSS | 194 | VDD | 234 | DQ63 |
| 35 | VSS | 75 | VDD | 115 | DQ59 | 155 | DQ30 | 195 | ODT0 | 235 | VSS |
| 36 | DQ26 | 76 | /S1 | 116 | VSS | 156 | DQ31 | 196 | A13 | 236 | VDDSPD |
| 37 | DQ27 | 77 | ODT1,NC | 117 | SA0 | 157 | VSS | 197 | VDD | 237 | SA1 |
| 38 | VSS | 78 | VDD | 118 | SCL | 158 | CB4 | 198 | /S3,NC | 238 | SDA |
| 39 | CB0 | 79 | /S2,NC | 119 | SA2 | 159 | CB5 | 199 | VSS | 239 | VSS |
| 40 | CB1 | 80 | VSS | 120 | VTT | 160 | VSS | 200 | DQ36 | 240 | VTT |

ODT1, CKE1：Connected to the register on 2 and 4 rank RDIMM ; NC on 1 rank RDIMM
/S2, /S3：Connected to the register on 4 rank RDIMM ; NC on 1 or 2 rank RDIMM

## Block Diagram
## 4GB, 512Mx72 Module(2 Rank x8)




**NOTE :**
1. DQ-to-I/O wiring may be changed within a byte.
2. Unless otherwise noted, resistor values are 15Ω ± 5%.
3. RS0 and RS1 alternate between the back and front sides of the DIMM.
4. ZQ resistors are 240Ω ± 1% . For all other resistor values refer to the appropriate wiring diagram.
5. See the wiring diagrams for all resistors associated with the command, address and control bus.

## Operating Temperature Condition

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Operating Temperature | TOPER | 0 to 85 | °C | 1,2 |

Note:
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

## Absolute Maximum DC Ratings

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Voltage on $V_{DD}$ relative to Vss | VDD | -0.4 ~ 1.975 | V | 1 |
| Voltage on $V_{DDQ}$ pin relative to Vss | VDDQ | -0.4 ~ 1.975 | V | 1 |
| Voltage on any pin relative to Vss | VIN, VOUT | -0.4 ~ 1.975 | V | 1 |
| Storage temperature | $T_{STG}$ | -55~+100 | °C | 1,2 |

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

## AC & DC Operating Conditions

**Recommended DC operating conditions (SSTL –1.5)**

| Parameter | Symbol | Rating | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min | Typ. | Max | | |
| Supply voltage | VDD | 1.425 | 1.5 | 1.575 | V | 1, 2 |
| Supply voltage for Output | VDDQ | 1.425 | 1.5 | 1.575 | V | 1, 2 |
| I/O Reference Voltage (DQ) | $VREF_{DQ}$(DC) | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | V | 3 |
| I/O Reference Voltage (CMD/ADD) | $VREF_{CA}$(DC) | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | V | 3 |
| AC Input Logic High | $V_{IH(AC)}$ | VREF+0.175 | - | - | V | |
| AC Input Logic Low | $V_{IL(AC)}$ | - | - | VREF-0.175 | V | |
| DC Input Logic High | $V_{IH(DC)}$ | $V_{REF}$+0.1 | - | VDD | V | |
| DC Input Logic Low | $V_{IL(DC)}$ | VSS | - | $V_{REF}$-0.1 | V | |

Note: There is no specific device VDD supply voltage requirement for SSTL-1.5 compliance.
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

## AC Input Level for Differential Signals

| Parameter | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| Differential Input Logical High | $V_{IHdiff}$ | +200 | - | mV | |
| Differential Input Logical Low | $V_{ILdiff}$ | - | -200 | | |

## IDD Specification parameters Definition

**( IDD values are for full operating range of Voltage and Temperature)**

### 4GB, 512Mx72 Module(2 Rank x8)

| Parameter | Symbol | DDR3 1600 CL11 | Unit |
|---|---|---|---|
| **Operating One bank Active-Precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD0 | 1305 | mA |
| **Operating One bank Active-read-Precharge current;** IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD1 | 1395 | mA |
| **Precharge power-down current**; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2P | 900 | mA |
| **Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2Q | 1030 | mA |
| **Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD2N | 1050 | mA |
| **Active power - down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD3P | 990 | mA |
| **Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD3N | 1310 | mA |
| **Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD4R | 1710 | mA |
| **Operating burst write current;** All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R | IDD4W | 1765 | mA |
| **Burst refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD5 | 1940 | mA |
| **Self refresh current;** CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | IDD6 | 246 | mA |
| **Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; | IDD7 | 2160 | mA |

Note:

## Timing Parameters & Specifications

| Speed | | DDR3 1600 | | Unit |
|---|---|---|---|---|
| Parameter | Symbol | Min | Max | |
| Average Clock Period | tCK | 1.25 | <1.5 | ns |
| CK high-level width | tCH | 0.47 | 0.53 | tCK |
| CK low-level width | tCL | 0.47 | 0.53 | tCK |
| DQS, /DQS to DQ skew, per group, per access | tDQSQ | - | 100 | ps |
| DQ output hold time from DQS, /DQS | tQH | 0.38 | - | tCK |
| DQ low-impedance time from CK, /CK | tLZ(DQ) | -450 | 225 | ps |
| DQ high-impedance time from CK, /CK | tHZ(DQ) | - | 225 | ps |
| Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels | tDS | 10 | - | ps |
| Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels | tDH | 45 | | ps |
| DQ and DM input pulse width for each input | tDIPW | 360 | - | ps |
| DQS, /DQS Read preamble | tRPRE | 0.9 | - | tCK |
| DQS, /DQS differential Read postamble | tRPST | 0.3 | - | tCK |
| DQS, /DQS Write preamble | tWPRE | 0.9 | - | tCK |
| DQS, /DQS Write postamble | tWPST | 0.3 | - | tCK |
| DQS, /DQS low-impedance time | tLZ(DQS) | -450 | 225 | ps |
| DQS, /DQS high-impedance time | tHZ(DQS) | - | 225 | ps |
| DQS, /DQS differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK |
| DQS, /DQS differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK |
| DQS, /DQS rising edge to CK, /CK rising edge | tDQSS | -0.27 | +0.27 | tCK |
| DQS, /DQS falling edge setup time to CK, /CK rising edge | tDSS | 0.18 | - | tCK |
| DQS, /DQS falling edge hold time to CK, /CK rising edge | tDSH | 0.18 | - | tCK |
| Delay from start of Internal write transaction to Internal read command | tWTR | Max (4tck, 7.5ns) | - | |
| Write recovery time | tWR | 15 | - | ns |
| Mode register set command cycle time | tMRD | 4 | - | tCK |
| /CAS to /CAS command delay | tCCD | 4 | - | nCK |
| Auto precharge write recovery + precharge time | tDAL | tWR+tRP/tck | | nCK |
| Active to active command period for 1KB page size | tRRD | Max (4tck, 6ns) | - | ns |

| Speed | | DDR3 1600 | | Unit |
|---|---|---|---|---|
| Parameter | Symbol | Min | Max | |
| Active to active command period for 2KB page size | tRRD | Max (4tck, 7.5ns) | - | |
| Four Activate Window for 1KB page size | tFAW | 30 | - | ns |
| Four Activate Window for 2KB page size products | tFAW | 40 | - | ns |
| Power-up and RESET calibration time | tZQinitl | 512 | - | tCK |
| Normal operation Full calibration time | tZQoper | 256 | - | tCK |
| Normal operation short calibration time | tZQcs | 64 | - | tCK |
| Exit self refresh to commands not requiring a locked DLL | tXS | Max (5tCK, tRFC+10ns) | - | |
| Exit self refresh to commands requiring a locked DLL | tXSDLL | tDLL(min) | - | tCK |
| Internal read to precharge command delay | tRTP | Max (4tck, 7.5ns) | - | |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCK(min)+1tCK | - | |
| Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL | tXP | Max (3tCK, 6ns) | - | |
| CKE minimum pulse width (high and low pulse width) | tCKE | Max (3tCK, 5ns) | | |
| Asynchronous RTT turn-on delay (Power-Down mode) | tAONPD | 2 | 8.5 | ns |
| Asynchronous RTT turn-off delay (Power-Down mode) | tAOFPD | 2 | 8.5 | ns |
| ODT turn-on | tAON | -225 | 225 | ps |
| ODT turn-off | tAOF | 0.3 | 0.7 | tCK |

## SERIAL PRESENCE DETECT SPECIFICATION

| TS512MKR72V6NL Serial Presence Detect | | | |
|---|---|---|---|
| **Byte No.** | **Function Described** | **Standard Specification** | **Vendor Part** |
| 0 | Number of SPD Bytes written / SPD device size / CRC coverage during module production | CRC:0-116Byte<br>SPD Byte use: 176Byte<br>SPD Byte total: 256Byte | 92 |
| 1 | SPD Revision | Version 1.0 | 10 |
| 2 | Key Byte / DRAM Device Type | DDR3 SDRAM | 0B |
| 3 | Key Byte / Module Type | RDIMM | 01 |
| 4 | SDRAM Density and Banks | 2Gb, 8banks | 03 |
| 5 | SDRAM Addressing | ROW:15, Column:10 | 19 |
| 6 | Reserved | - | 00 |
| 7 | Module Organization | 2Rank / x8 | 09 |
| 8 | Module Memory Bus Width | ECC, 72bit | 0B |
| 9 | Fine Timebase Dividend and Divisor | 2.5ps | 52 |
| 10 | Medium Timebase Dividend | 0.125ns | 01 |
| 11 | Medium Timebase Divisor | 0.125ns | 08 |
| 12 | SDRAM Minimum Cycle Time (tCKmin) | 1.25ns | 0A |
| 13 | Reserved | - | 00 |
| 14 | CAS Latencies Supported, Least Significant Byte | 6, 7, 8, 9, 10, 11 | FC |
| 15 | CAS Latencies Supported, Most Significant Byte | - | 00 |
| 16 | Minimum CAS Latency Time (tAAmin) | 13.125ns | 69 |
| 17 | Minimum Write Recovery Time (tWRmin) | 15ns | 78 |
| 18 | Minimum /RAS to /CAS Delay Time (tRCDmin) | 13.125ns | 69 |
| 19 | Minimum Row Active to Row Active Delay Time (tRRDmin) | 6ns | 30 |
| 20 | Minimum Row Precharge Time (tRPmin) | 13.125ns | 69 |
| 21 | Upper Nibble for tRAS and tRC | - | 11 |
| 22 | Minmum Active to Precharge Time (tRASmin) | 35ns | 18 |
| 23 | Minmum Active to Active/Refresh Time (tRCmin) | 48.125ns | 81 |
| 24 | Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte | 160ns | 00 |
| 25 | Minmum Refresh Recovery Time (tRASmin), Most Significant Byte | 160ns | 05 |
| 26 | Minmum Internal Write to Read Command Delay Time (tWTmin) | 7.5ns | 3C |
| 27 | Minimum Internal Read to Precharge Command Delay Time (tRTPmin) | 7.5ns | 3C |
| 28 | Upper Nibble for tFAW | 30ns | 00 |
| 29 | Minmum Four Active Window Delay Time (tFAWmin) | 30ns | F0 |
| 30 | SDRAM Optional Features | DLL off Mode,<br>RZQ/6, RZQ/7 | 83 |
| 31 | SDRAM Thermal and Refresh Options | No ODT, No ASR | 01 |
| 32 | DDR3-MODULE THERMAL SENSOR | Support TS | 80 |
| 33 | DDR3-SDRAM DEVICE TYPE | Mono | 00 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 34-59 | Reserved | - | 00 | | | | | |
| 60 | Module Nominal Height | 18.75mm | 04 | | | | | |
| 61 | Module Max Thickness | 1~2mm | 11 | | | | | |
| 62 | Reference Raw Card Used | Rev. 0.0, R/C L | 0A | | | | | |
| 63 | DIMM Module Attributes | 1 Row of DRAM, 1Register used | 05 | | | | | |
| 64 | DDR3-HEATSPREADER SOLUTION | Without HS | 00 | | | | | |
| 65 | Register Manufacturer ID Code, Least Significant Byte | Inphi | 04 | | | | | |
| | | IDT | 80 | | | | | |
| | | TI | 80 | | | | | |
| 66 | Register Manufacturer ID Code, Most Significant Byte | Inphi | B3 | | | | | |
| | | IDT | B3 | | | | | |
| | | TI | 97 | | | | | |
| 67 | Register Revision Number | Inphi GS-02 | 11 | | | | | |
| | | IDT B | 61 | | | | | |
| | | TI v4.2 | 28 | | | | | |
| 68 | Register Type | SSTE32882 | 00 | | | | | |
| 69 | Register Control Word Funttion RC1/RC0 | Default | 00 | | | | | |
| 70 | Register Control Word Funttion RC1/RC0 | R/C L | 50 | | | | | |
| 71 | Register Control Word Funttion RC5/RC4 | R/C L | 00 | | | | | |
| 72-116 | Reserved | - | 00 | | | | | |
| 117 | Module Manufacturer ID Code, Least Significant Byte | Transcend | 01 | | | | | |
| 118 | Module Manufacturer ID Code, Most Significant Byte | Transcend | 4F | | | | | |
| 119 | Module Manufacturing Location | - | 54 | | | | | |
| 120-121 | Module Manufacturing Date | - | 00 | | | | | |
| 122-125 | Module Serial Number | - | 00 | | | | | |
| 126-127 | Cyclical Redundancy Code | - | A4,3A | | | | | |
| 128-145 | Module Part Number | TS512MKR72V6NL | 54 | 53 | 35 | 31 | 32 | 4D |
| | | | 4B | 52 | 37 | 32 | 56 | 36 |
| | | | 4E | 4C | 20 | 20 | 20 | 20 |
| 146-147 | Revision Code | - | 00 | | | | | |
| 148-149 | DRAM Manufacturer ID Code | By Manufacturer | Variable | | | | | |
| 150-175 | Manufacturer Specific Data | By Manufacturer | Variable | | | | | |
| 176-255 | Open for customer use | Undefined | 00 | | | | | |