ATP Electronics, Inc.
750 North Mary Ave. Sunnyvale, CA 94085 U.S.A.
Tel: 408-732-5000
Fax: 408-732-5055
http://www.atpinc.com

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ATP AQ12M72E8BKH9S

4GB DDR3-1333 UNBUFFERED ECC DIMM

DESCRIPTION

The ATP AQ12M72E8BKH9S is a high performance 4GB DDR3-1333 Unbuffered ECC SDRAM memory module. It is organized as 512M x 72 in a 240-pin Dual-In-Line Memory Module (DIMM) package. The module utilizes eighteen 256Mx8 DDR3 SDRAMs in FBGA package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 4GB (512M x 72)
- DIMM Rank: 2 Ranks
- Cycle Time: 1.5ns (667MHz)
- CAS Latency: 9
- Power supply: 1.5V ± 0.075V
- Internal self calibration through ZQ
- Burst lengths: 8
- Auto & Self refresh
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Dynamic On Die Termination
- Fly-by topology
- PCB Height: 1.18 inches
- Asynchronous Reset
- RoHS compliant

Part No.	Max Freq	Interface
AQ12M72E8BKH9S	667MHz (1.5ns@CL=9) x2	SSTL_1.5

PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
A0~A9, A11~A14	SDRAM Address Bus	ODT0, ODT1	On die termination
A10/AP	Address Input/Auto precharge	VTT	SDRAM I/O termination supply
BA0~BA2	SDRAM Bank Select	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{RESET}$	Set DRAMs to Known State
CB0~CB7	DIMM ECC Check bits	$\overline{WE}$	Write Enable
CK0, CK1	Clock Inputs, positive line	$\overline{CS0}$, $\overline{CS1}$	Chip Selects
$\overline{CK0}$, $\overline{CK1}$	Clock inputs, negative line	SA0~SA2	I^2C serial bus data line for EEPROM
CKE0, CKE1	Clock Enables	SCL	I^2C serial bus clock for EEPROM
DM0~DM8	Data Masks	SDA	I^2C slave address select for EEPROM
DQ0~DQ63	Data Input/Output	TEST	Memory bus test tool (Not Connect and Not Useable on DIMMs)
DQS0~DQS8	Data strobes/ high data strobes	VDD	Core Power
$\overline{DQS0}$ ~ $\overline{DQS8}$	Data strobes(negative line)	VDDQ	I/O Driver Power
VREFDQ	Input/Output Reference supply	VDDSPD	SPD Power
VREFCA	Command/address reference supply	VSS	Ground
$\overline{Event}$	Reserved for optional hardware temperature sensing	NC	No Connect
		RSVD	Reserved for Future Use

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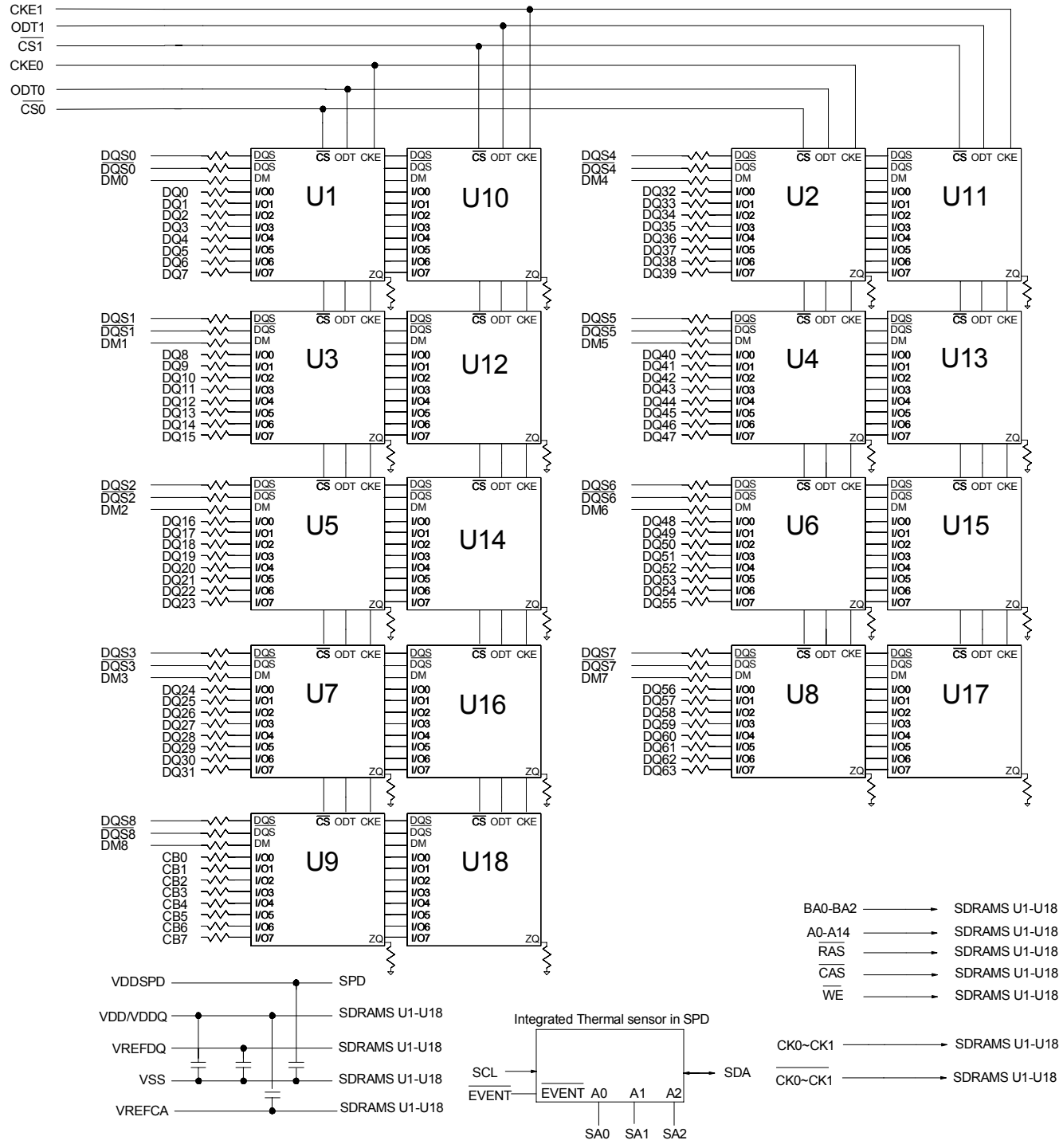
PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	DQ4	62	VDD	182	VDD
3	DQ0	123	DQ5	63	CK1	183	VDD
4	DQ1	124	VSS	64	$\overline{CK1}$	184	CK0
5	VSS	125	DM0	65	VDD	185	$\overline{CK0}$
6	$\overline{DQS0}$	126	NC	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	$\overline{EVENT}$
8	VSS	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	$\overline{RAS}$
13	DQ9	133	VSS	73	$\overline{WE}$	193	$\overline{CS0}$
14	VSS	134	DM1	74	$\overline{CAS}$	194	VDD
15	$\overline{DQS1}$	135	NC	75	VDD	195	ODT0
16	DQS1	136	VSS	76	$\overline{CS1}$	196	A13
17	VSS	137	DQ14	77	ODT1	197	VDD
18	DQ10	138	DQ15	78	VDD	198	NC
19	DQ11	139	VSS	79	NC	199	VSS
20	VSS	140	DQ20	80	VSS	200	DQ36
21	DQ16	141	DQ21	81	DQ32	201	DQ37
22	DQ17	142	VSS	82	DQ33	202	VSS
23	VSS	143	DM2	83	VSS	203	DM4
24	$\overline{DQS2}$	144	NC	84	$\overline{DQS4}$	204	NC
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	DQ22	86	VSS	206	DQ38
27	DQ18	147	DQ23	87	DQ34	207	DQ39
28	DQ19	148	VSS	88	DQ35	208	VSS
29	VSS	149	DQ28	89	VSS	209	DQ44
30	DQ24	150	DQ29	90	DQ40	210	DQ45
31	DQ25	151	VSS	91	DQ41	211	VSS
32	VSS	152	DM3	92	VSS	212	DM5
33	$\overline{DQS3}$	153	NC	93	$\overline{DQS5}$	213	NC
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	DQ30	95	VSS	215	DQ46
36	DQ26	156	DQ31	96	DQ42	216	DQ47
37	DQ27	157	VSS	97	DQ43	217	VSS
38	VSS	158	CB4	98	VSS	218	DQ52
39	CB0	159	CB5	99	DQ48	219	DQ53
40	CB1	160	VSS	100	DQ49	220	VSS
41	VSS	161	DM8	101	VSS	221	DM6
42	$\overline{DQS8}$	162	NC	102	$\overline{DQS6}$	222	NC
43	DQS8	163	VSS	103	DQS6	223	VSS
44	VSS	164	CB6	104	VSS	224	DQ54
45	CB2	165	CB7	105	DQ50	225	DQ55
46	CB3	166	VSS	106	DQ51	226	VSS
47	VSS	167	NC (TEST)	107	VSS	227	DQ60
48	NC	168	$\overline{RESET}$	108	DQ56	228	DQ61
		KEY		109	DQ57	229	VSS
49	NC	169	CKE1	110	VSS	230	DM7
50	CKE0	170	VDD	111	$\overline{DQS7}$	231	NC
51	VDD	171	NC	112	DQS7	232	VSS
52	BA2	172	A14	113	VSS	233	DQ62
53	NC	173	VDD	114	DQ58	234	DQ63
54	VDD	174	A12	115	DQ59	235	VSS
55	A11	175	A9	116	VSS	236	VDDSPD
56	A7	176	VDD	117	SA0	237	SA1
57	VDD	177	A8	118	SCL	238	SDA
58	A5	178	A6	119	SA2	239	VSS
59	A4	179	VDD	120	VTT	240	VTT
60	VDD	180	A3				

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975V	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975V	V	1,3
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1
Storage Temperature	T_{STG}	-55 to +100	°C	1,2
Operating Temperature	T_{CASE}	0 to +95	°C	1,2

Note:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6xVDDQ, When VDD and VDDQ are less than500mV; VREF may be equal to or less than 300mV.

AC & DC OPERATING CONDITIONS (SSTL- 1.5)

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units	Notes
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1,2
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1,2
$VREF_{DQ}$(DC)	I/O	0.49 * V_{DDQ}	0.50 * V_{DDQ}	0.51 * V_{DDQ}	V	4,5
$VREF_{DQ}$(DC)	I/O	0.49 * V_{DDQ}	0.50 * V_{DDQ}	0.51 * V_{DDQ}	V	4,5
Input High Voltage (DC)	V_{IH} (DC)	V_{REF} + 0.100	-	V_{DD}	V	3
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.175	-	-	V	3
Input Low Voltage (DC)	V_{IL} (DC)	V_{SS}	-	V_{REF} - 0.100	V	3
Input Low Voltage (AC)	V_{IL} (AC)	-	-	V_{REF} - 0.175	V	3

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, VREF = VREFDQ. For input only pins except RESET, or VREF = VREFCA
4. The ac peak noise on VREF may not allow VREF to deviate from VREF (DC) by more than ± 1% VDD (for reference: approx. ± 15mV)
5. For reference: approx. VDD/2 ± 15mV

IDD SPECIFICATION PARAMETER

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1,090	mA
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD =tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	1,230	mA
IDD2P	**Precharge power-down current;** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	660	mA
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	760	mA
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	760	mA
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	660	mA
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	950	mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD),tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCHING; Date bus inputs are SWITCHING	1,800	mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRAS-max(IDD), tRP = tRP(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are SWITCH-ING; Data pattern is same as IDD4W	1,750	mA
IDD5B	**Burst auto refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2,130	mA
IDD6	**Self refresh current**; CK and CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	230	mA
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC= tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	3,020	mA

TIMING PARAMETER

Parameter	Symbol	DDR3-1333		Units
		min	Max	
Clock cycle time at CL=9.0, CWL=9.0	tCK	1.5	<1.875	ps
Internal read command to first data	tAA	13.5(13.125[2])	20	ns
ACT to internal read or write delay time	tRCD	13.5(13.125[2])		ns
PRE command period	tRP	13.5(13.125[2])		ns
ACT to ACT or REF command period	tRC	49.5(49.125[2])		ns
ACTIVE to PRECHARGE command period	tRAS	36	9*tREFI	ns
Average high pulse width	tCH(avg)	0.47	0.53	tCK
Average low pulse width	tCL(avg)	0.47	0.53	tCK
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ		125	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38		tCK
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-500	250	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)		250	ps
Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	tDS(base)	30		ps
Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	tDH(base)	65		ps
DQS, $\overline{DQS}$ READ Preamble	tRPRE	0.9	-	tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3		tCK
DQS, $\overline{DQS}$ output high time	tQSH	0.4	-	tCK
DQS, $\overline{DQS}$ output low time	tQSL	0.4	-	tCK
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE	0.9	-	tCK
DQS, $\overline{DQS}$ WRITE Postamble	tWPST	0.3	-	tCK
DQS, $\overline{DQS}$ rising edge output access time from rising CK，$\overline{CK}$	tDQSCK	-255	255	ps
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	250	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	tCK
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	tCK
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	tCK
DLL locking time	tDLLK	512		nCK[1]
Internal READ Command to PRECHARGE Command delay	tRTP	max(4tCK,7.5ns)		
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)		
WRITE recovery time	tWR	15		ns
Mode Register Set command cycle time	tMRD	4		nCK[1]
Mode Register Set command update delay	tMOD	max(12tCK,15ns)		
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	4		nCK[1]
Auto precharge write recovery + precharge time	tDAL	tWR + roundup (tRP / tCK)		nCK[1]
Multi-Purpose Register Recovery Time	tMPRR	1		nCK[1]
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4tCK,6ns)		
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)		
Four activate window for 1KB page size	tFAW	30		ns
Four activate window for 2KB page size	tFAW	45		ns
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65		ps
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140		ps
Power-up and RESET calibration time	tZQinitI	512		nCK[1]
Normal operation Full calibration time	tZQoper	256		nCK[1]
Normal operation short calibration time	tZQCS	64		nCK[1]
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+ 10ns)		
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP		max(3tCK,6 ns)	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-250	250	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK
RTT dynamic change skew	tADC	0.3	0.7	tCK
2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	160		ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+10ns)		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)		nCK[1]
Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI	tCK
Write leveling output delay	tWLO	0	9	ns
Write leveling output error	tWLOE	0	2	ns

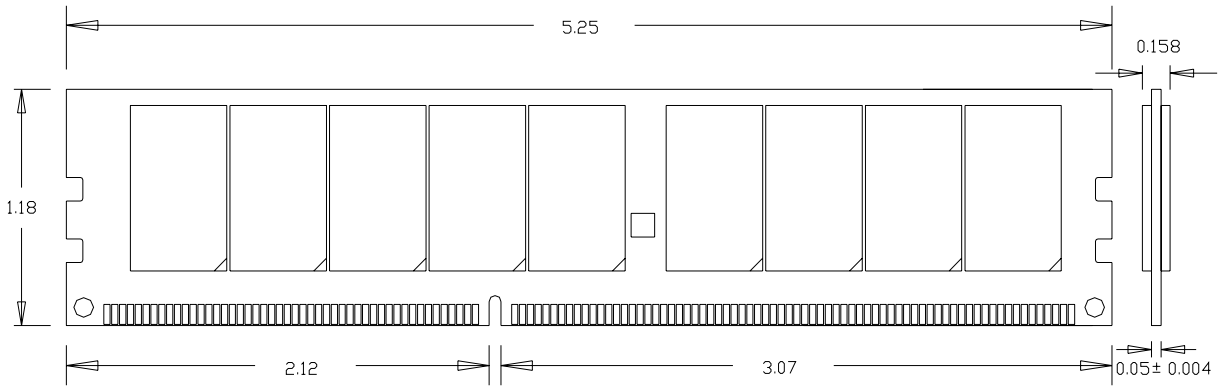
1:Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
2: For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match.

PHYSICAL DIMENSIONS (UNITS IN INCHES)

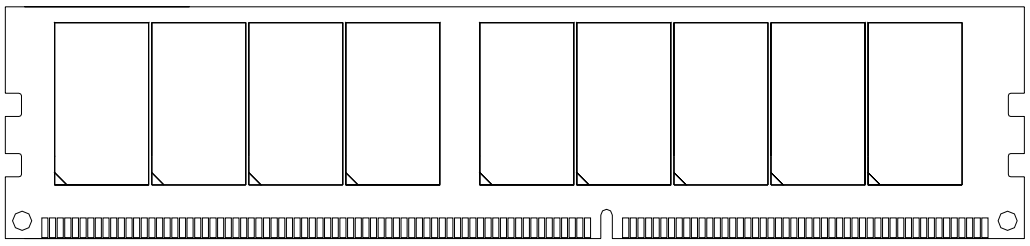
(Drawing not to scale)

240-pin DIMM

Front



Back



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