

# **USB 2.0 Disk Module Specification**

**(Type A and Type B)**

**Version 1.13**

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**K. PCB Board Dimension (Unit: mm) (PCB P/N: C7152X12OGN1-MA).21**

**Revision History**

<b>Revision</b>	<b>History</b>	<b>Draft Date</b>	<b>Author</b>
1.0	First Release	18-Jan-08	Steven
1.1	Add top view and bottom view	30-May-08	Steven
1.2	Modify pin header define & add 2D diagram	16-Oct-08	Steven
1.3	Add Appendix: Part Number Table	03-Nov-08	Ekron
1.4	Change D4. USB pin header drawing Add Appendix B: Toshiba Part Number	06-Nov-08	Ekron
1.5	Advantech Release	31-Dec-08	Ethan
1.6	Modify P/N information	23-Feb-09	Tones
1.7	Modify pin header description	24-Mar-09	Tones
1.8	Modify PCB board screw hole size	6-Apr-09	Tones
1.9	Increase Endurance and Waveform	26-May-09	Tones
1.10	Increase Mechanical and MTBF data	4-Jun-09	Tones
1.11	Fixed the Vibration and Shock data	24-Jun-09	Tones
1.12	Define form template	29-Jul-09	Tones
1.13	Modify system features	11-Nov-09	Tones

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## **A. General Description**

The Advantech SQFlash UDM (USB Disk Module) is based on USB 2.0 controller which supports USB 2.0 & 1.1 and interface to NAND Flash Memory. This USB Disk Module is specially designed for motherboard and build-in to the PC / Notebook / IA system.

By using this UDM solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. It supports USB Mass Storage function and supports for USB boot function from BIOS. This solution provides not only easy to install, but also fast, easy to use and low cost way for user.

## B. Controller Features

- **Support Host Interfaces**
  - USB 2.0 & 1.1 Interface
- **Support USB HID transport**
  - Endpoint 3
- **Support Flash Memory Interfaces**
  - Build-in NAND Flash Memory
- **USB Interface**
  - Fully compatible with USB Specification Version 2.0 & 1.1
  - High speed 480Mbit/second supporting
  - Full speed 12Mbit/second supporting
  - Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
  - Support four Endpoints
  - Support Data Payload
  - Support USB power saving mode
- **Build-In NAND Flash Memory Interface**
  - Build-in hardware ECC circuit.
  - Support SLC (Single level cell) 2k-page large block NAND Flash.
  - Support SLC (Single level cell) 4k-page large block NAND Flash.
  - Support MLC (Multi level cell) 2k-page Large Block NAND flash.
  - Support MLC (Multi level cell) 4k-page Large Block NAND flash.
  - Support MLC (Multi level cell) 8k-page Large Block NAND flash.
- **Support In-System Programming through USB Port**
- **Transfer Rate for USB Interface**
  - “High speed” Up to 480Mbits/sec for USB 2.0
  - “Full speed” Up to 12Mbits/sec for USB 1.1
- **Support 3.3V Flash I/O**
  - Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.
- **Support 1.8V Flash I/O**
  - Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.
- **Operating Voltage**
  - 2.7 ~ 3.6V.
- **USB bus-powered capability.**
- **Power saving implemented.**
- **Working Frequency:**
  - 12MHz

## C. System Features

### ■ Capacities

- SLC type : 1GB · 2GB · 4GB · 8GB

### ■ Flash type

- Only use SLC (single level cell) NAND flash of average 10 times lifecycle and much faster against MLC (multiple level cell)

### ■ 3.3V / 5V operation voltage

### ■ Error Detection / Correction Core (EDC/ECC)

- Built-in EDC/ECC up to 12 random bits error per 512 bytes.

### ■ Wear Leveling

- Built-in Static and Dynamic wear leveling function

### ■ Temperature Ranges

- Commercial Temperature
  - 0°C to 70°C for operating
  - -40°C to 85°C for storage

### ■ Performance

- SLC type
  - Sustain Read Speed up to 30 MB/s
  - Sustain Write Speed up to 20 MB/s

### ■ Humidity

- Operating Humidity: 5% ~ 95%
- Non-Operating Humidity: 5% ~ 95%

### ■ Endurance

- SLC type: > 5,000,000 program/erase cycles

### ■ MTBF

- > 6,000,000 hours

### ■ Mechanical Specification

- Vibration : 20G Peak, 80 ~ 2,000 Hz, 3 Axes
- Shock : 2,500G Peak

### ■ NAND flash Data Retention

- 10 years

### ■ PCB Size: 26.5 x 37.8 x 1.6 mm

## D. General Description

### ■ Advanced NAND Flash Controller

Advantech SQFlash UDM includes Bad Block Management Algorithm, Wear Leveling Algorithm and Error Detection / Correction Code (EDC/ECC) Algorithm.

### ■ Bad Block Management

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash UDM implement an efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

### ■ Wear Leveling

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash UDM provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

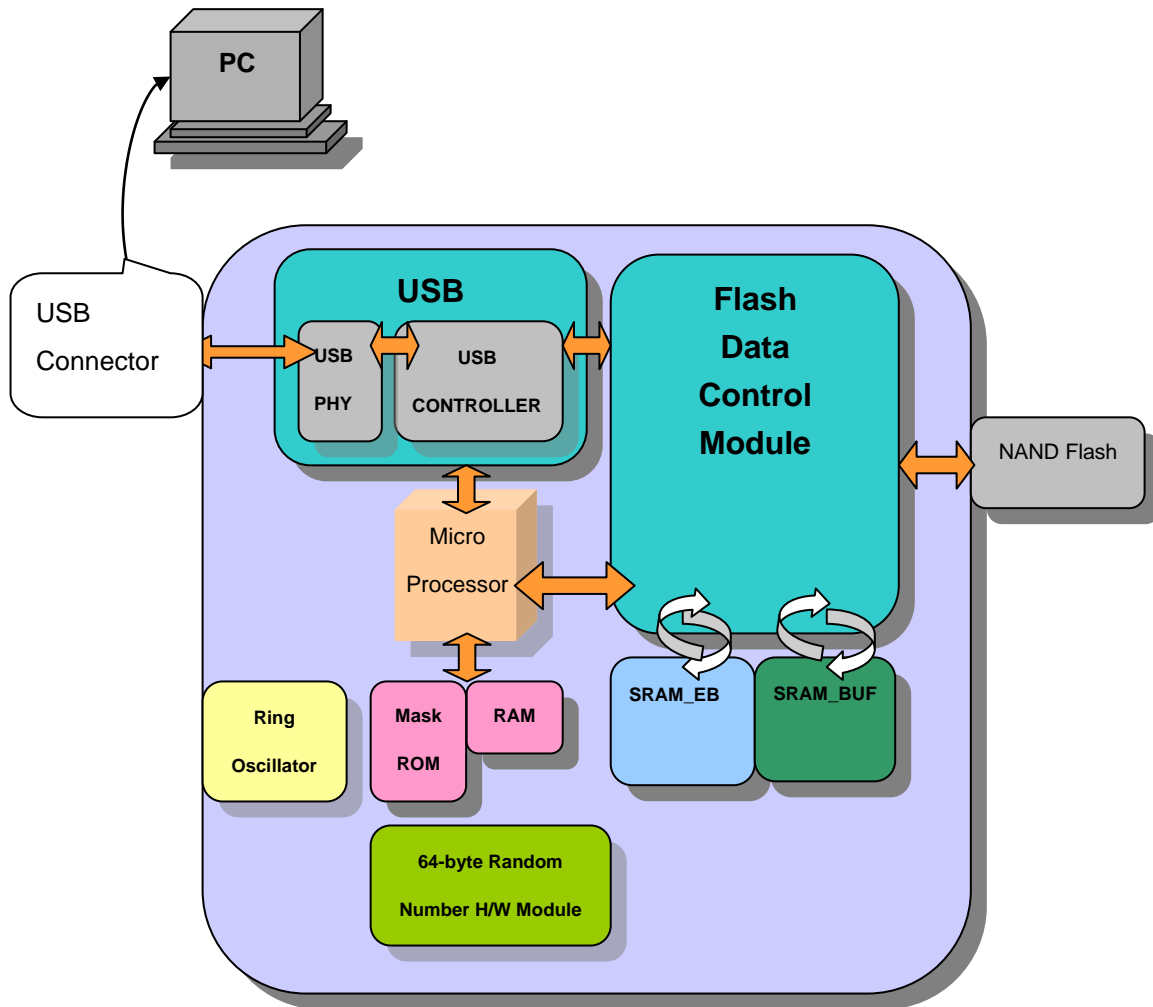
### ■ Error Detection / Correction

Advantech SQFlash UDM utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. Built-in EDC/ECC up to 12 random bits error per 512 bytes.

### ■ Sophisticate Product Management Systems

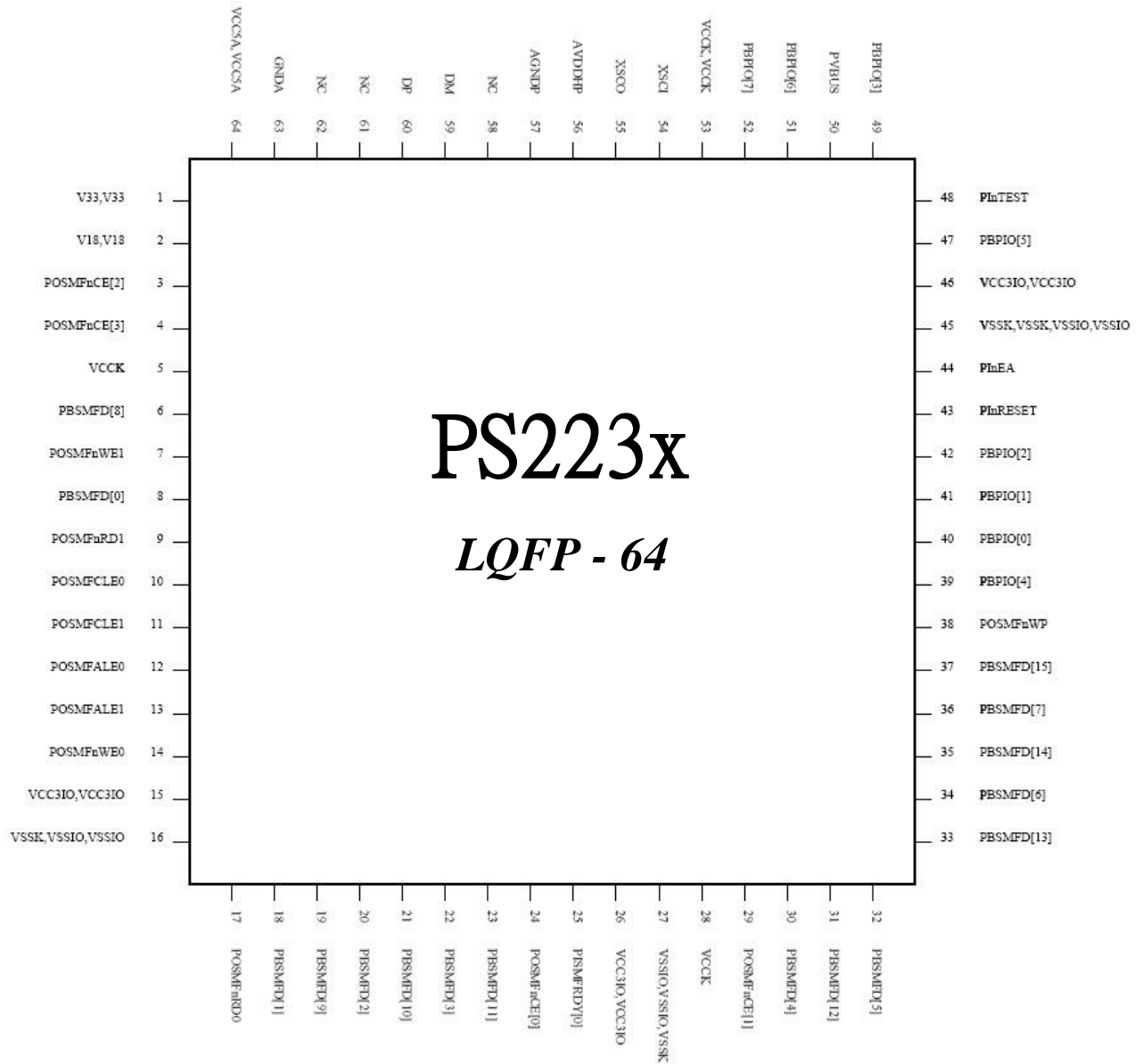
Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

## E. BLOCK DIAGRAM



## F. Pin Assignment and Description

### Pin Assignment - 64pins



### Pins Listed in Numeric Order – 64pins

Specifications subject to change without notice, contact your sales representatives for the most update information.

Pin	Signal	Pin	Signal	Pin	Signal
1	V33	23	PBSMFD[11]	45	VSSIO/VSSK
2	V18	24	PBSMFnCE[0]	46	VCC3IO
3	PBSMFnCE[2]	25	PISMFRDY[0]	47	PBPIO[5]
4	PBSMFnCE[3]	26	VCC3 IO	48	PlnTEST
5	VCCK	27	VSSIO/VSSK	49	PBPIO[3]
6	PBSMFD[8]	28	VCCK	50	PVBUS
7	POSMFnWE1	29	POSMFnCE[1]	51	PBPIO[6]
8	PBSMFD[0]	30	PBSMFD[4]	52	PBPIO[7]
9	POSMFnRD1	31	PBSMFD[12]	53	VCCK
10	POSMFCLE0	32	PBSMFD[5]	54	XSCI
11	POSMFCLE1	33	PBSMFD[13]	55	XSCO
12	POSMFALE0	34	PBSMFD[6]	56	VCC33A_HSRT
13	POSMFALE1	35	PBSMFD[14]	57	GND33A_HSRT
14	POSMFnWE0	36	PBSMFD[7]	58	NC
15	VCC3IO	37	PBSMFD[15]	59	DM
16	VSSIO,VSSK	38	POSMFnWP	60	DP
17	POSMFnRD0	39	PBPIO[4]	61	NC
18	PBSMFD[1]	40	PBPIO[0]	62	NC
19	PBSMFD[9]	41	PBPIO[1]	63	GND A
20	PBSMFD[2]	42	PBPIO[2]	64	VCC5A
21	PBSMFD[10]	43	PlnRESET		
22	PBSMFD[3]	44	PlnEA		

### Pin Description – 64pins

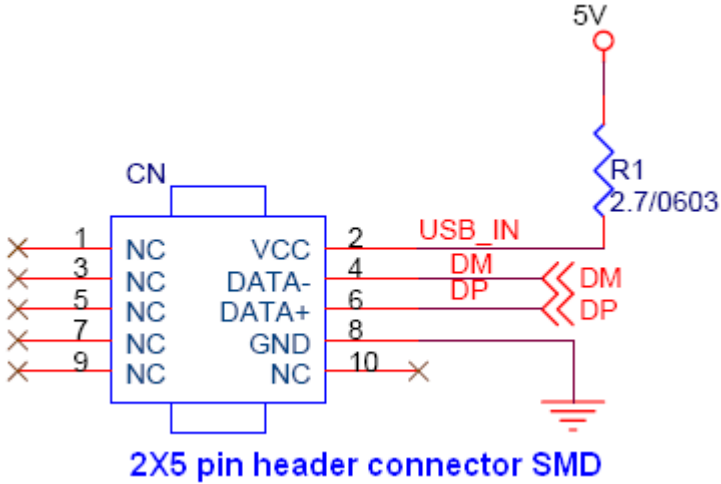
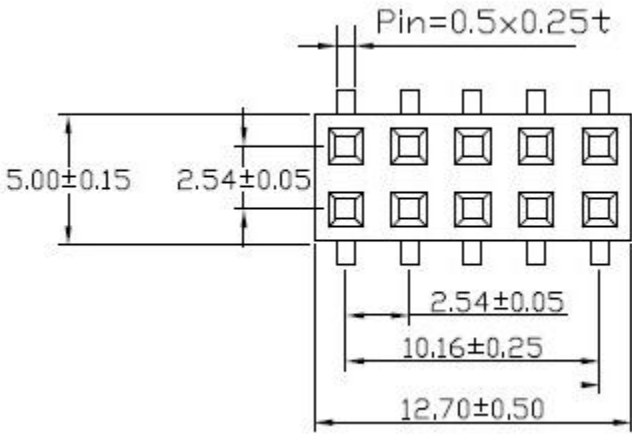
USB + Regulator Interface		
Pin Name	Dir.	Pin Description
V18	VCC18	1.8V regulator power supply
V33	VCC33	3.3V regulator power supply
VCC5A	VCC5	5.0V regulator power input
GND A	GND	0V regulator ground reference input
DP	I/O	USB 2.0 data in positive pin terminal.
DM	I/O	USB 2.0 data in negative pin terminal.
RREF	I	Connect to external reference resistor(12K±1%) to GND.
VCC33A_HSRT	VCC33	USB 2.0 IO power (3.3V)
GND33A_HSRT	GND	USB 2.0 IO ground reference (0V)
VCC33A_PLL	VCC33	USB 2.0 PLL power (3.3V)
GND33A_PLL	VCC33	USB 2.0 PLL ground (0V)
XSCO	O	Crystal oscillator output
XSCI	I	Crystal oscillator input
VCCK	I	USB 2.0 core power (1.8V)
NC		No Connection

FLASH Interface		
Pin Name	Dir.	Pin Description
POSMFnCE[3:0]	O	Flash chip enable, low active.
PBSMFD[15:0]	I/O	Flash data bus
POSMFALE0, POSMFALE1	O	Flash address latch enable, high active.
POSMFCLE0, POSMFCLE1	O	Flash command latch enable, high active.
POSMFnRD0, POSMFnRD1	O	Flash read control signal, low active.
POSMFnWE0, POSMFnWE1	O	Flash write control signal, low active.
POSMFnWP	O	Flash write protect control signal, low active.
PISMFRDY[0]	I	Flash ready/busy signal input

Global Signal		
Pin Name	Dir.	Pin Description
PInRESET	I	Reset Signal
PInTEST	I	Test Mode Signal.
PInEA	I	EAMODE Select Signal.
PVBUS	I	USB VBUS input
PBPIO[7:0]	I/O	8-bit GPIO
VCC3IO	VCC33	3.3V IO power
VCCK	VCC18	1.8V digital core power
VSSIO	GND	0V IO ground reference
VSSK	GND	0V digital core ground reference

### USB Pin Header Type A Size & Defines (Unit: mm) – 10pins

Specifications subject to change without notice, contact your sales representatives for the most update information.



**USB Pin Header Type A Description – 10pins**

<b>USB Pin Header Description – Type A</b>		
<b>No.</b>	<b>Pin Name</b>	<b>Pin Description</b>
1	NC	No Connection
2	VCC	5.0V USB Bus power input
3	NC	No Connection
4	DM	USB 2.0 data in negative pin terminal.
5	NC	No Connection
6	DP	USB 2.0 data in positive pin terminal.
7	NC	No Connection
8	GND	0V regulator ground reference input.
9	NC	No Connection
10	NC	No Connection

## G. System Power Consumption

Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Normal	66.00	67.03
Suspend	0.38	0.39
Sleep	0.38	0.38
Read	91.08	104.12
Write	93.88	118.74
Un-configured	42.24	42.46

The above values are for reference only; it may change according to the flash memory used.

## H. Electrical Specifications

### Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+5.5	V
2	$V_{IN}$	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	$T_a$	Operating Temperature (Commercial)	0	+70	°C
4	$T_a$	Operating Temperature (Industrial)	-40	+85	°C
5	$T_{st}$	Storage Temperature (Commercial)	-40	+85	°C
6	$T_{st}$	Storage Temperature (Industrial)	-50	+125	°C

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature (Commercial)	$T_a$	0	+25	+70	°C
Operating Temperature (Industrial)	$T_a$	-40	+25	+85	°C
$V_{DD}$ Voltage	$V_{DD}$	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

## I. DC Characters

DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V <sub>CK</sub>	Core Power Supply	Core Area	1.62	1.8	1.98	V
V <sub>CC3IO</sub>	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	°C
V <sub>t</sub>	Switching threshold	LVTTL		1.5		V
V <sub>t-</sub>	Schmitt Trigger Negative Going threshold voltage	LVTTL	0.8	1.1		V
V <sub>t+</sub>	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
V <sub>ol</sub>	Output Low voltage	I <sub>ol</sub>   = 2 ~ 16 mA			0.4	V
V <sub>oh</sub>	Output High voltage	I <sub>oh</sub>   = 2 ~ 16 mA	2.4			V
R <sub>pu</sub>	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
R <sub>pd</sub>	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = V <sub>CC3I</sub> or 0			1	μA
I <sub>oz</sub>	Tri-state Output Leakage Current		-10	±1	10	μA

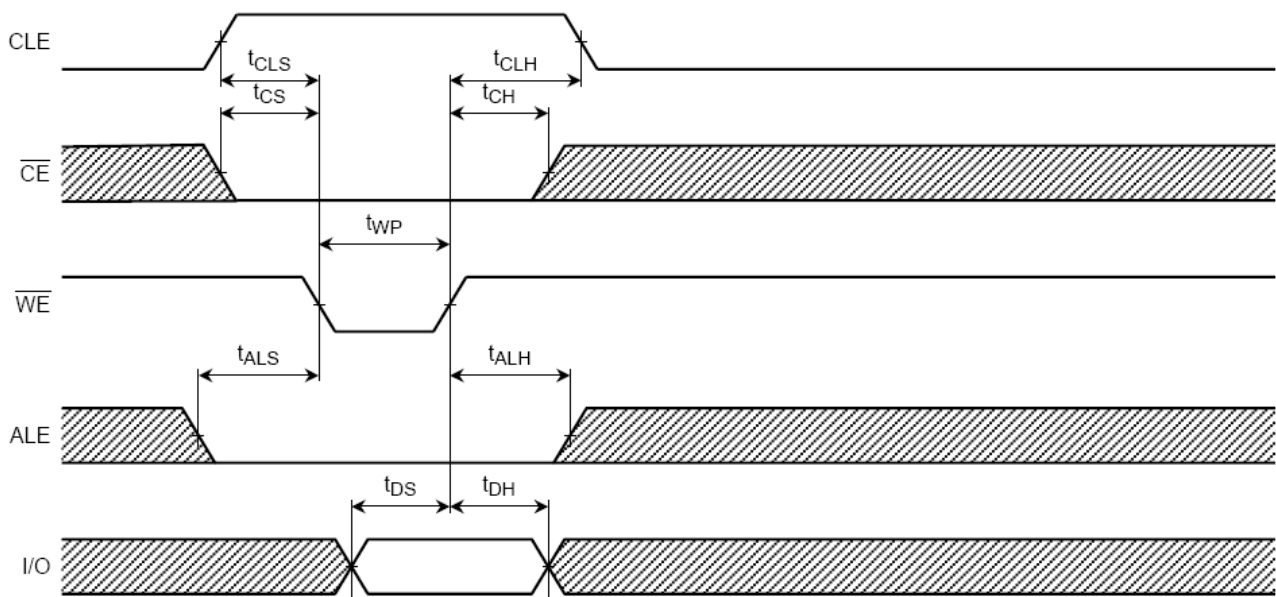
## J. AC Characters

### Flash Memory Interface Timing

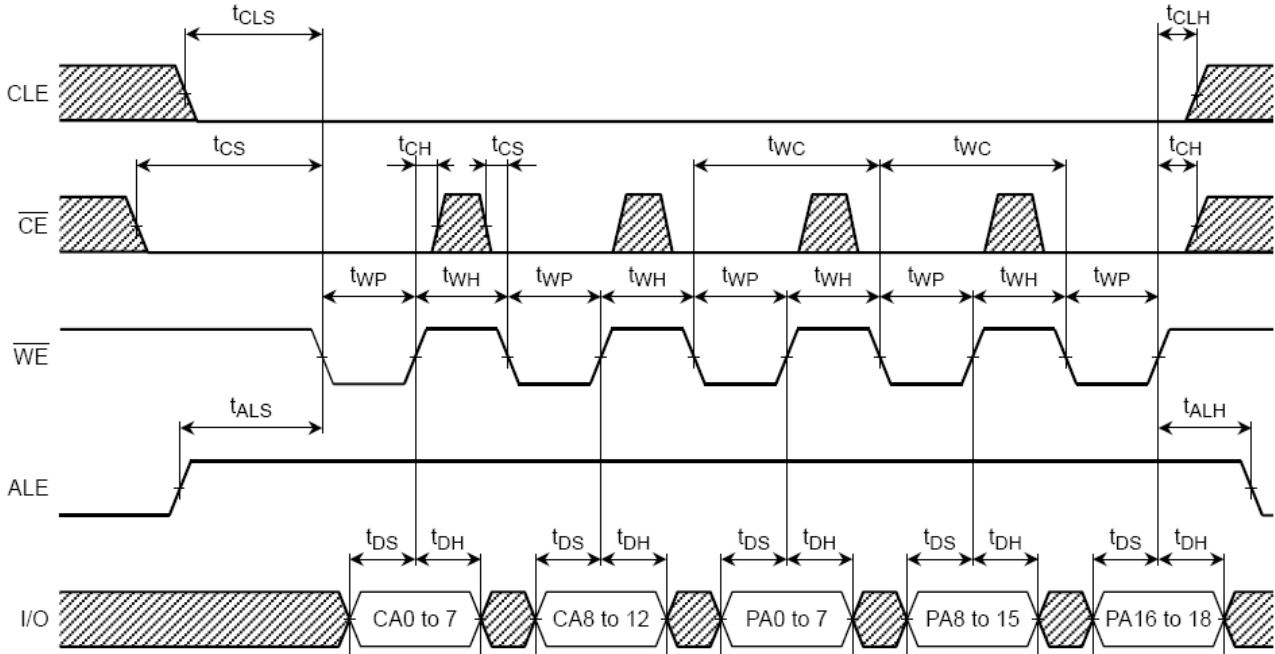
*NAND Flash Memory Interface Timing*

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	$t_{CLS}$	0	-	ns
CLE Hold Time	$t_{CLH}$	10	-	ns
CE Setup Time	$t_{CS}$	0	-	ns
CE Hold Time	$t_{CH}$	10	-	ns
WE Pulse Width	$t_{WP}$	25	-	ns
ALE Setup Time	$t_{ALS}$	0	-	ns
ALE Hold Time	$t_{ALH}$	10	-	ns
Data Setup Time	$t_{DS}$	20	-	ns
Data Hold Time	$t_{DH}$	10	-	ns
Write Cycle Time	$t_{WC}$	45	-	ns
WE High Hold Time	$t_{WH}$	15	-	ns
Read Cycle Time	$t_{RC}$	50	-	ns
/RE Pulse Width	$t_{RP}$	25	-	ns
/RE High Hold Time	$t_{REH}$	15	-	ns
Ready to /RE Low	$t_{RR}$	60	-	ns

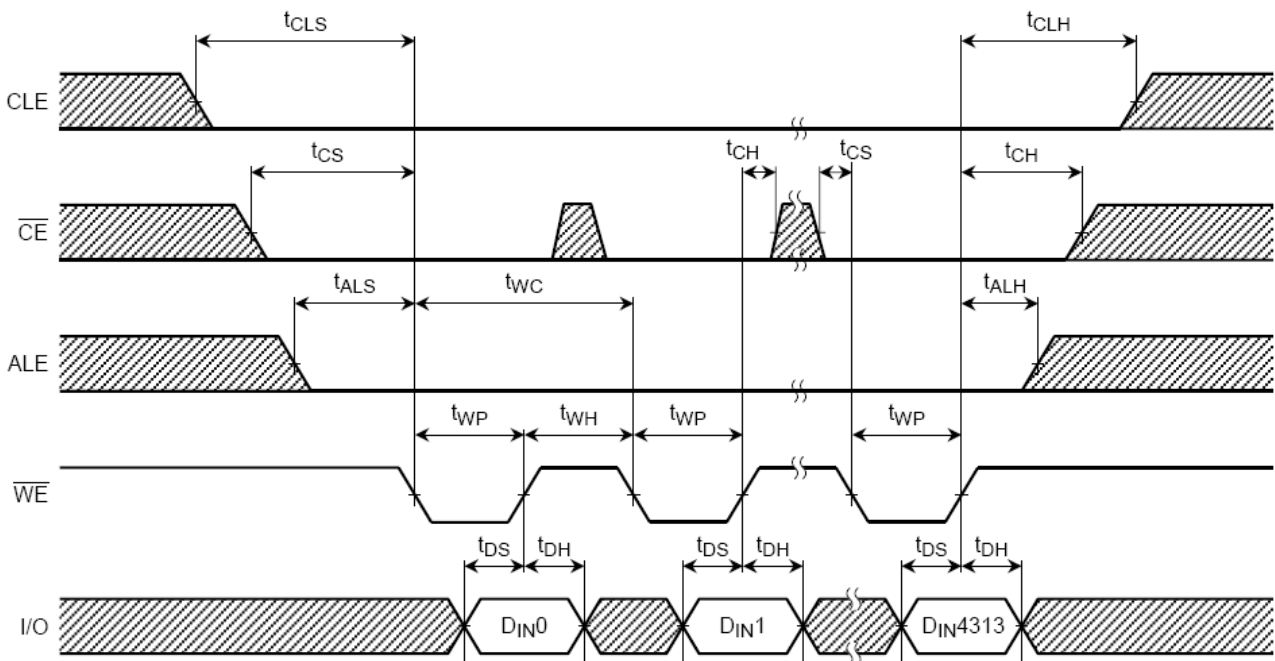
### Command Input Cycle Timing



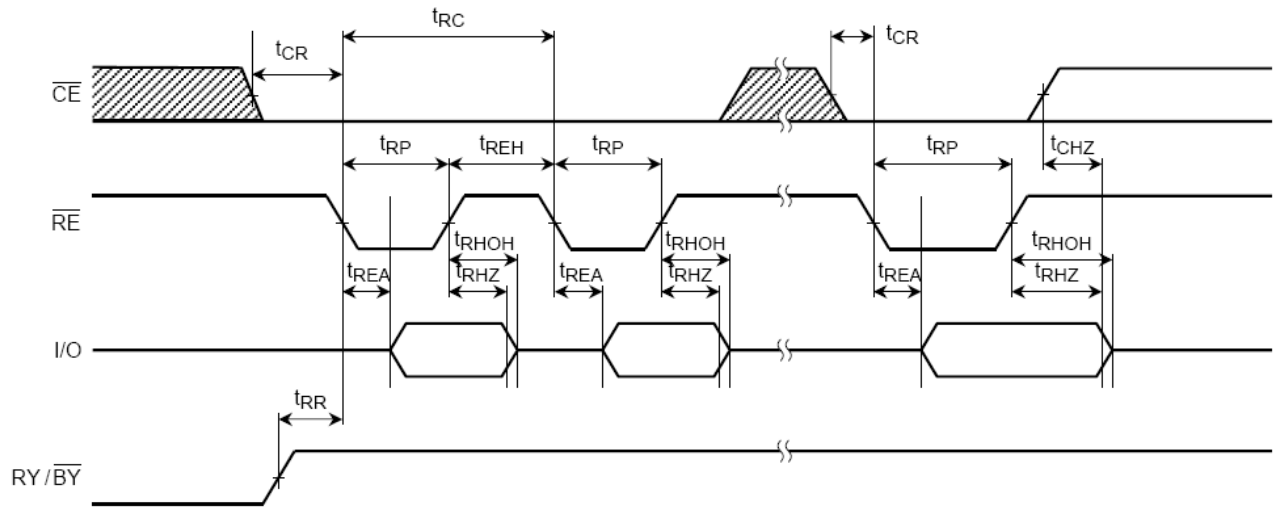
**Address Input Cycle Timing**



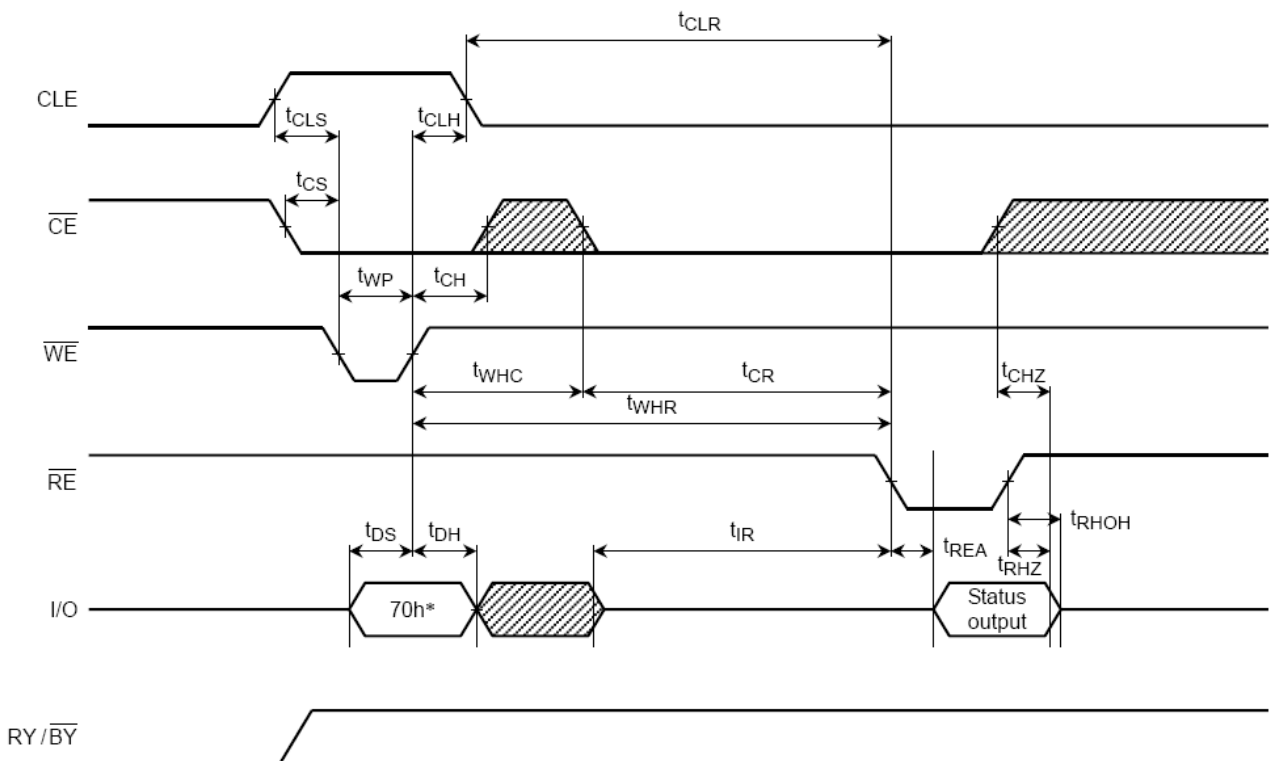
**Data Input Cycle Timing**



**Serial Read Cycle Timing**

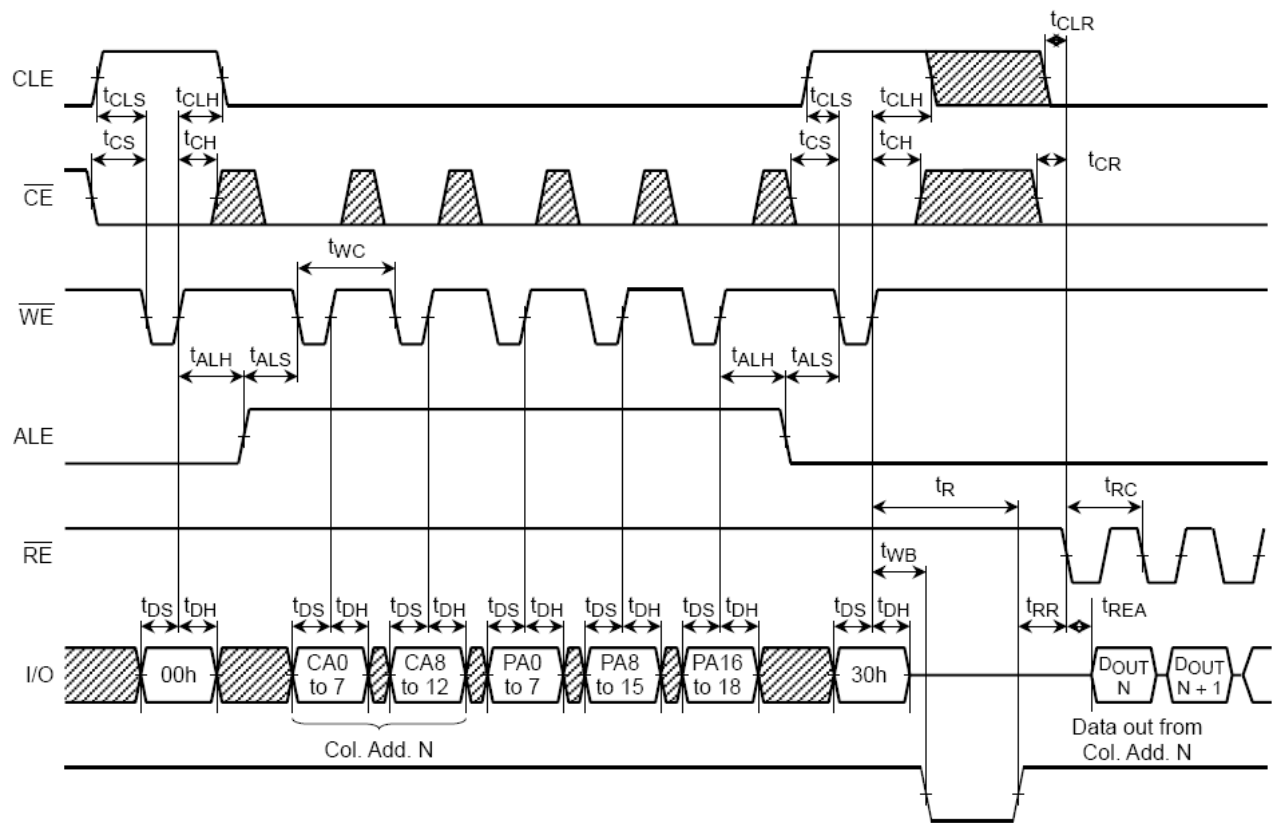


**Status Read Cycle Timing**

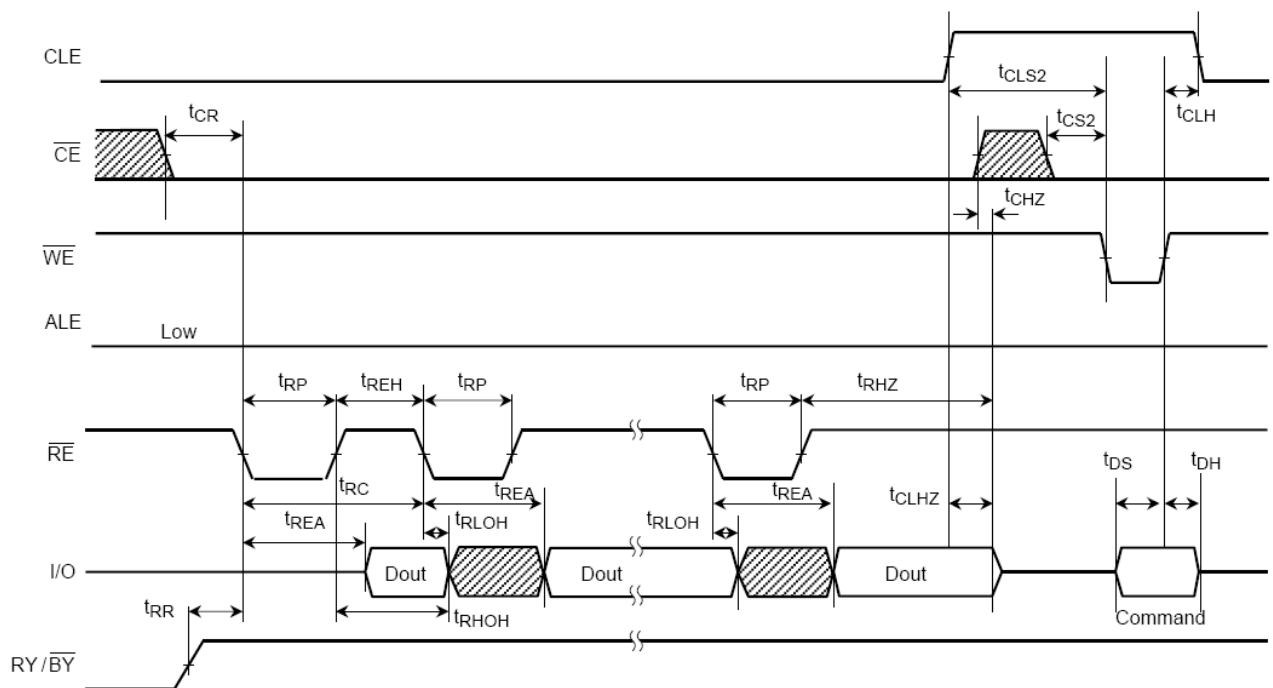


**Read Cycle Timing**

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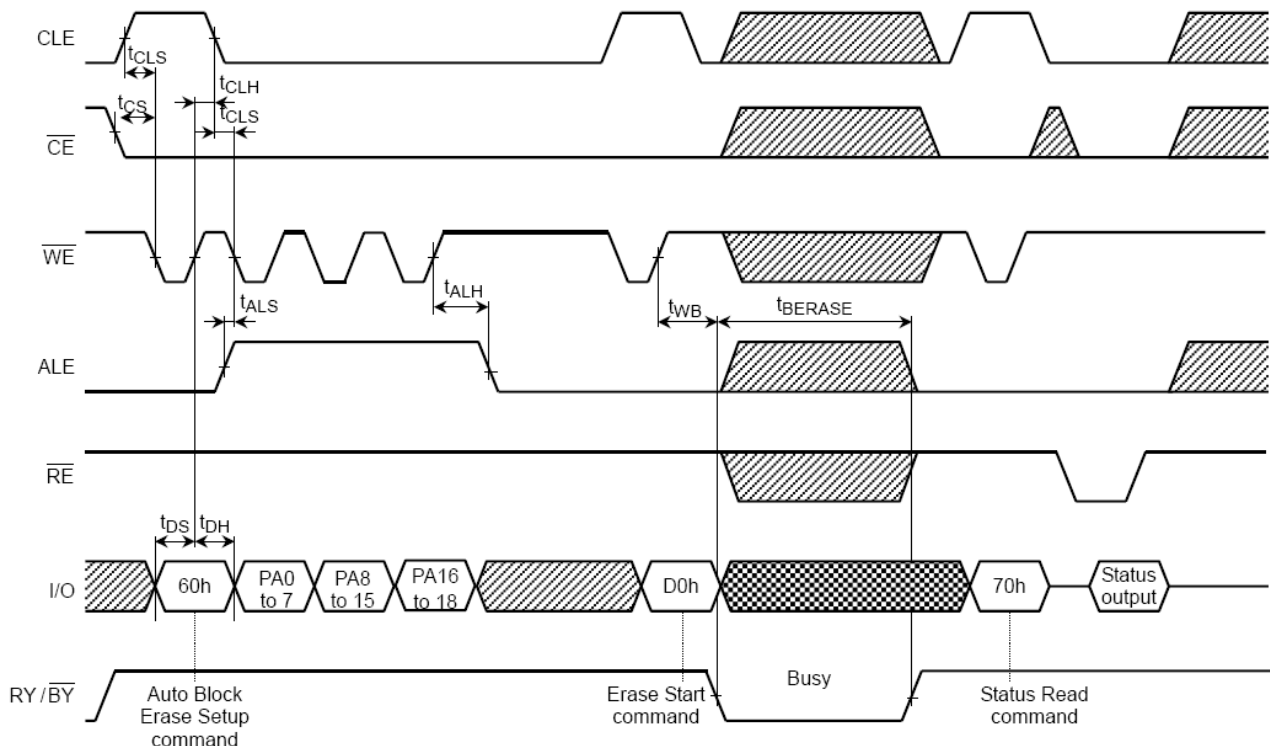


**Data Output Timing**

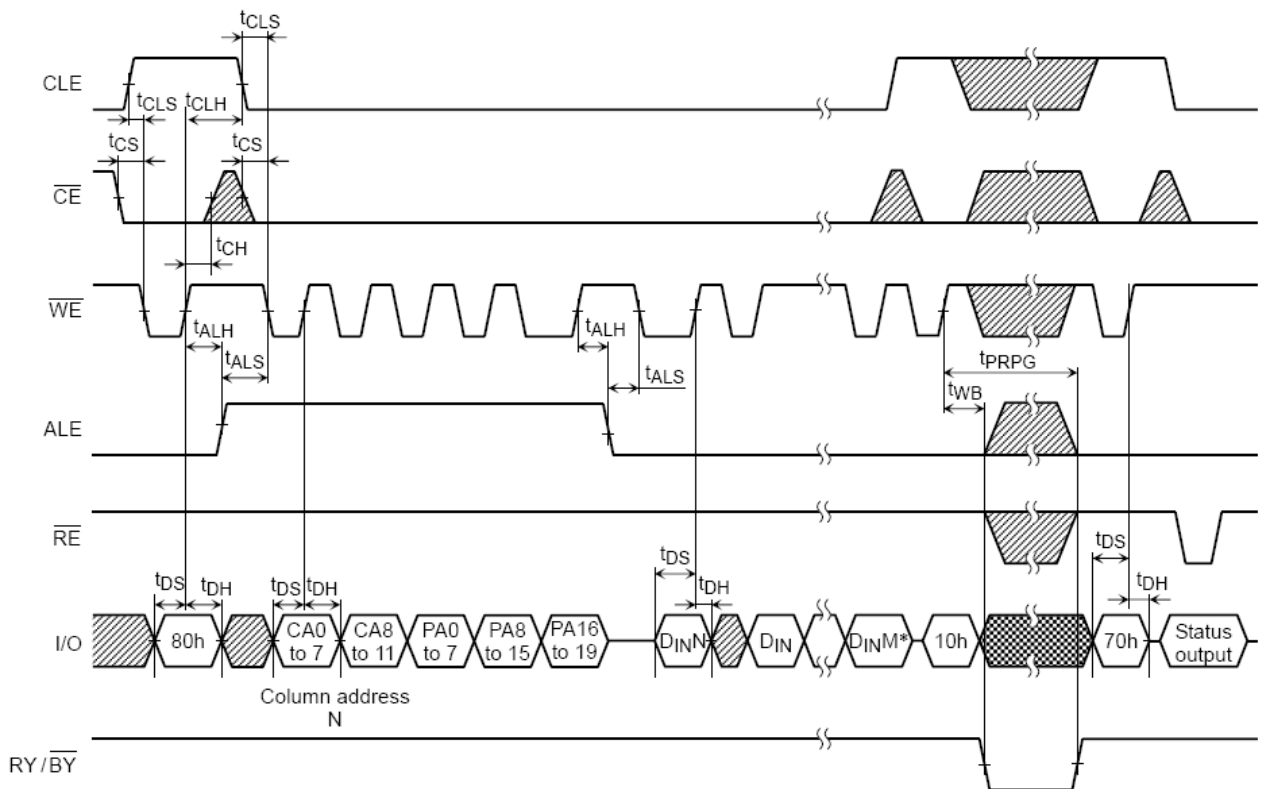


**Auto Block Erase Timing**

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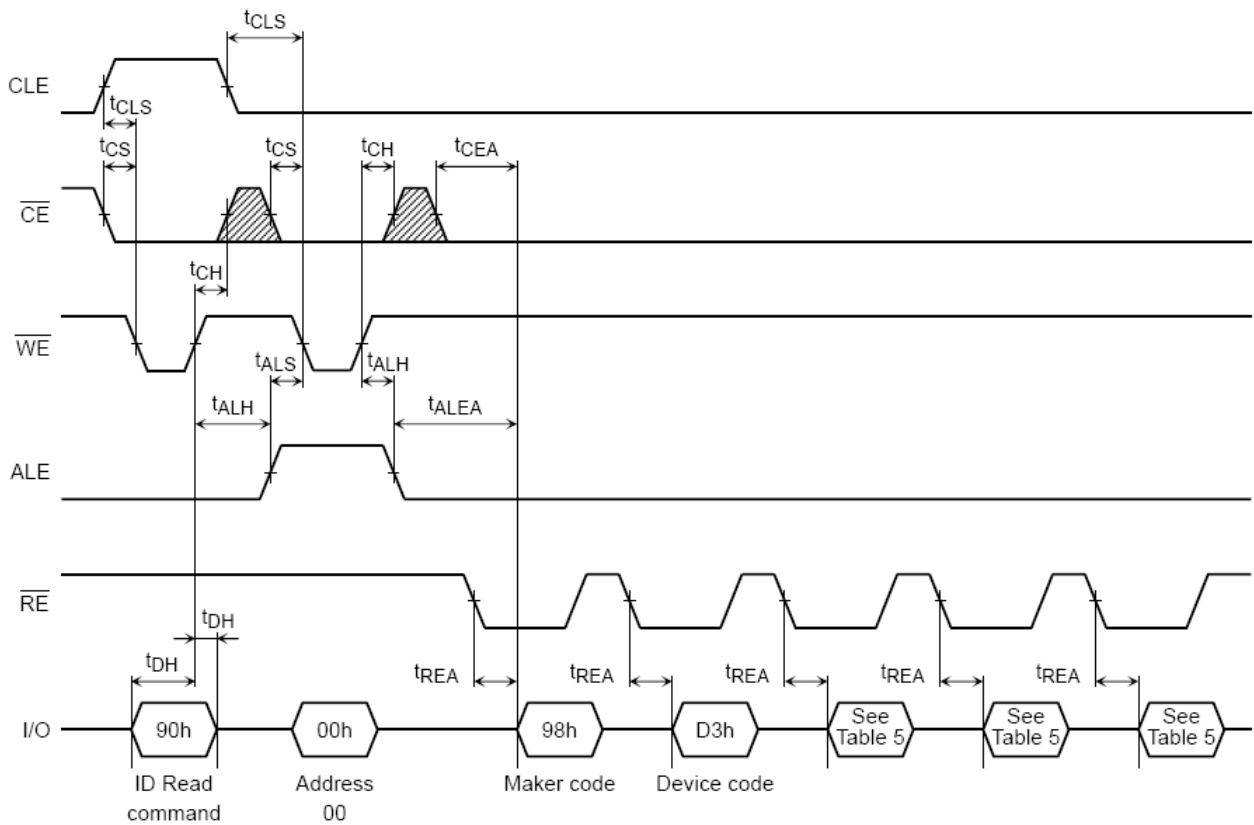


**Auto-Program Operation Timing**

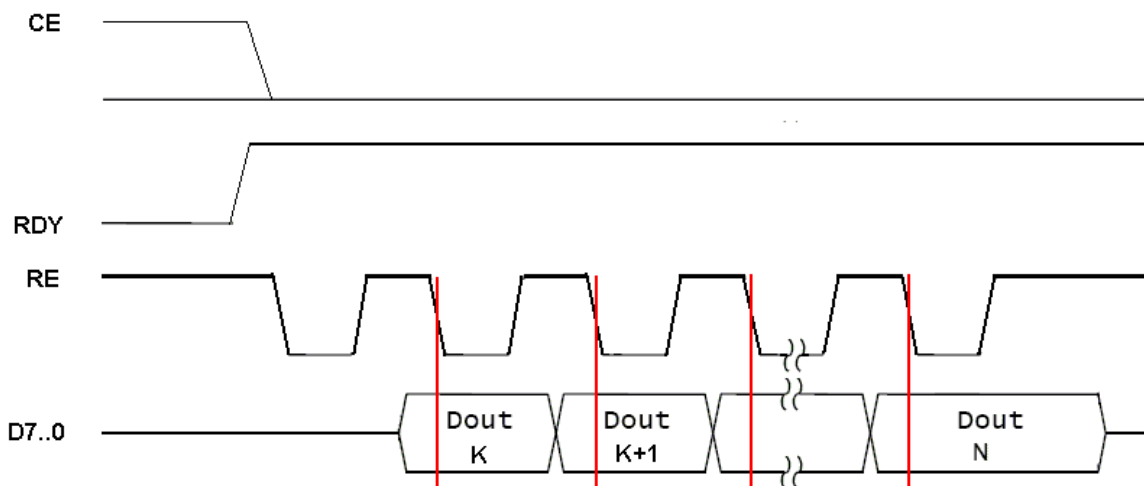


**ID Read Operation Timing**

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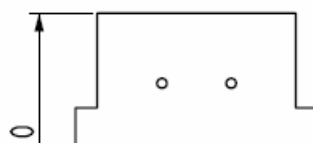
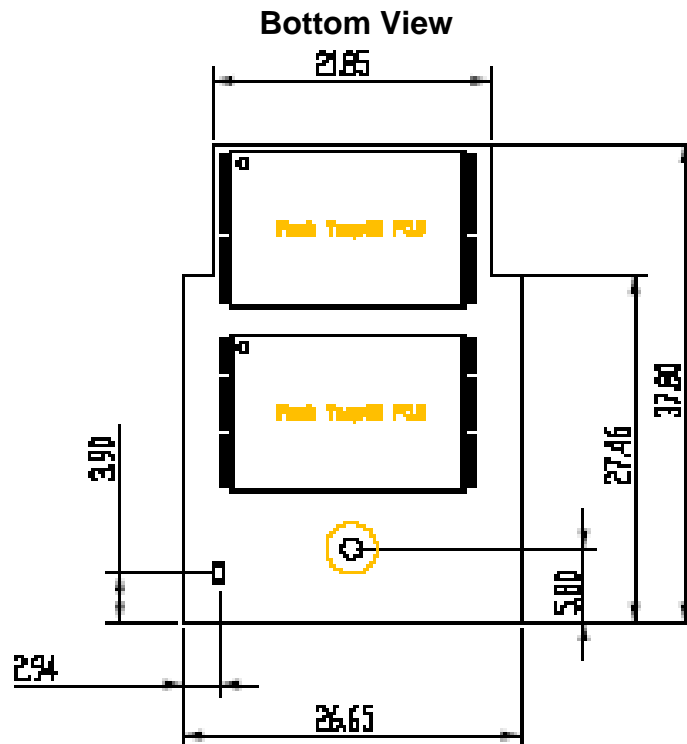
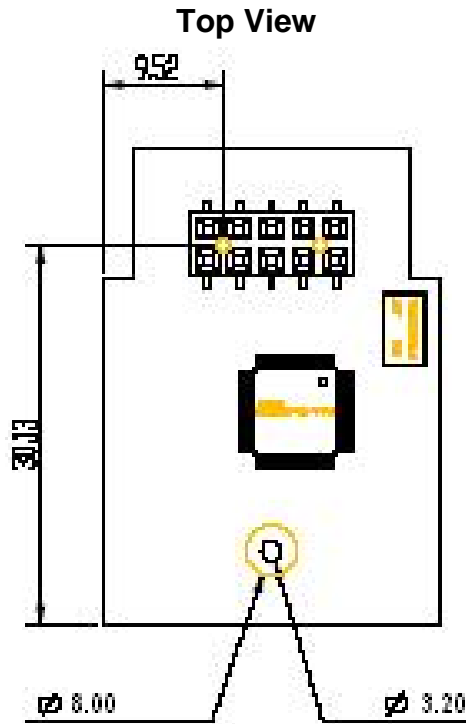


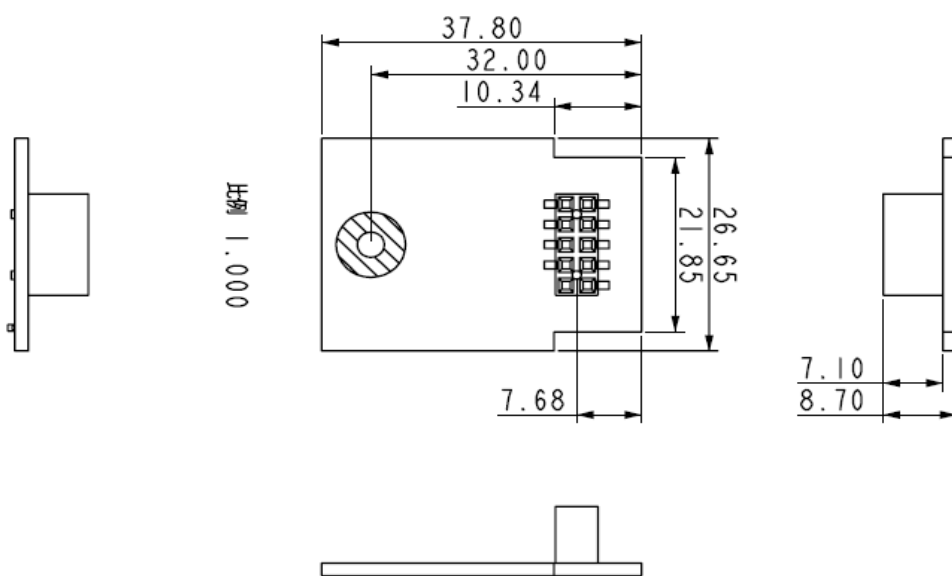
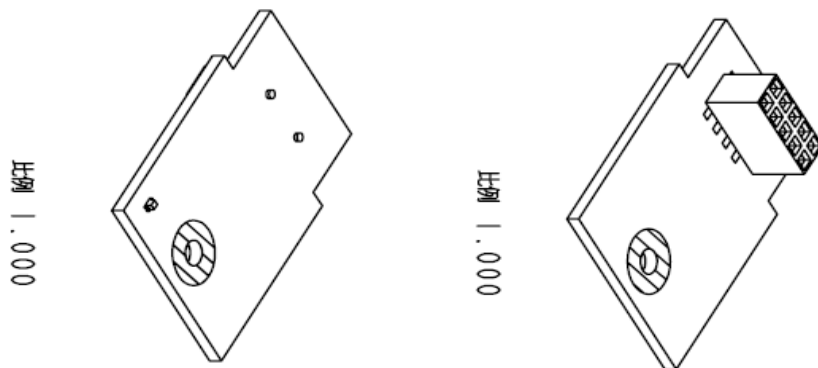
**EDO mode for data latch**



EDO mode to latch the data at the negative edge of RE.

**K. PCB Board Dimension (Unit: mm) (PCB P/N: C7152X120GN1-MA)**





## Appendix A: Product Part Number Table

<b>Product</b>	<b>Advantech PN</b>
Advantech SQFlash 1G UDM HOR LP MOUNTING SCREW	SQF-UDMS1-1G-HAE
Advantech SQFlash 2G UDM HOR LP MOUNTING SCREW	SQF-UDMS2-2G-HAE
Advantech SQFlash 4G UDM HOR LP MOUNTING SCREW	SQF-UDMS2-4G-HAE
Advantech SQFlash 8G UDM HOR LP MOUNTING SCREW	SQF-UDMS2-8G-HAE