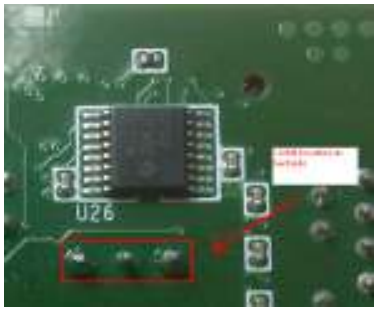
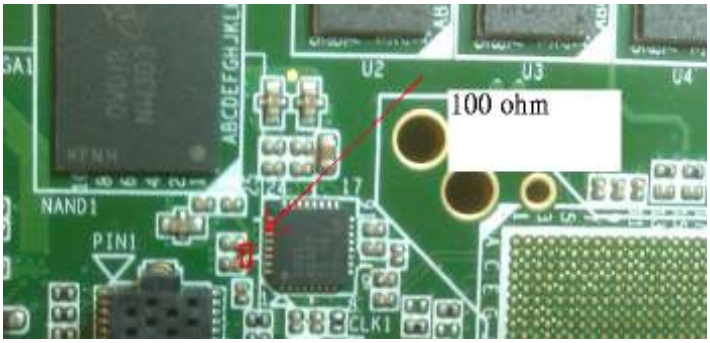
1. Fold the middle pin of power jack and move the power jack to backside to avoid the interference with AMC golden finger

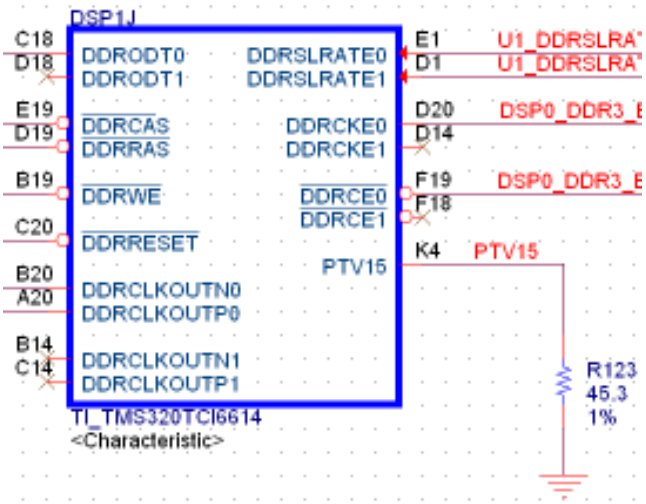

2. Move the COM1 to backside and adopt a 90 degree connector to avoid the interference with XDS560V2 mezzanine card.



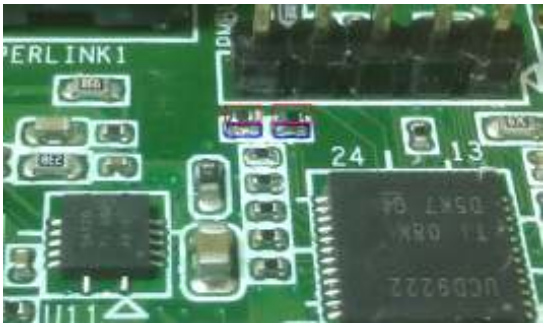
3. The CDCE62002 do not have built in 100-ohm terminations, so add a 100-ohm resistor across the CLK1 sides of the C46 and C51 for REFCKP/N inputs to CLK1 (DDR3 reference clock)

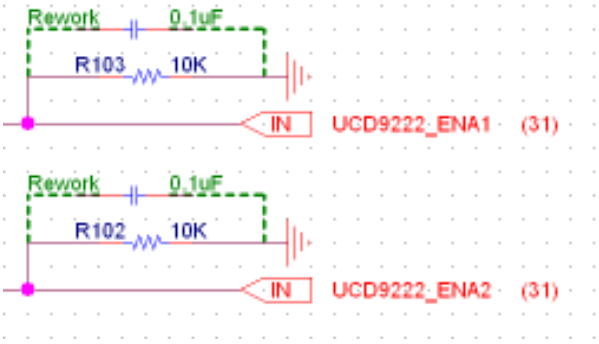


4. Change the value of R123 to 45.3 ohm

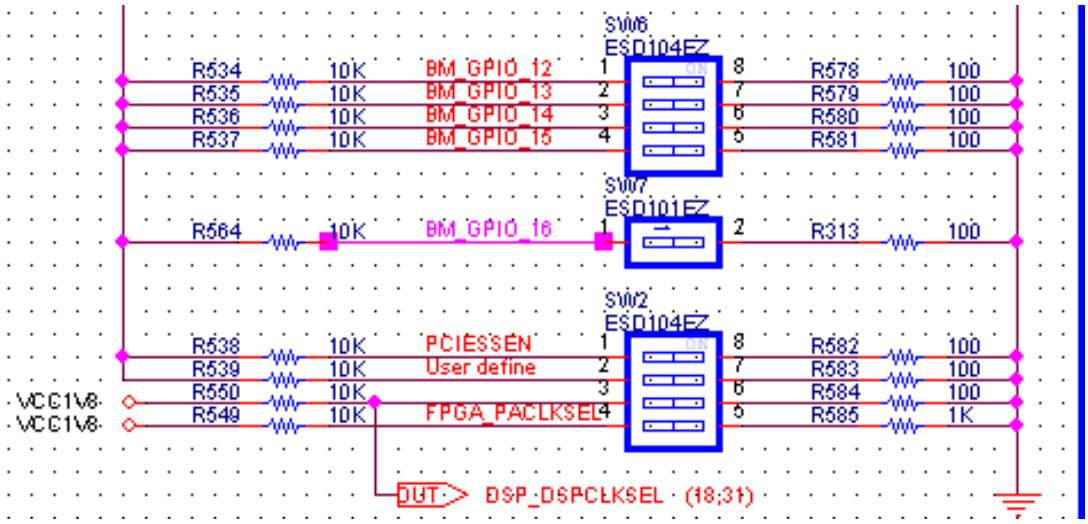


5. Due to the UCD74106 unstable issue, parallel the 0.1uF capacitor at R102 and R103 to filter the noise on UCD9222_ENA1 and UCD9222_ENA1





6. BM_GPIO_16 is not connected to FPGA, and so we make a workaround on FPGA code to control GPIO16 with SW2(user define pin)



7. The footprint of OSC1(VCTCXO) are too small to assembly on PCB. We will measure the clock signal after SMT to assure the functionality.