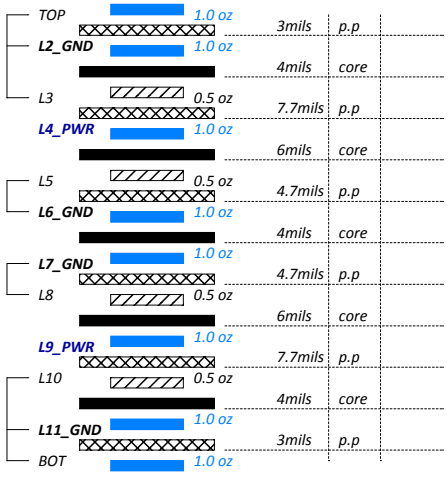
TMS320TCI6614 EVM Board for TI

Rev. A101-1 (Alpha2)

PCB PN : 19C2830300

Project Code :

PCB Thickness : 69 mils(1.75mm)
12 Layers



NOTE: THESE SCHEMATICS ARE REFERENCE ONLY.
FOR COMMITTED PERFORMANCE AND FUNCTIONALITY
OF THE TMS320TCI6614 DEVICE, PLEASE REFER
TO THE DEVICE DATA MANUAL.

Texas Instruments
12203 SW Freeway
Stafford, TX 77477
USA

Designed for TI by ADVANTECH DSPM-8303E

TEXAS INSTRUMENTS ADVANTECH

Title		
COVER PAGE		
Size: C	Document Number: TMS320TCI6614	Rev: A101
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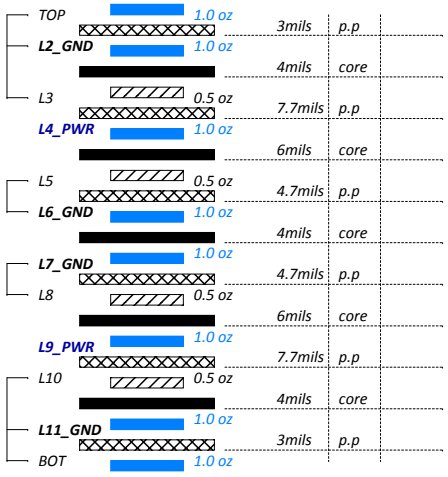
TMS320TCI6614 EVM Board for TI

Rev. A101-1 (Alpha2)

PCB PN : 19C2830300

Project Code :

PCB Thickness : 69 mils(1.75mm)
12 Layers



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TMDXEVM6614LXE Revision Table

TMDXEVM6614LXE Rev 1.0 (Alpha1 / PCB-19C2830300)

Item	Description	Page
A	The UART connector interfers with the XDS560V2 mezzanine card 1. Move the COM1 to backside of PCB and use a 90 degree connector on Alpha 1 and Alpha 2 units 2. Move the COM1 location to fix the interference on Beta PCB	16
B	The footprint pitches of OSC1 (VCTCXO) was incorrect to not fit the assembly of PCB 1. The facility fixed this issue by the processes of PCB assembly on Alpha1 and Alpha2 units 2. Fix the VCTCXO footprint on Beta PCB	27
C	Change the value of R123 to 45.3 ohm	14
D	The power jack was interferred with AMC breakout board and Adpater 1. Move the power jack to backside of PCB to avoid the interference with AMC breakout board on Alhpa 1 and Alpha 2 units 2. Rotate the power jack to fix this issue on Beta PCB	11
E	The SW7 of sliding switch, BM_GPIO_16 was missed to connect the FPGA for the SOC boot configurations 1. Take the User_Define bit on SW2 to be the bit of GPIO16 configuration of SOC on Alpha1 and Alpha2 units 2. Route the BM_GPIO16 to pin N3 of FPGA on Beta PCB	32
F	The CDCE62002 do not have built in 100 ohm terminations at inputs 1. Paralle a 100 ohm resistor across the CLK1 sides of the C46 and C51 on Alpha1 and Alpha 2 2. Add the location R597 on Beta PCB	22
G	UCD9222 Enable pins were coupled of the noises when VCC1v0 (UCD74106) had over 2 amps loading. 1. Parallel a 0.1uF capacitor at R102 and R103 to filter the noise on UCD9222_ENA1 and UCD9222_ENA1 (power enabling pins) on Alpha1 and Alpha 2 units 2. Add the locaton C576 and C577 on Beta PCB	34
H	The symbol of the GPS chip in the schematics, TC6000G, was not matched as the spec.It will modify the symbol to match the TC6000G specification on Beta version.	27
I	The GPS_EN was not followed by TC6000G timing requirement. It will modify the EN pin contorlled by the FPGA for a proper timing on Beta version.	27

TMDXEVM6614LXE Rev 2.0 (Alpha2 / PCB-19C2830300)

Item	Description	Page
A	Change SOC to Rev 1.1 silicon	
B	Alll ECNs were implied on Alpha 2 units	

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Title: TMDXEVM6614LE Revision Table

Size	Document Number	Rev
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Title: TITLE & TABLE OF CONTENTS

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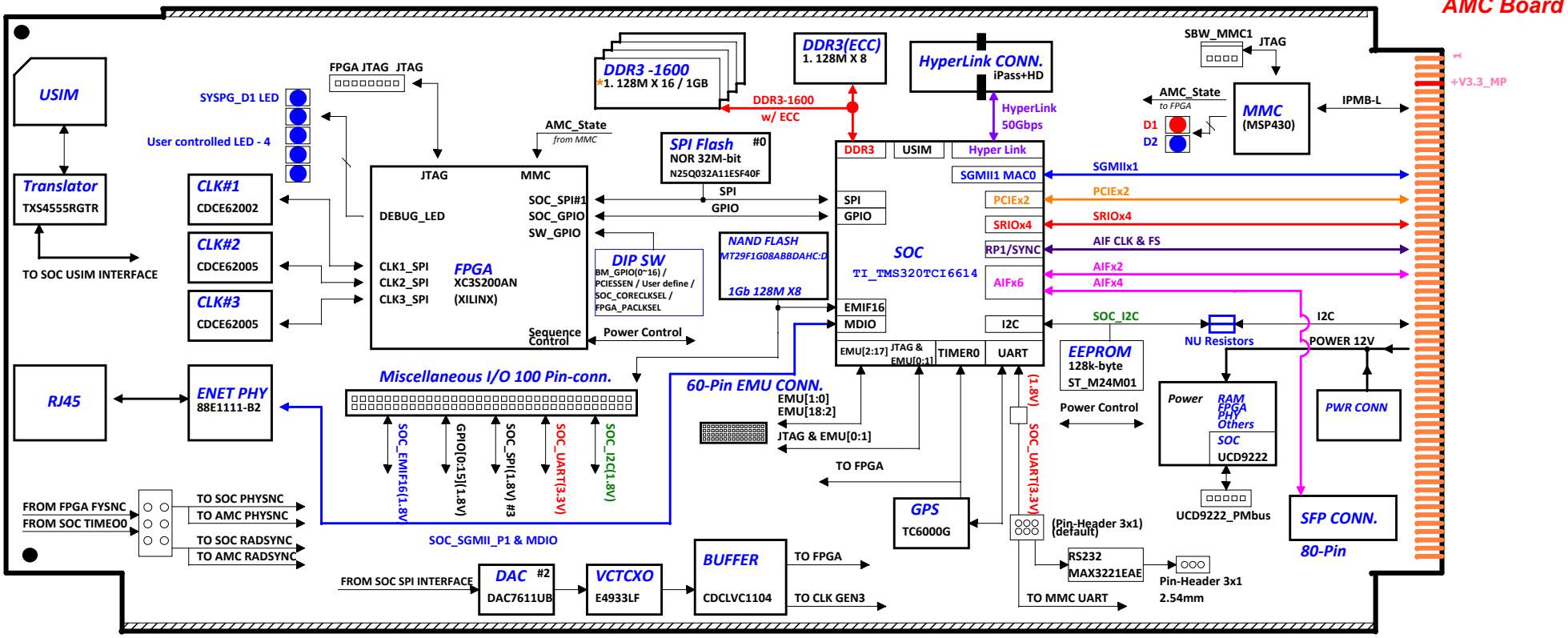
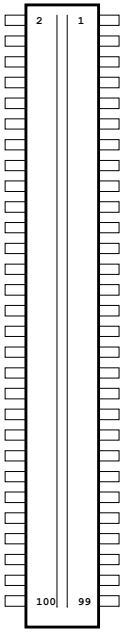
TMS320TCI6614 EVM BLOCK DIAGRAM



Miscellaneous I/O 100 Pin conn. Signal

PIN	Port mapping
02	GND
04	EMIFA00
06	EMIFA01
08	EMIFA02
10	EMIFA03
12	EMIFA04
14	GND
16	EMIFA05
18	EMIFA06
20	EMIFA07
22	EMIFA08
24	EMIFA09
26	GND
28	EMIFA10
30	EMIFA11
32	EMIFA12
34	EMIFA13
36	EMIFA14
38	GND
40	EMIFA15
42	EMIFA16
44	EMIFA17
46	EMIFA18
48	EMIFA19
50	GND

PIN	Port mapping
52	EMIFA20
54	EMIFA21
56	EMIFA22
58	EMIFA23
60	GND
62	GPIO00
64	GPIO01
66	GPIO02
68	GPIO03
70	GPIO04
72	GPIO05
74	GPIO06
76	GPIO07
78	GPIO08
80	GPIO09
82	GPIO10
84	GPIO11
86	GPIO12
88	GPIO13
90	GPIO14
92	GPIO15
94	GND
96	CLK2_SYNC
98	CLK3_SYNC
100	GND



EMIFCE2Z

PIN	Port mapping
01	GND
03	SDA
05	SCL
07	GND
09	EMIFD0
11	EMIFD1
13	EMIFD2
15	EMIFD3
17	GND
19	EMIFD4
21	EMIFD5
23	EMIFD6
25	EMIFD7
27	GND
29	EMIFD8
31	EMIFD9
33	EMIFD10
35	EMIFD11
37	GND
39	EMIFD12
41	EMIFD13
43	EMIFD14
45	EMIFD15
47	GND
49	EMIFCE1Z

PIN	Port mapping
51	GPIO16
53	GND
55	EMIFBE0z
57	EMIFBE1z
59	EMIFOEz
61	EMIFWEz
63	EMIFRnW
65	EMIFWAIT1
67	GND
69	TIMI0
71	TIMO0
73	TIMI1
75	TIMO1
77	GND
79	SSPMISO
81	SSPMOSI
83	SSPCS3
85	SSPCK
87	GND
89	GND
91	UARTTXD
93	UARTRXD
95	UARTRTS
97	UARTCTS
99	GND

AMC Port mapping

Port	Port mapping
TCLKA	TCLKA
TCLKB	TCLKB
FCLKA	100MHz
00	SGMII
01	
02	
03	
04	PCI-E_1
05	PCI-E_2
06	
07	
08	SRIO_1
09	SRIO_2
10	SRIO_3

Port	Port mapping
11	SRIO_4
12	
13	
14	
15	
17	AIF_4
	TCLKC / TCLKD
18	AIF_5
19	AIF_CLK & FS
20	Expansion I2C
JTAG	

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Title	BLOCK DIAGRAM_AMC	
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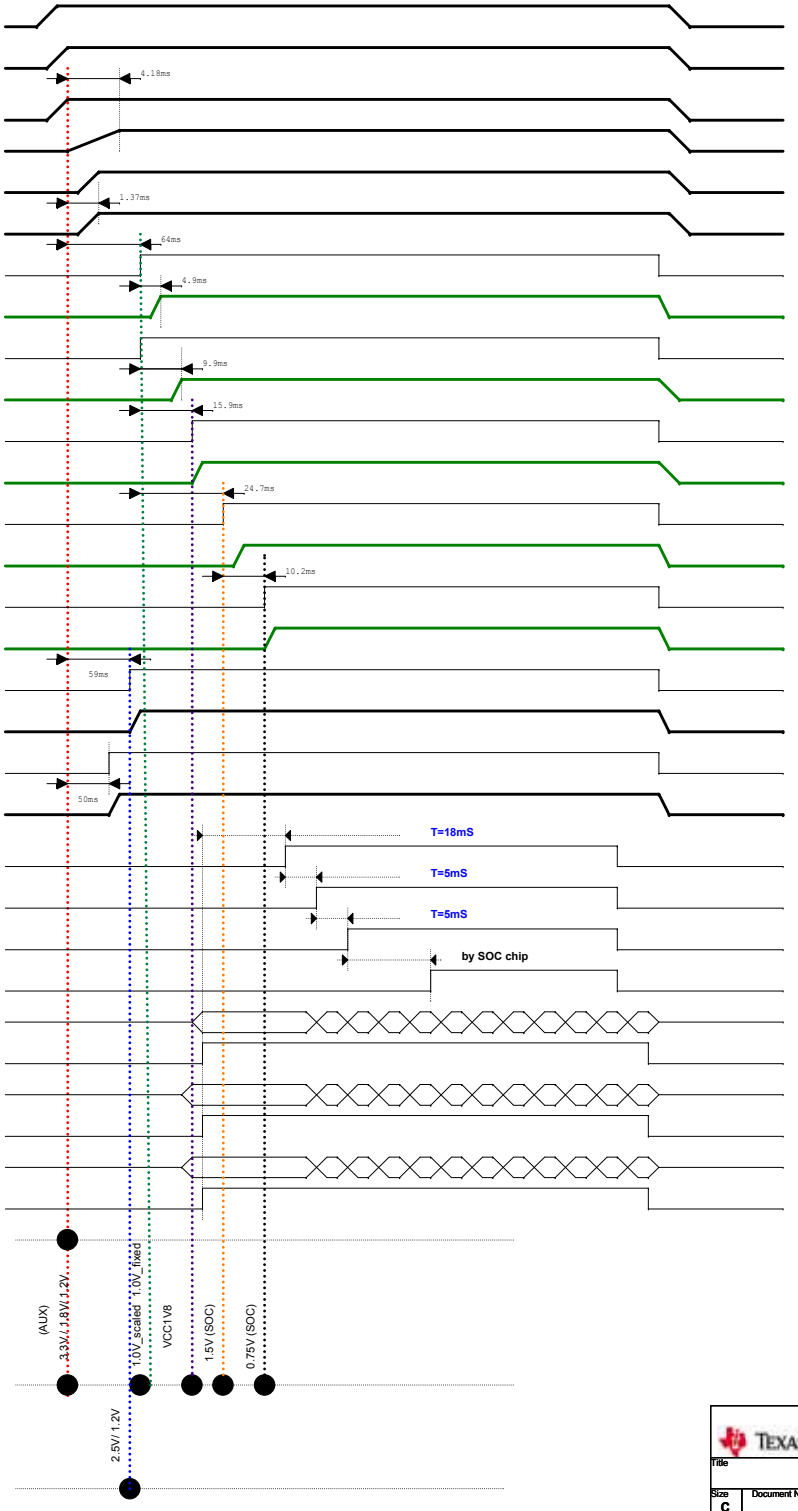
Power Sequence

		VCC3V3_MP_AMC
S0	MMC	VCC3V3_MP
S1		VCC12
S2	Other FT2232H XC3S200AN	VCC3V3_AUX
S3	XC3S200AN	VCC1V8_AUX
S4	88E1111 XC3S200AN	VCC1V2
S5		PMBUS & UCD9222_ENA1
S6	SOC TMS320TCI6614	CVDD
S7		PMBUS & UCD9222_ENA2
S8	SOC TMS320TCI6614	VCC1V0
S9		VCC1V8_EN
S10	SOC TMS320TCI6614	VCC1V8
S11		VCC1V5_EN
S12	DDR3 SOC TMS320TCI6614	DDR3 SDRAM VCC1V5
S13		VCC0V75_EN
S14	DDR3 SOC TMS320TCI6614	DDR3 Vref VCC0V75
S15		VCC2V5_EN
S16	88E1111	VCC2V5
S17		VCC5_EN
S18	XDS560V2 Mazzenine Board	VCC5



Ther is no specific power-up nor power-down sequence.

XILINX_XC3S200AN
1.2V_AUX (VCCINT)
1.8V_AUX (VCC1V8_AUX)
3.3V_AUX (VCCAUX)

XILINX_XC3S200AN

When power on: VCC_1V0 scaled → VCC_1V0 Fixed → VCC1V8 → 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref)

When power down: 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref) → VCC1V8 → VCC_1V0 Fixed → VCC_1V0 scaled

SOC TMS320TCI6614
VCC1V0 Scaled/(CVDD)
VCC1V0 Fixed/(CVDD1)
VCC1V8/ (DVDD18)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

SOC TMS320TCI6614

Ther is no specific power-up nor power-down sequence.

88E1111 (PHY)
2.5V
1.2V

88E1111

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Title	Power Sequence	
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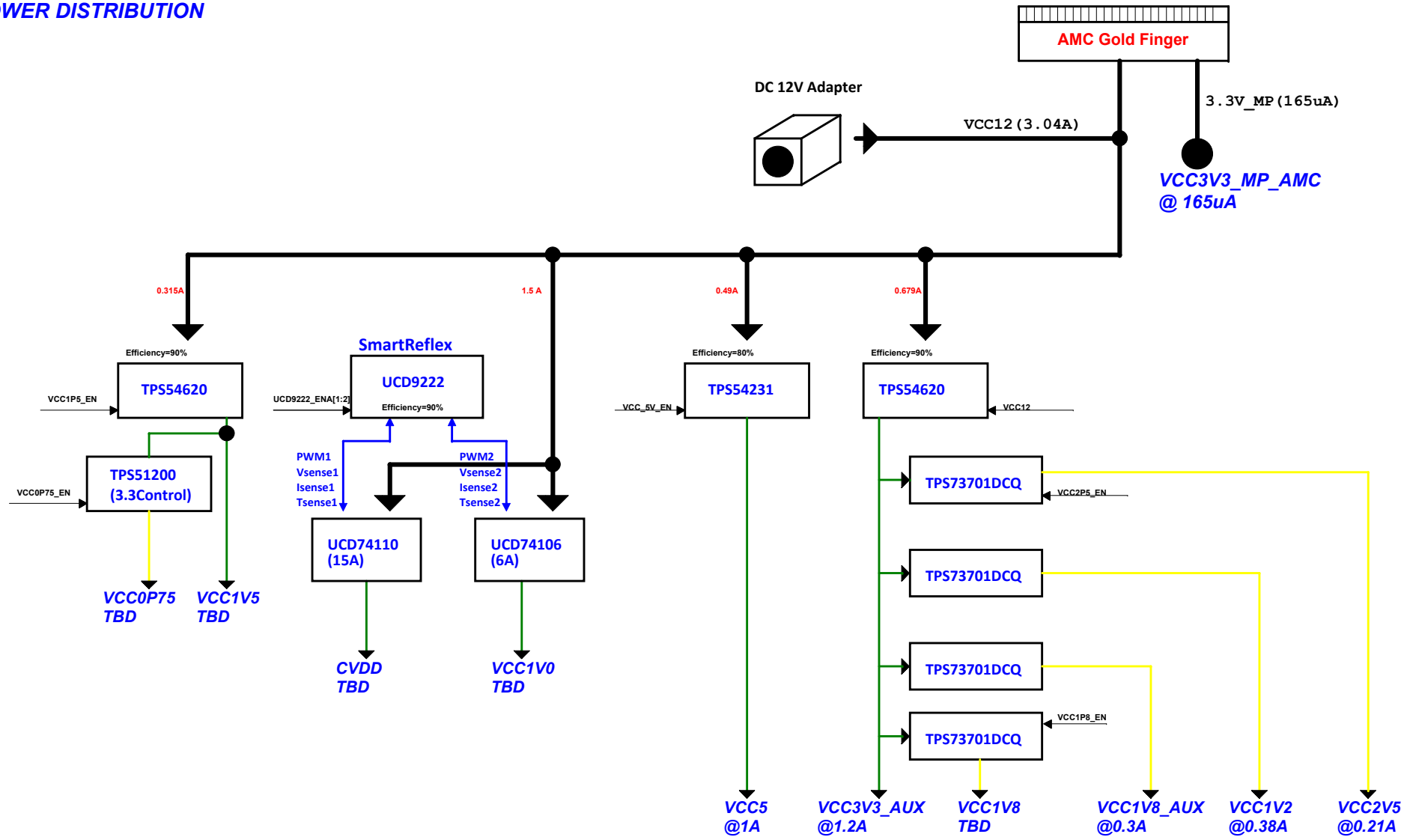
POWER CONSUMPTION

For Power Consumption please refer to TMS320TCI6614 Data Manual

http://www.ti.com/lit/ds/symlink/tms320tci6614.pdf

POWER DISTRIBUTION



DDR3
1.5V / 0.24A (VDD)*5 Total:1.2A
0.75V / 0.25A (Vref)

Quad Core SOC
TI_TMS320TCI6614
VCC1V0 / 9.75A Scaled/(CVDD)
VCC1V0 / 4.52A Fixed/(CVDD1)
VCC1V8 / 0.15A (DVDD18)
1.5V / 0.47A (DDR3_IO)
0.75V/(DDR3_Vref)

RS232
3.3V

XDS560V2
Mazzenine Board
5.0V / 1A
3.3V / 0.3A

EEPROM
3.3V

MicronNAND FLASH
1.8V / 0.02A

NOR FLASH
Standyby mode 1.8V/80uA

XILINX_XC3S200AN
1.2V_AUX/ 0.125A (VCCINT)
3.3V_AUX/ 0.024A (VCCAUX)

88E1111 (PHY)
2.5V / 0.21A
1.2V / 0.25A

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DSPM-8303E

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Title: POWER DISTRIBUTION		
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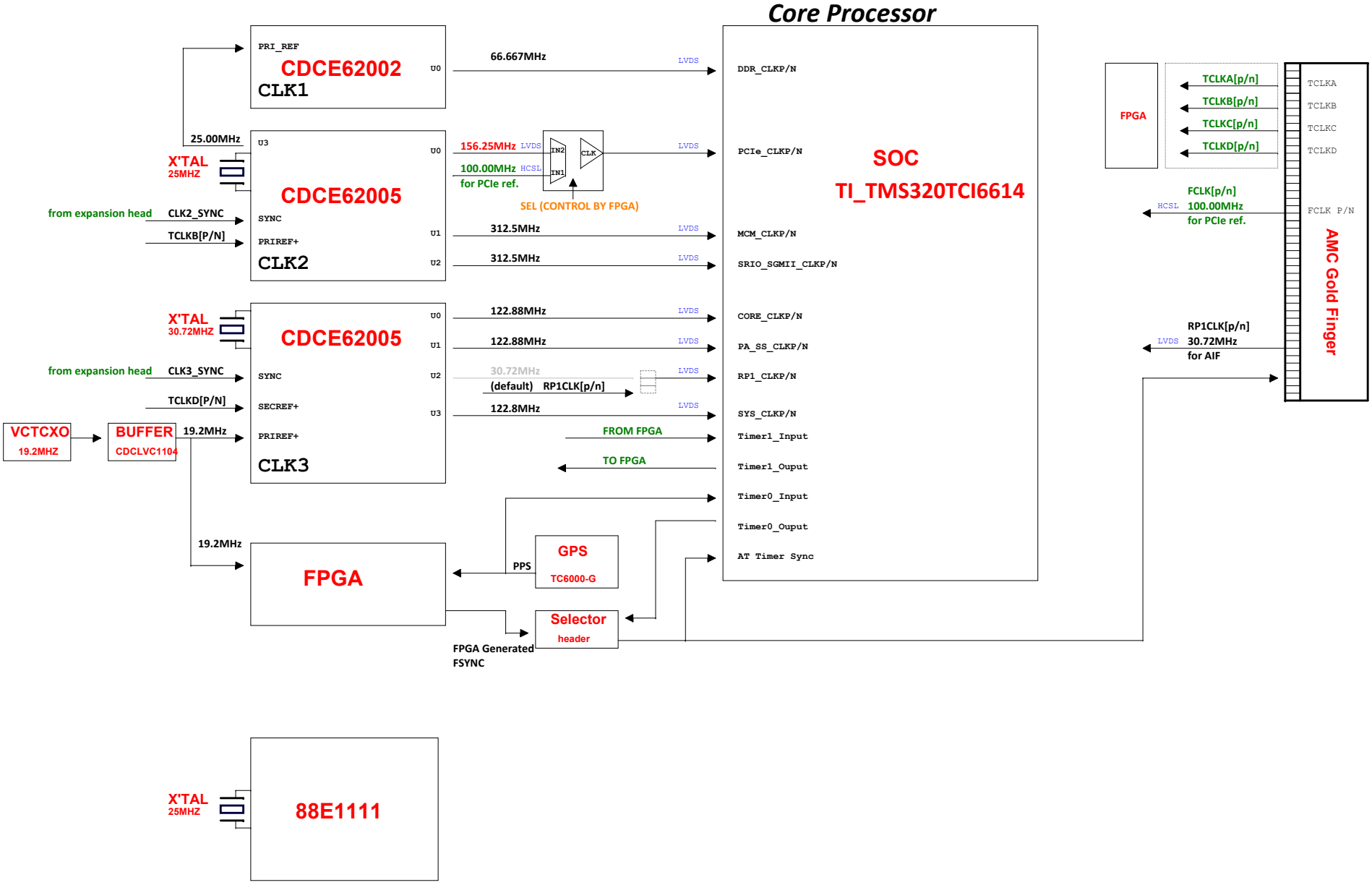
CLOCK DIAGRAM



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Title: CLOCK DIAGRAM		
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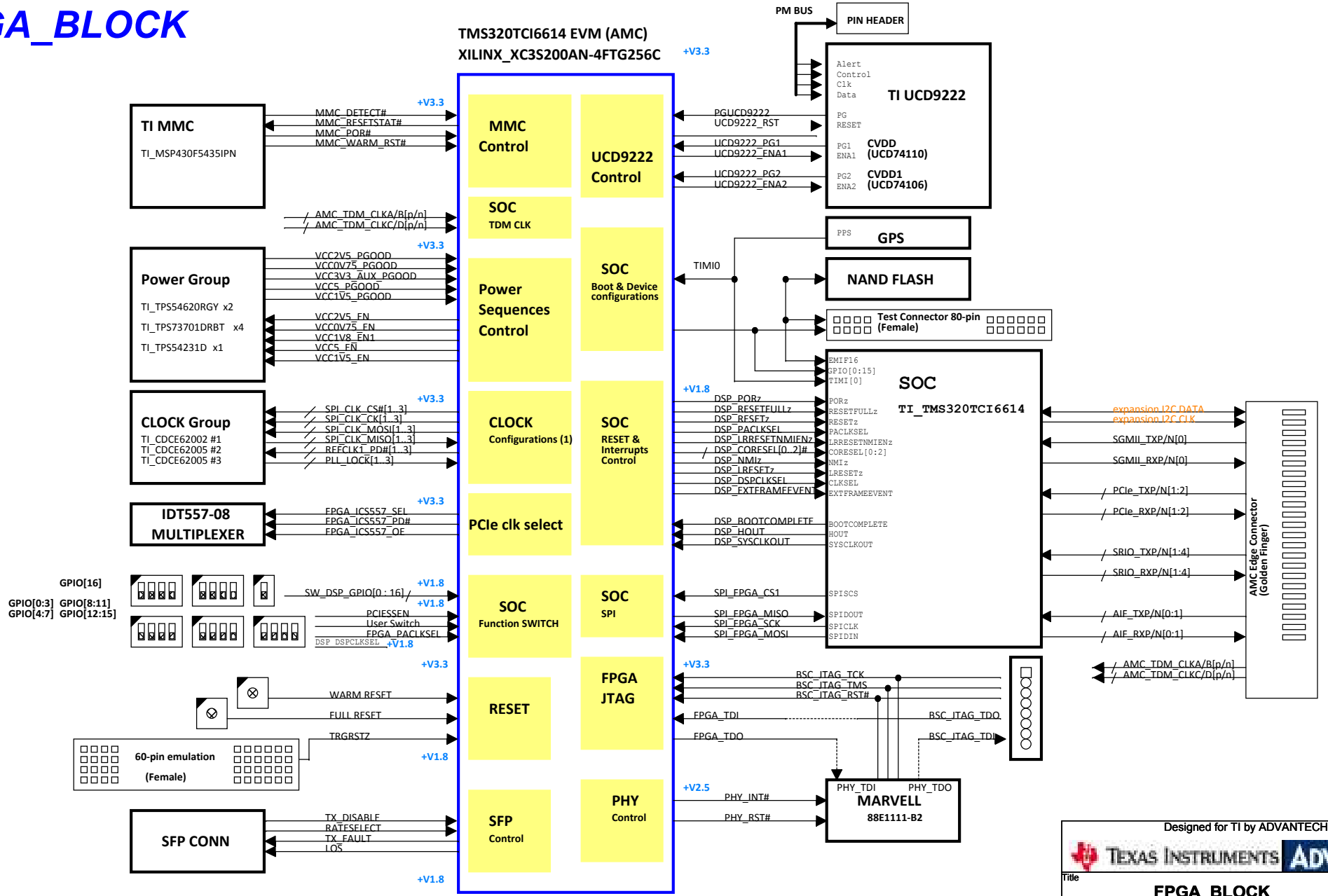
FPGA_BLOCK



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Title: FPGA_BLOCK

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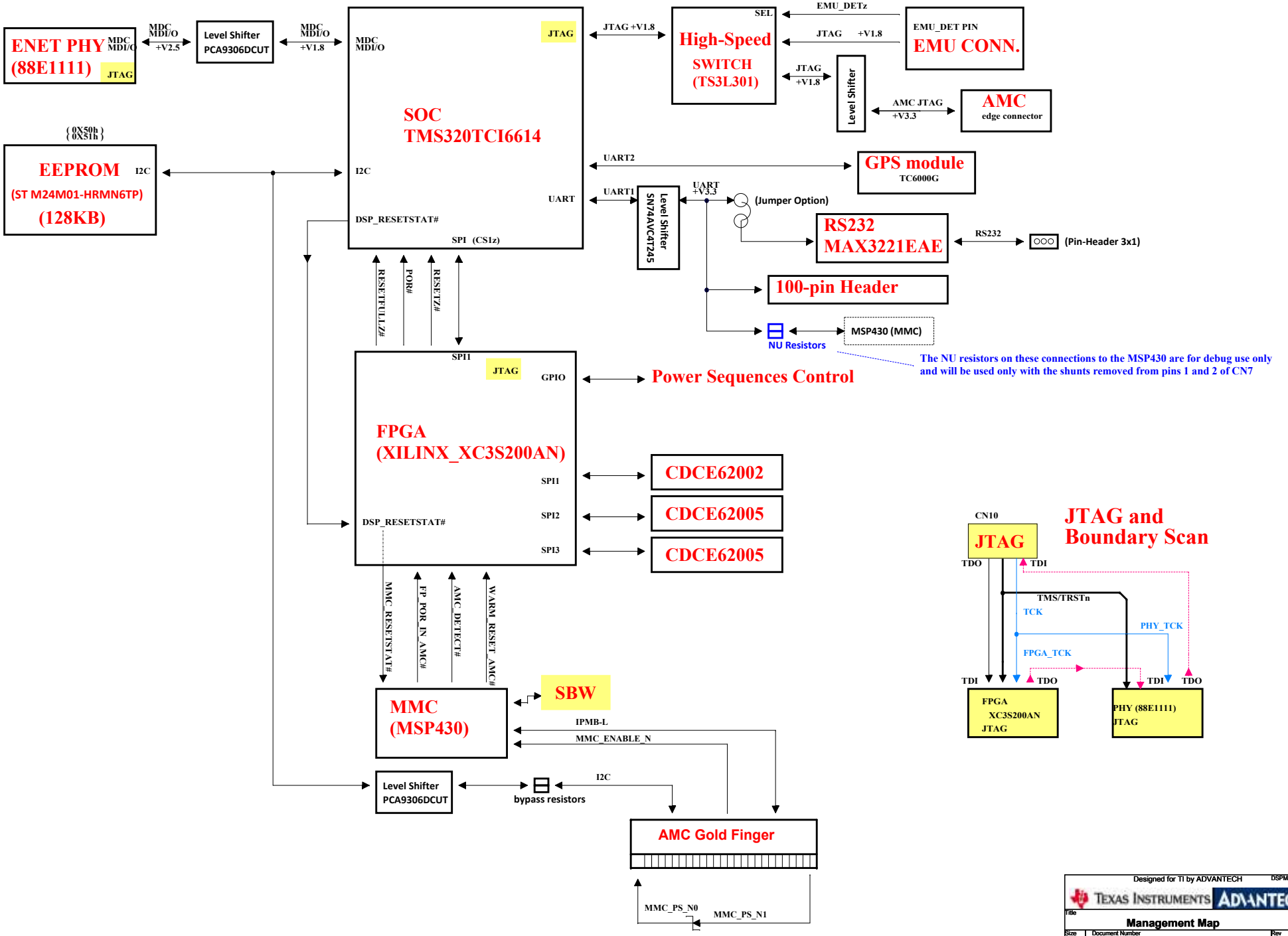
Management Map



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TEXAS INSTRUMENTS ADVANTECH

Title: Management Map		
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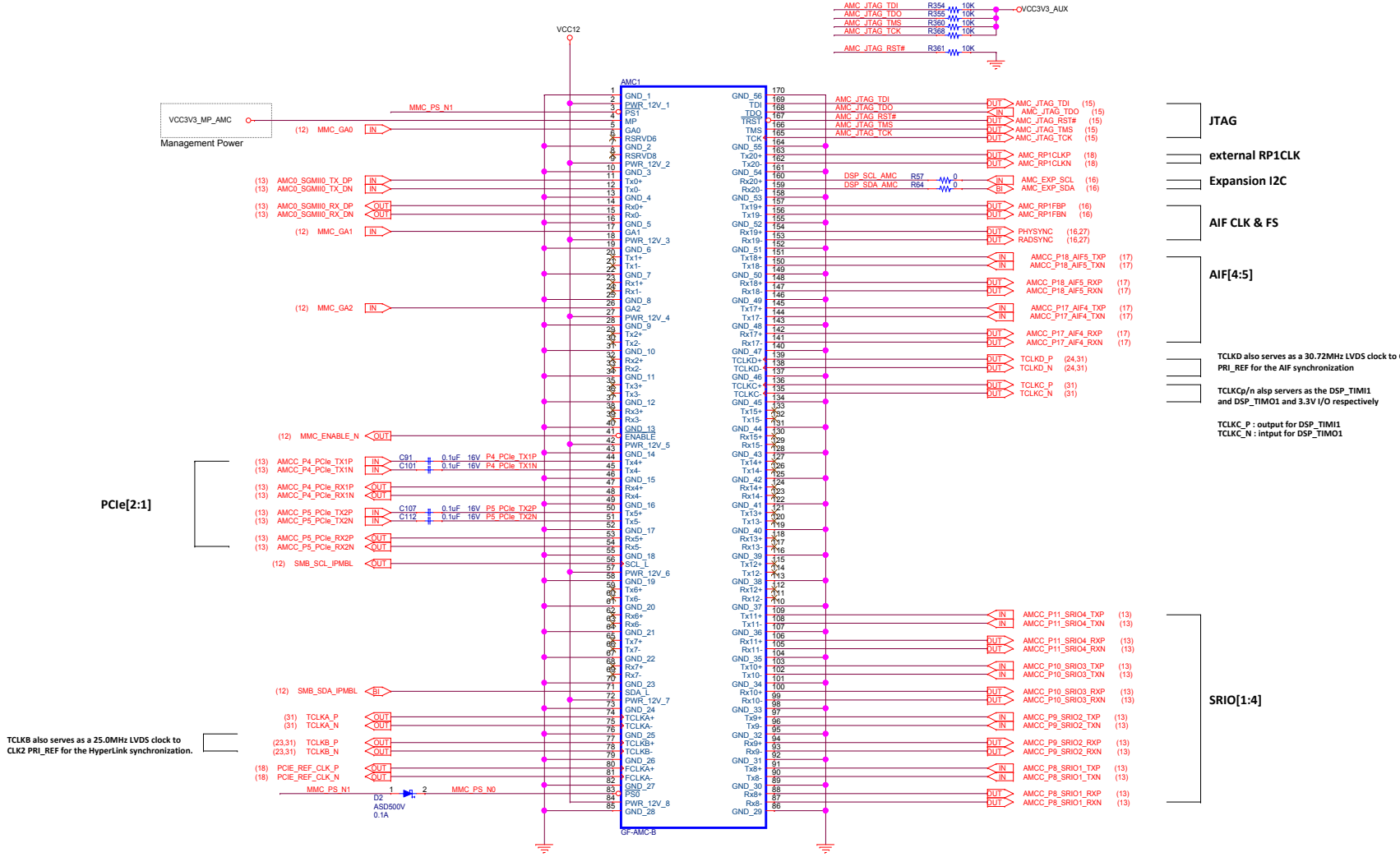
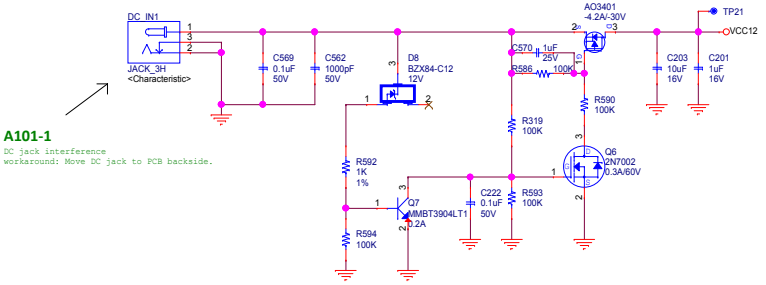
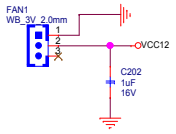


OVP: ~12.7V+0.6V = ~13.3V



DC FAN Connet for SOC



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Title: AMC GF		
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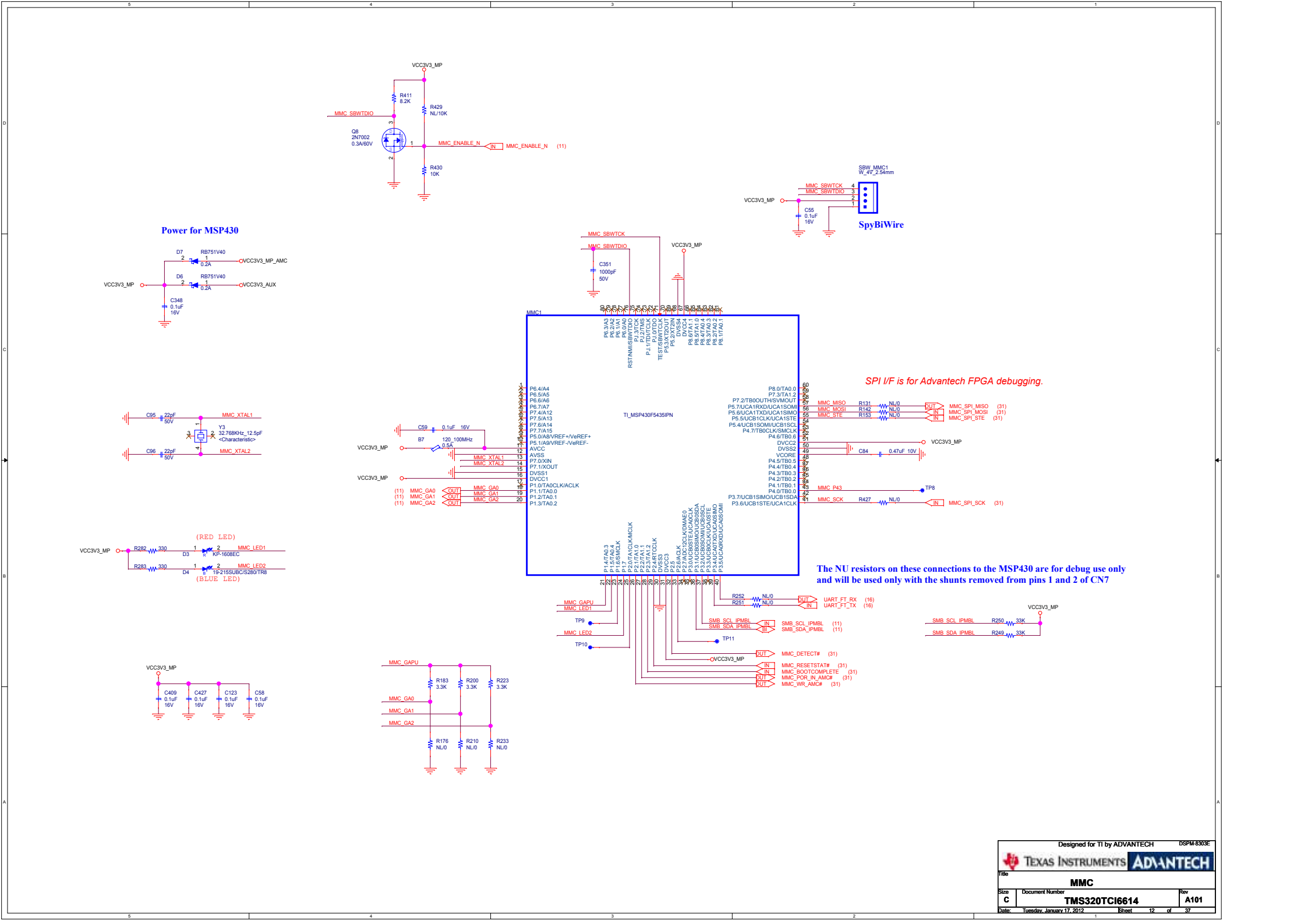
Power for MSP430
SpyBiWire
SPI I/F is for Advantech FPGA debugging.
The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7
TI_MSP430F5435IPN
MMC1
(RED LED)
(BLUE LED)
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DSPM-8303E
Title
MMC
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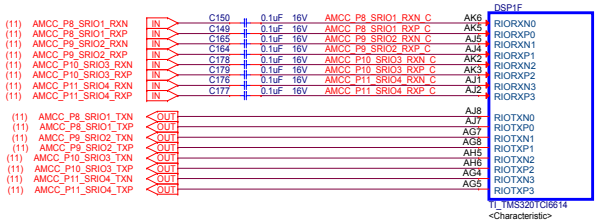
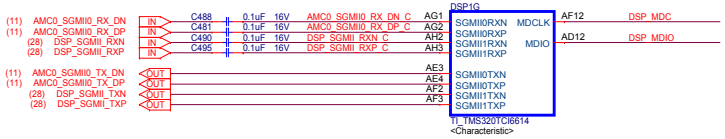
SRIO

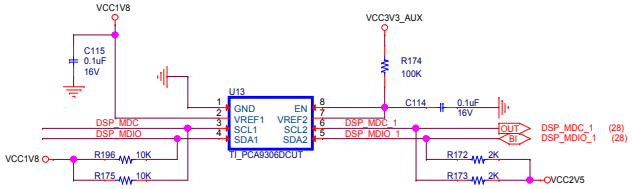


Caution!

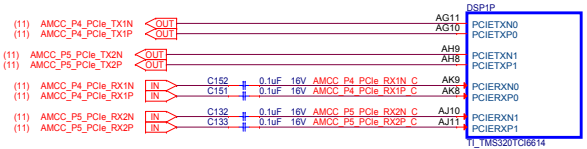
"Place ALL SERDES DC-blocking caps on top layer adjacent to the SOC's RX pins so that there are no additional vias"

SGMII

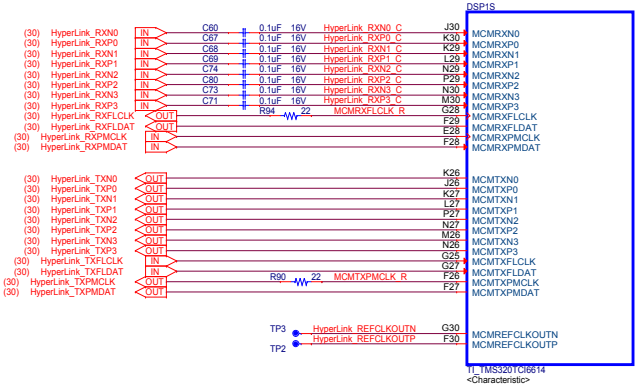




PCIE



HyperLink



"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"

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Title: SOC_SERDES_PORTS		
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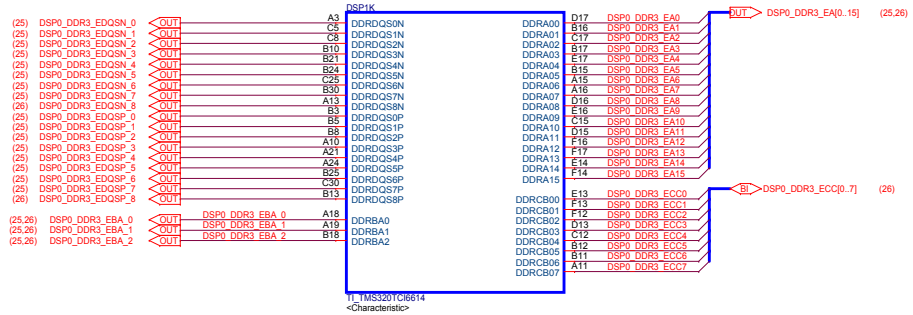

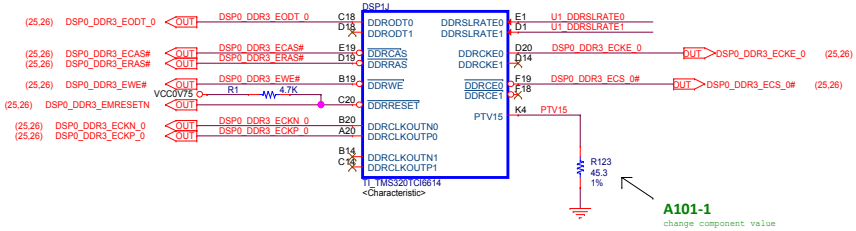

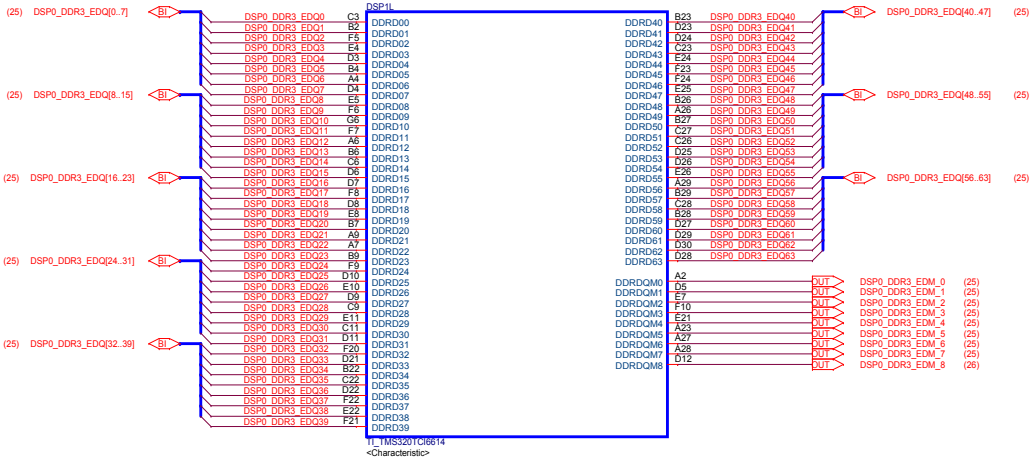

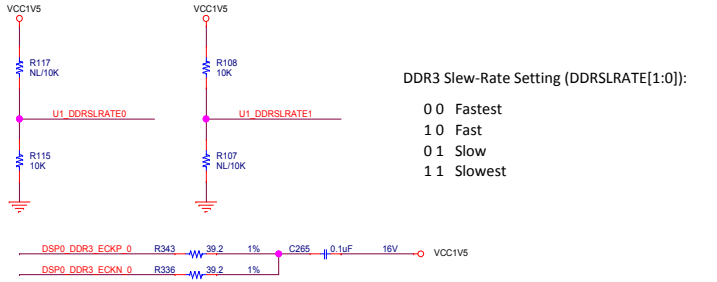

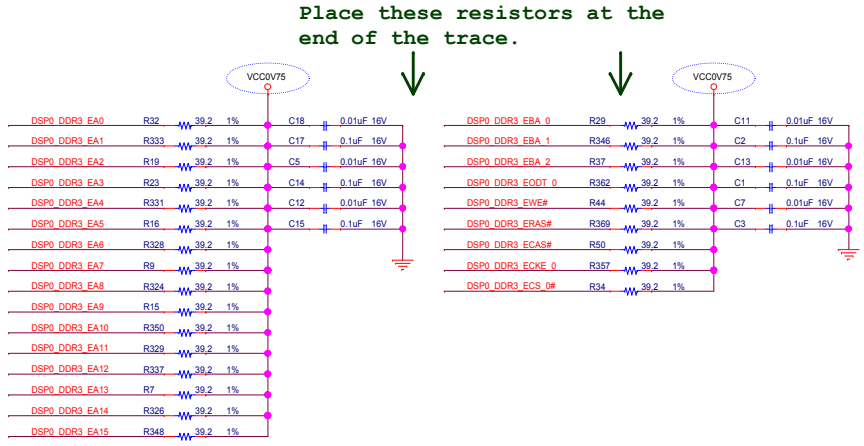

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Title	SOC_DDR3
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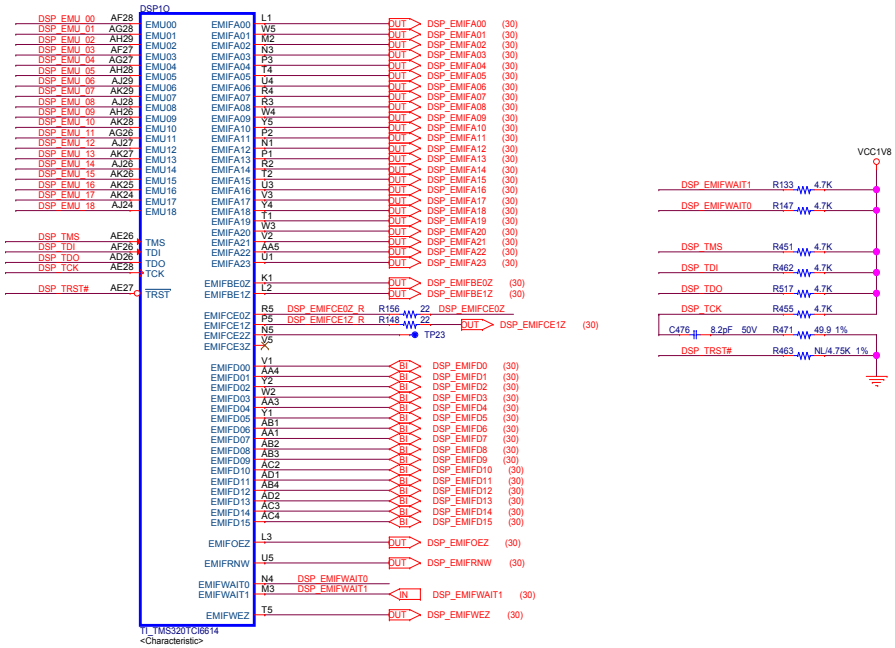
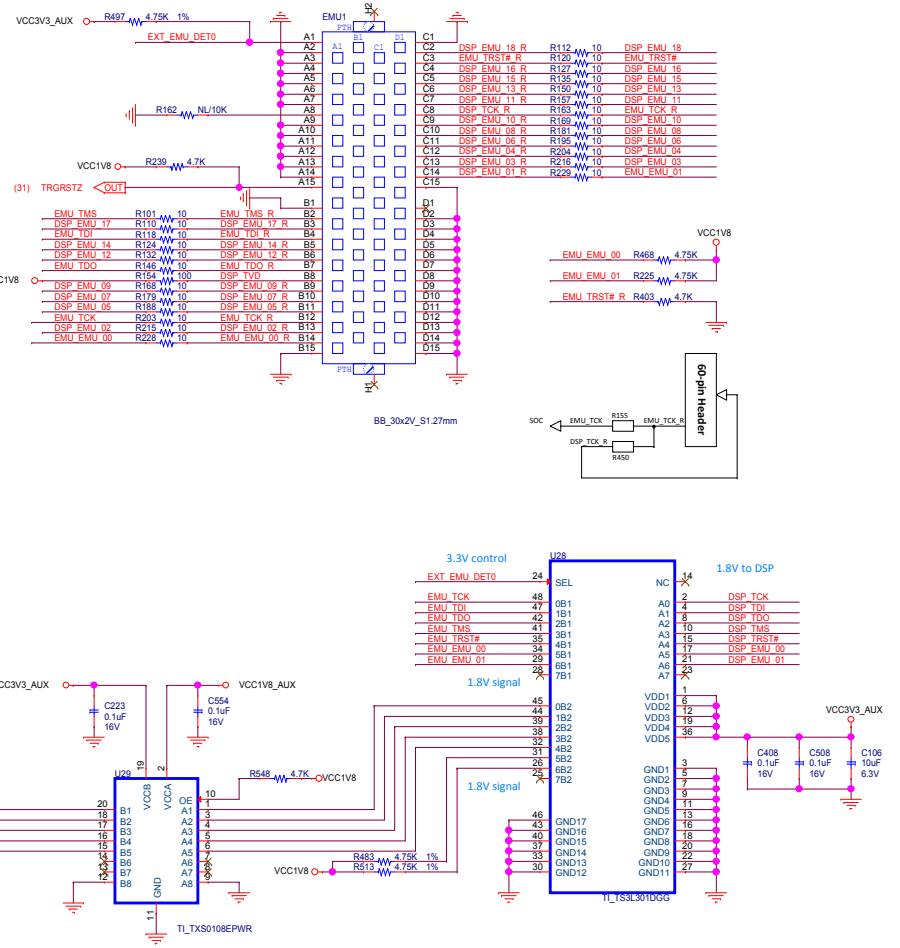
SOC EMIF & EMU & JTAG

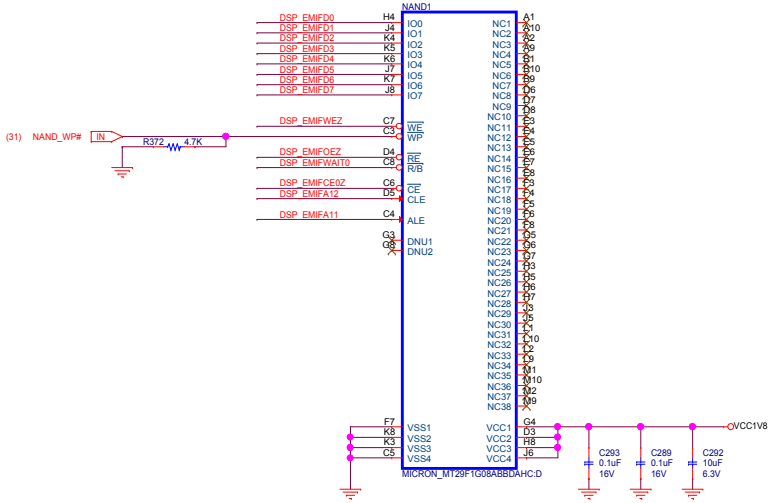


EMU CONN.

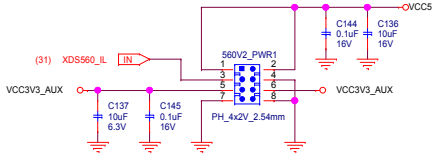


Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation

NAND FLASH



Power Supply for Daughter Board



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DSPM-8303E

Title: SOC_JTAG_EMU_AIF

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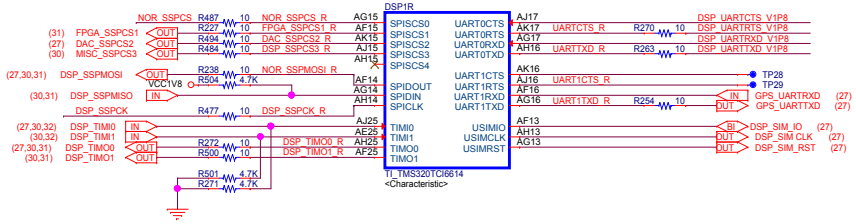
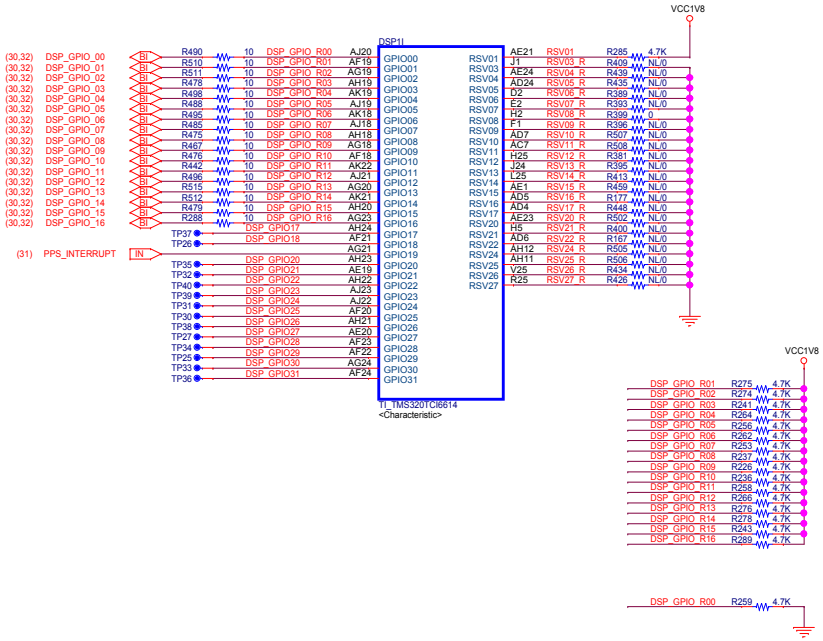
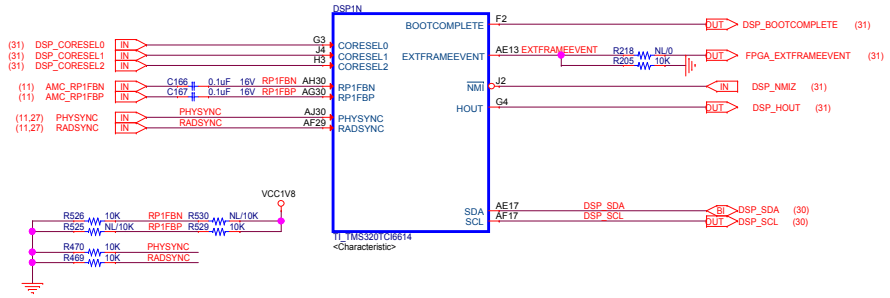
I2C, TIMER0,1, SPI, UART



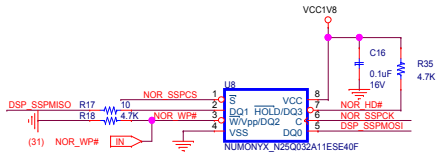
GPIO & RSV



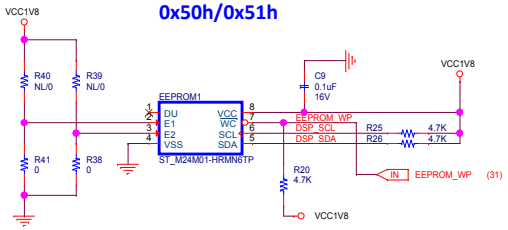
Core Control

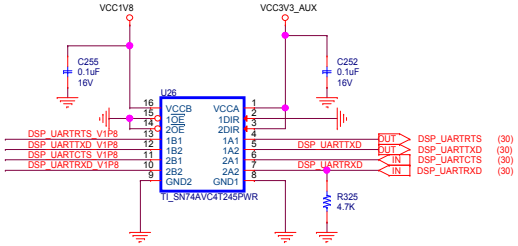


4M SPI NOR Flash

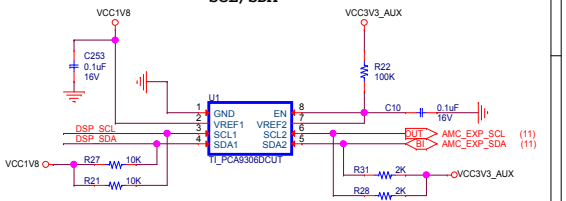


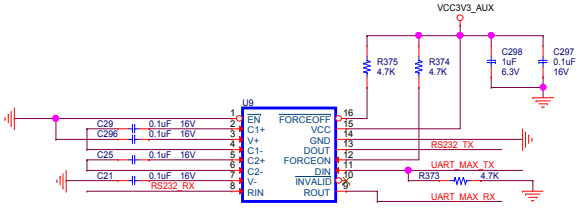
1M-bit I2C EEPROM 0x50h/0x51h

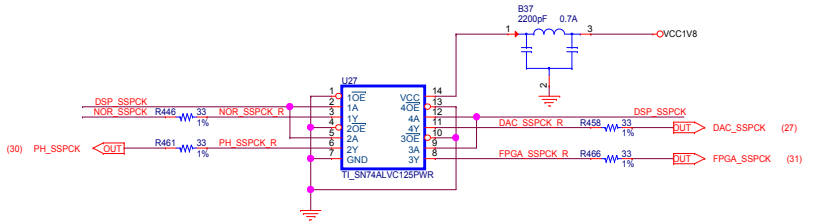




SCL/SDA

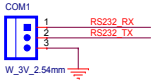




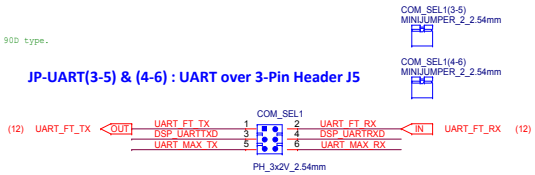


A101-1

UART interference with xds560v2,
workaround: Move UART connector to PCB backside and adopt 90D type.



JP-UART(3-5) & (4-6) : UART over 3-Pin Header J5



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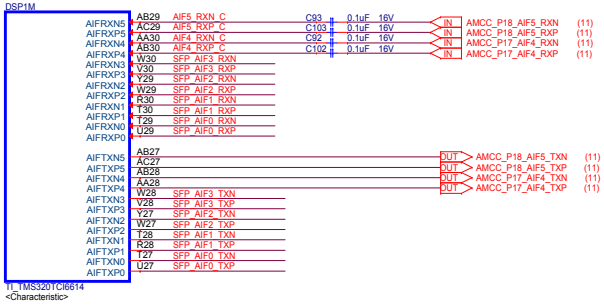
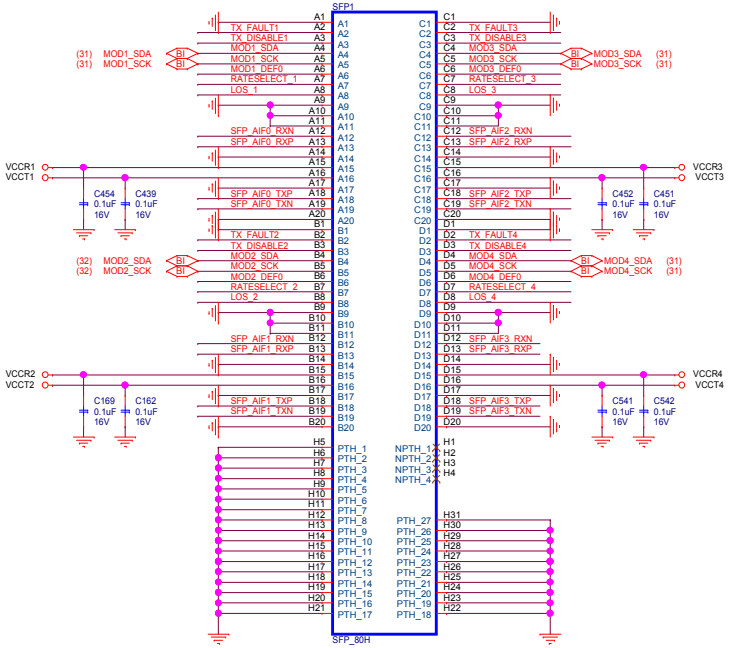
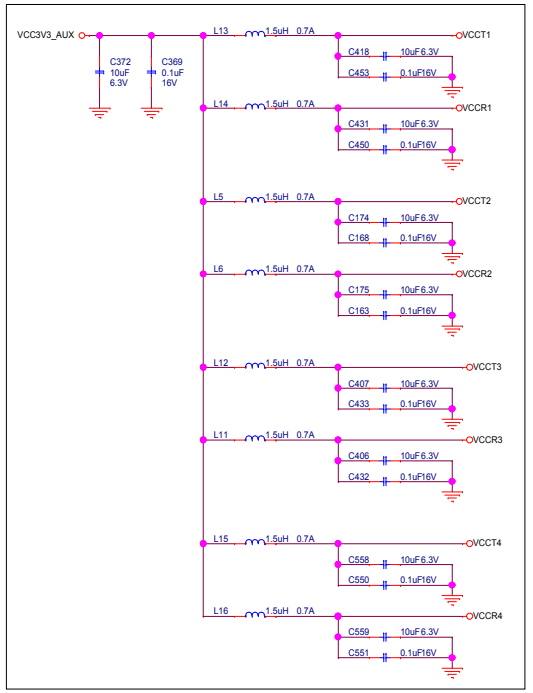
SOC AIF

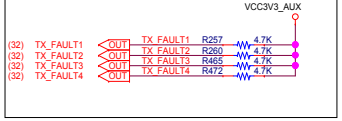


SFP CONN

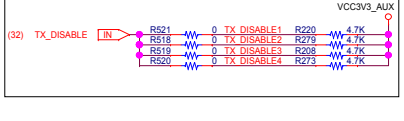


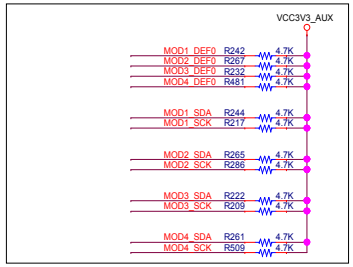


Strip pin	TX_FAULT
High(2.0V - VCCT)	Output indicates a laser fault of same kind
Low(< 0.8V)	Normal Operation



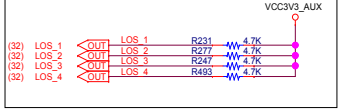
Strip pin	TX_DISABLE
High(2.0V - 3.465V)	Transmitter off
Low (< 0.8V)	Transmitter on



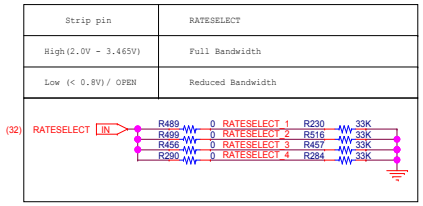


NOTE :
MOD_DEF0 is grounded by the module
to indicate that the module is present

Strip pin	LOS
High(2.0V - VCCT)	thisoutput indicates the received optical power is below the worst-case receiver sensitivity (asdefined by the standard in use)
Low (< 0.8V)	Normal Operation



Strip pin	RATESELECT
High(2.0V - 3.465V)	Full Bandwidth
Low (< 0.8V)/ OPEN	Reduced Bandwidth



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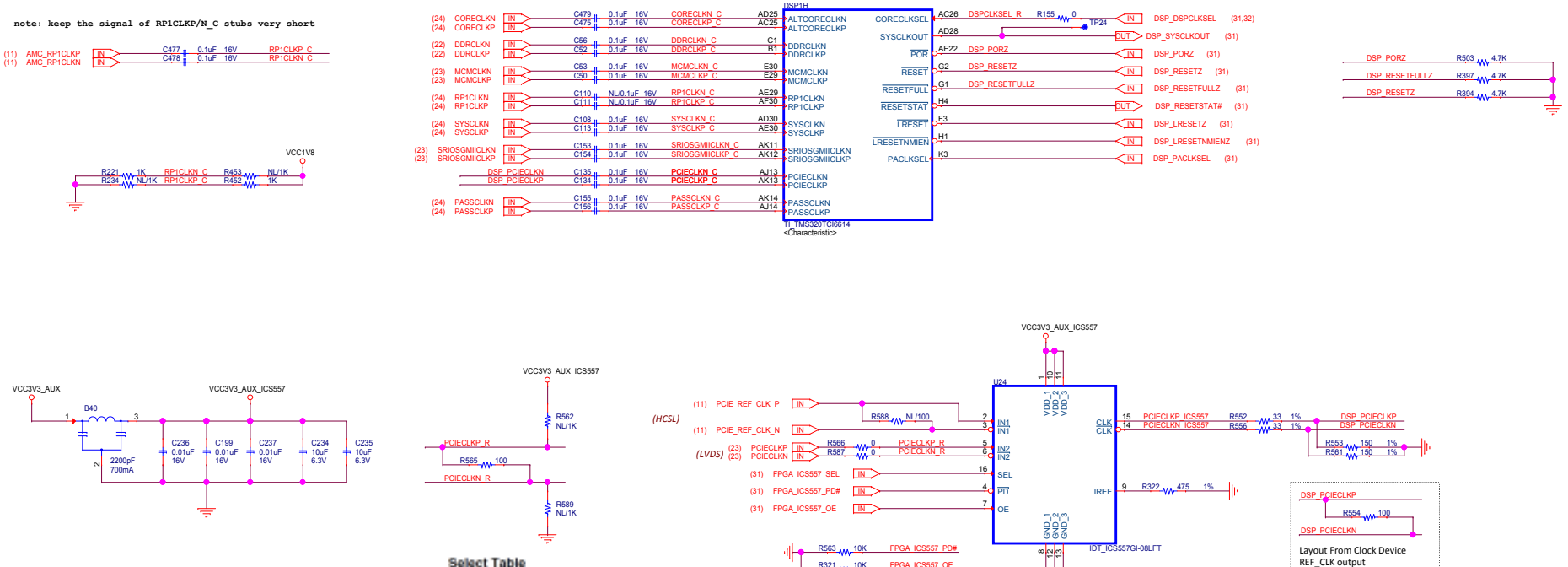
SOC CLOCK / RESET

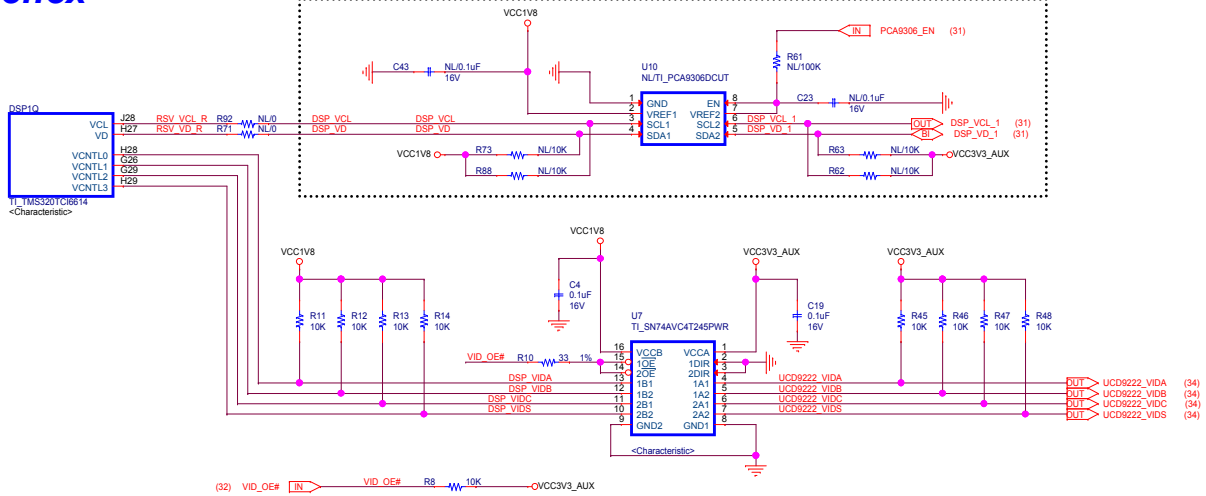
All blocking capacitors should be placed near SOC to keep connecting routes short and minimize vias

note: keep the signal of RP1CLKP/N_C stubs very short



Smart Reflex

DISABLE THIS FUNCTION



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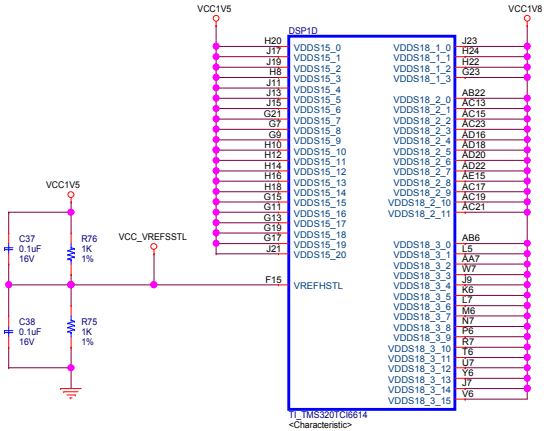
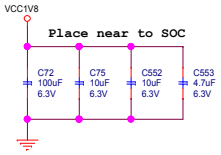
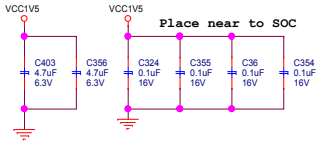
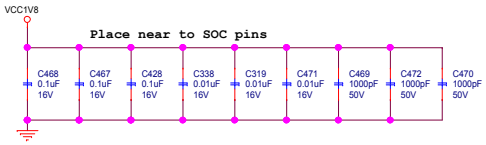
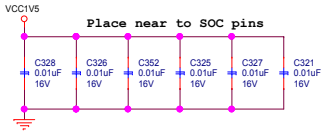
1.8V / 1.5V

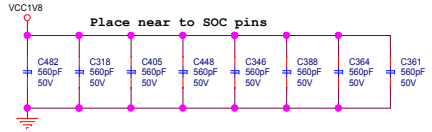


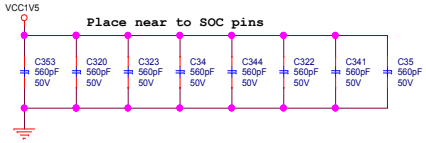


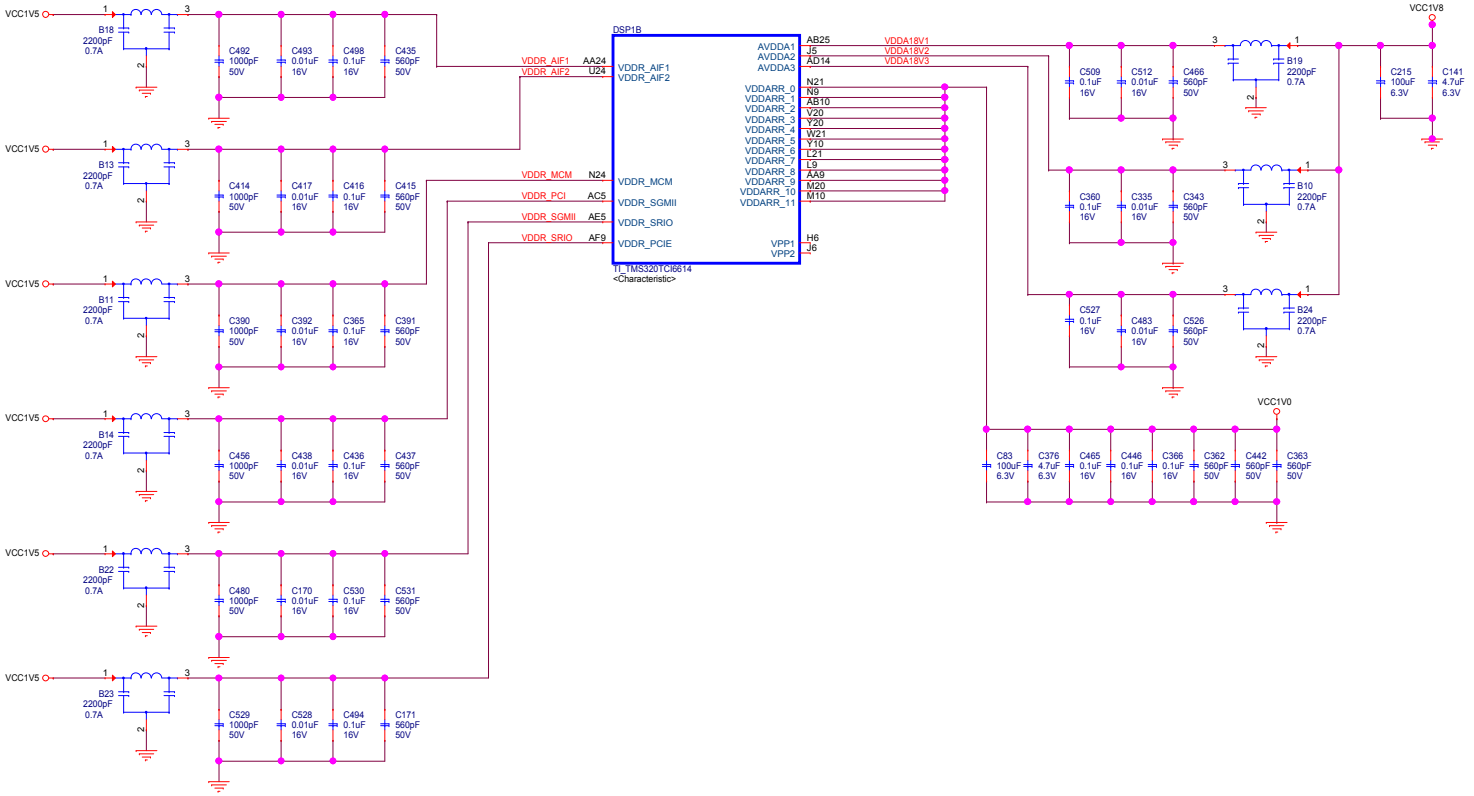












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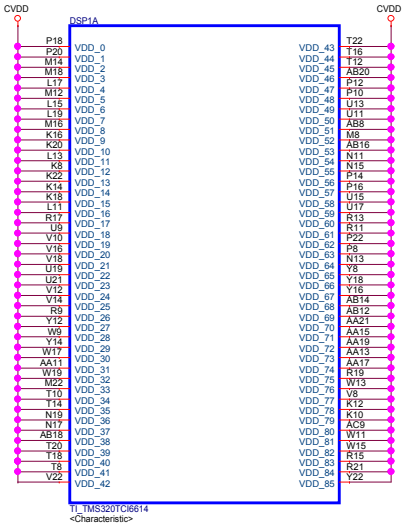
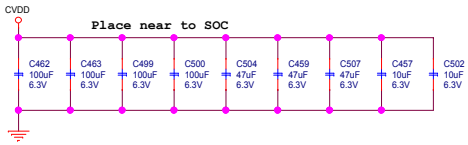
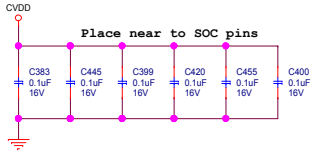
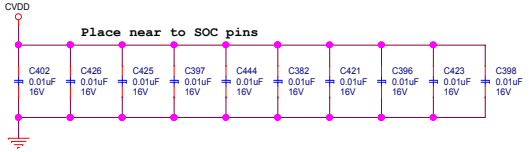
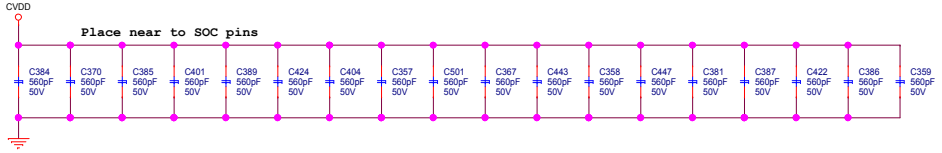
0.85V - 1.05V (CVDD) (Smart Reflex)



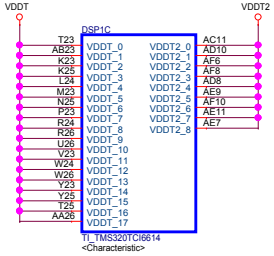


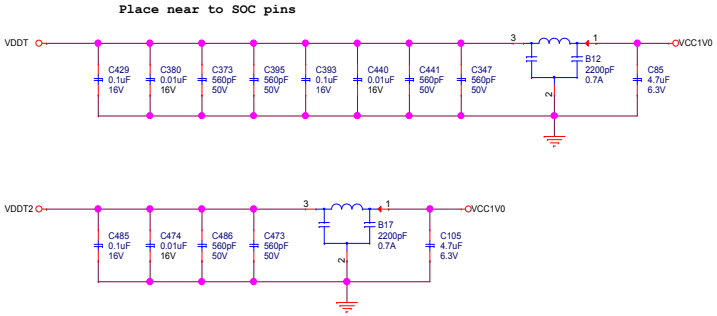






Fix_1.0V(VCC1P0)





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Title = SOC_POWERB

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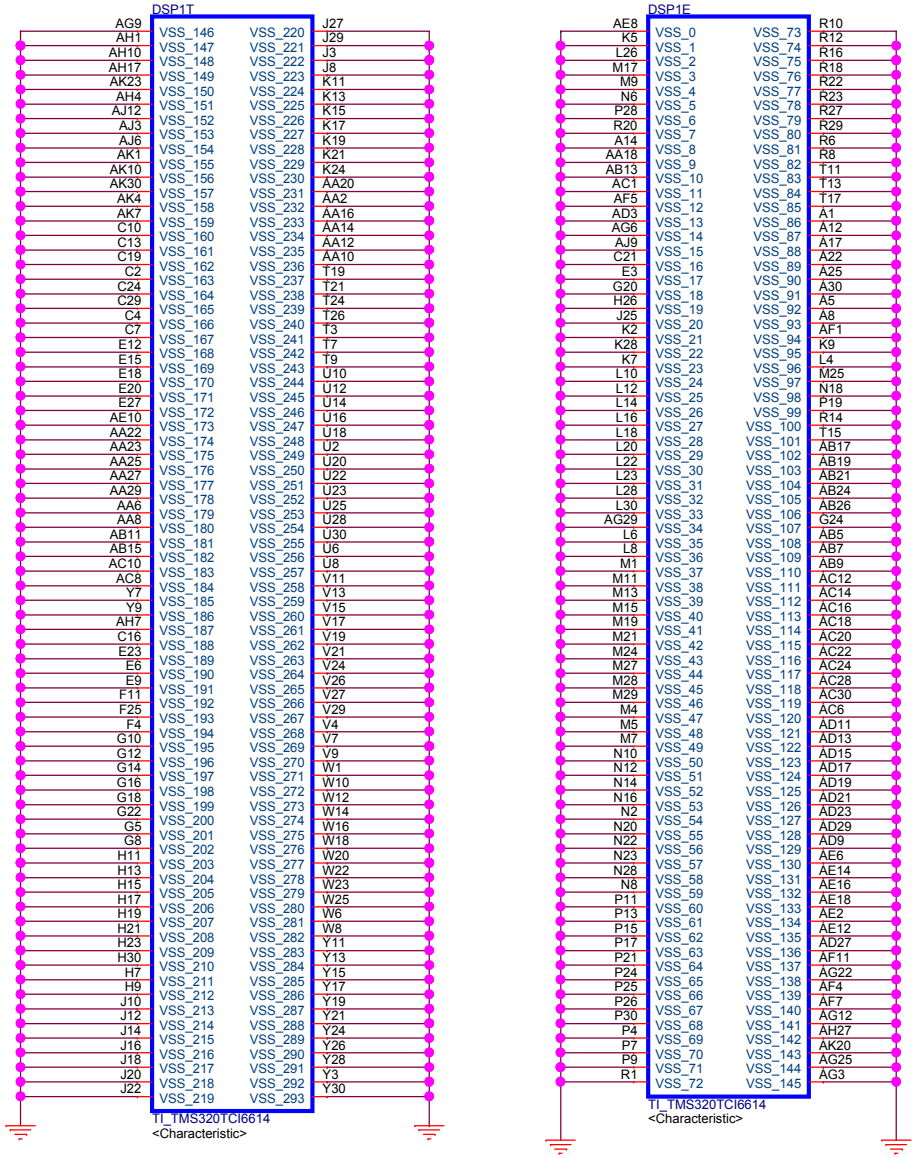

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Title: SOC_GND

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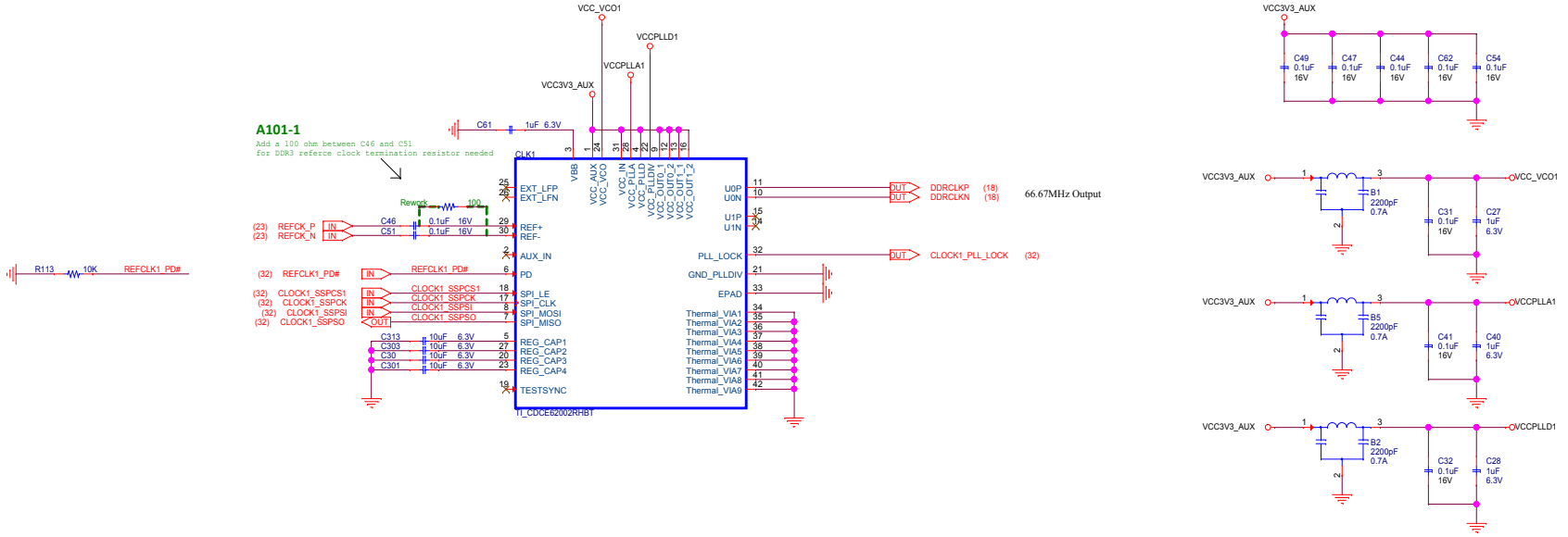
CLOCK GEN1 (DDR3)



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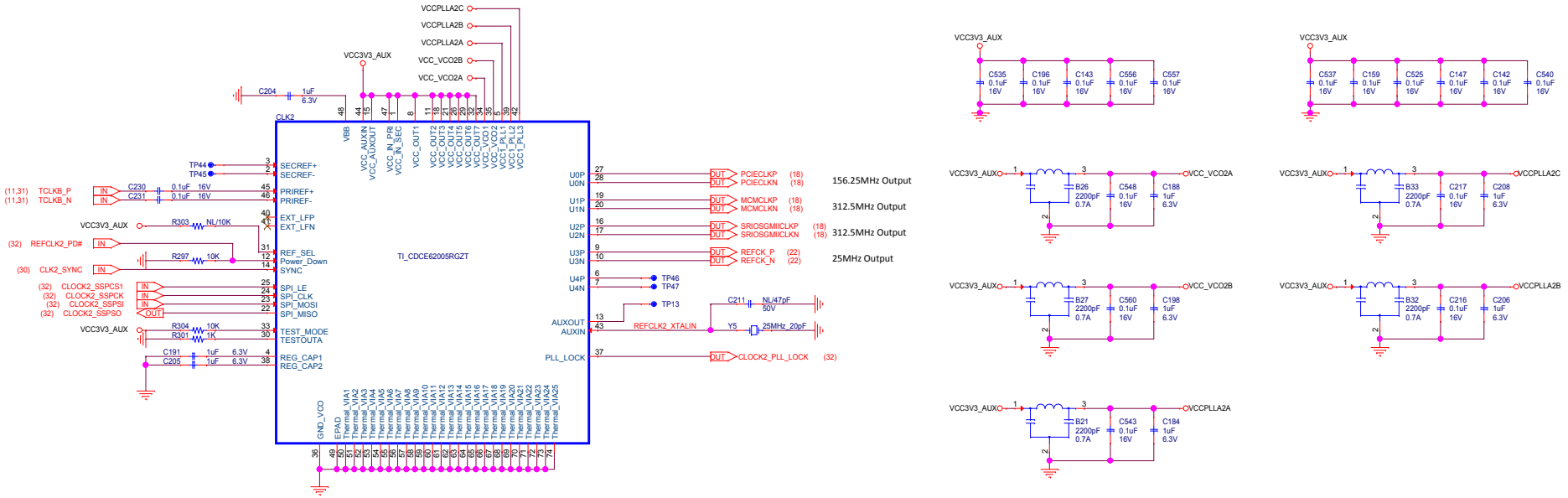
CLOCK GEN2



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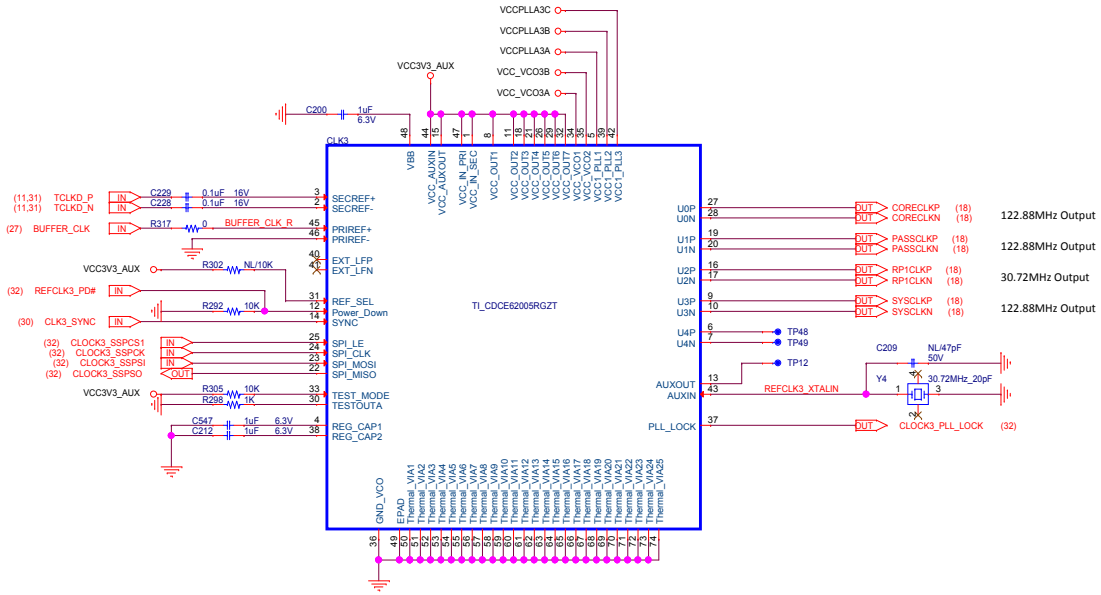
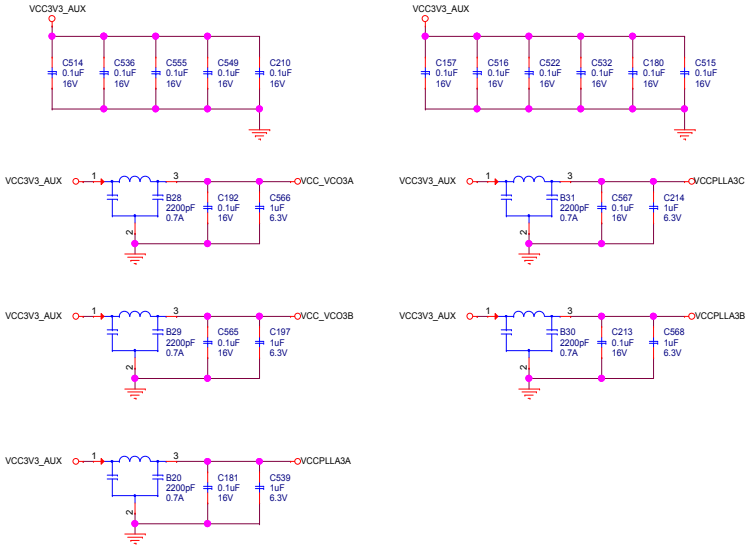
CLOCK GEN3





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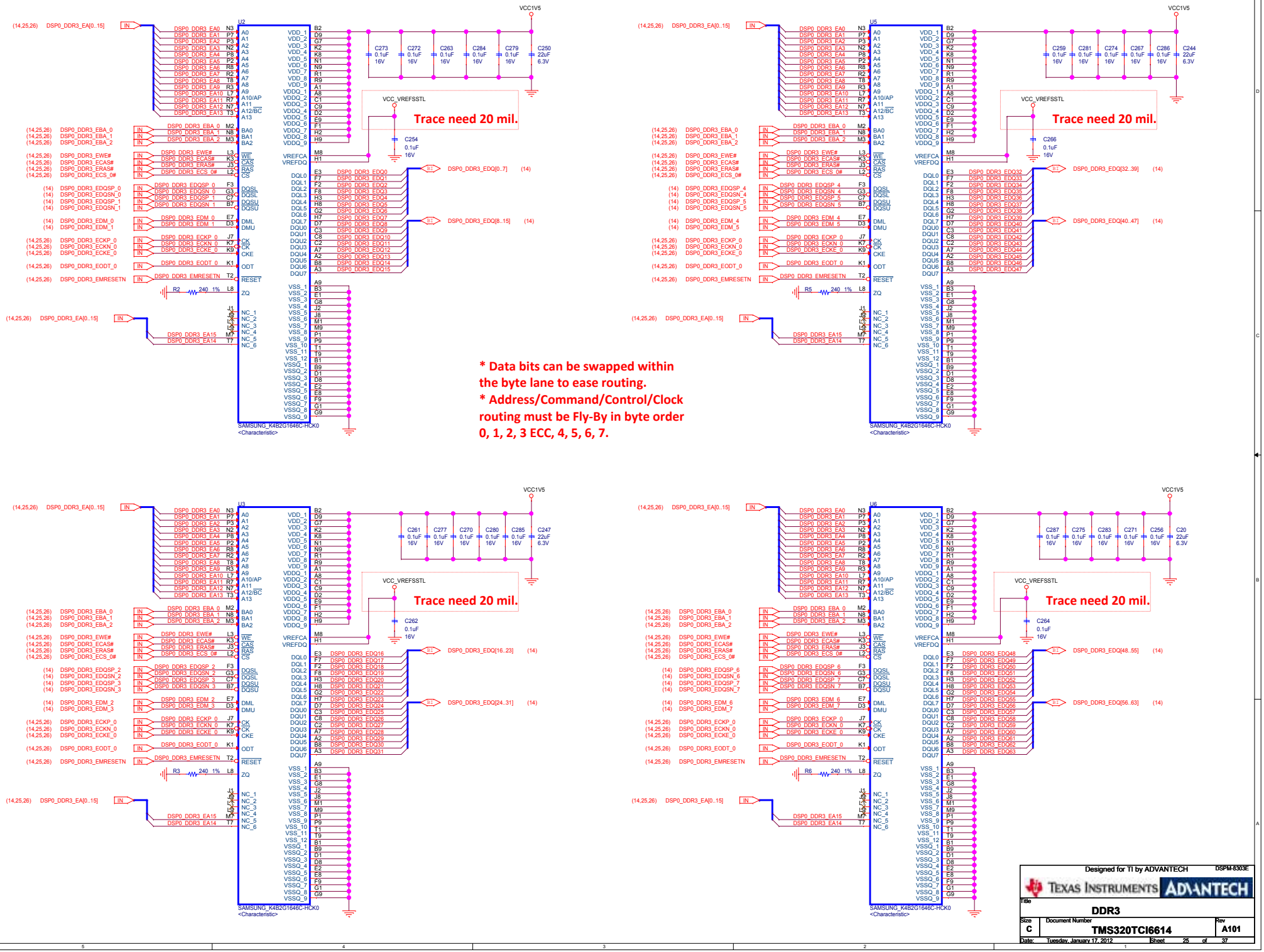
VCC1V5
U2
U5
U3
U6
VCC_VREFSSTL
Trace need 20 mil.
SAMSUNG_K4B2G1646C-HCK0
<Characteristic>
* Data bits can be swapped within the byte lane to ease routing.
* Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.
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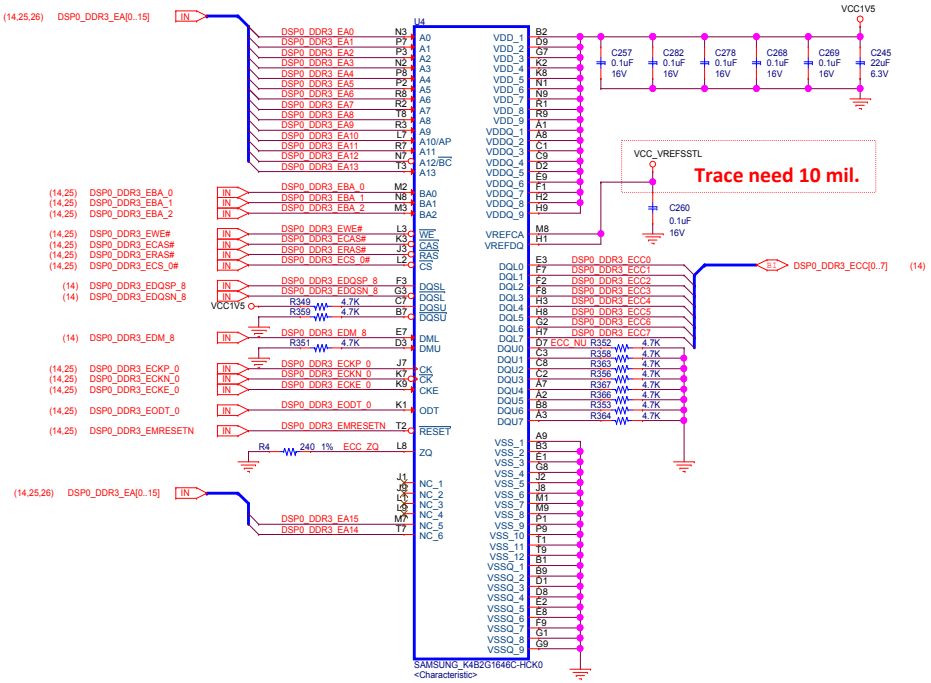
FOR ECC USE



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DDR3_ECC		
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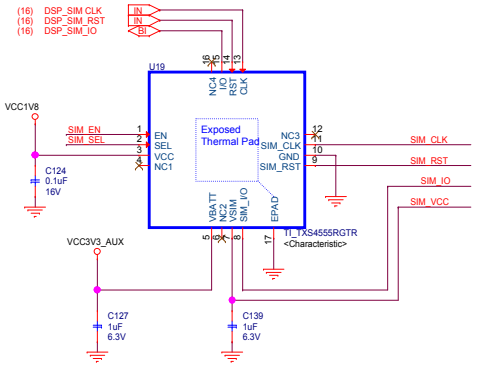
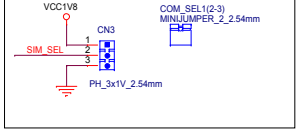
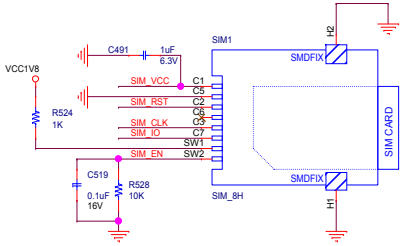
USIM

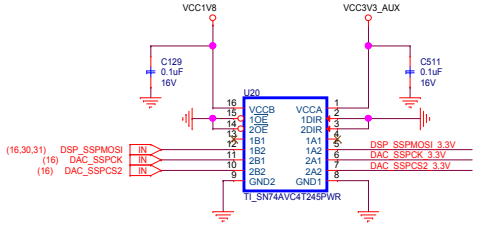


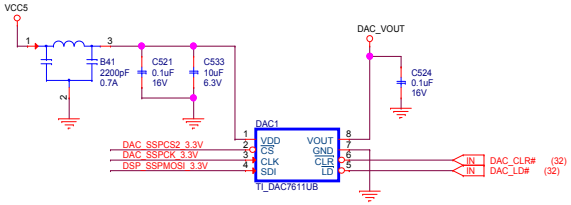
	High	Low (Default)
SIM_SEL	VCC_SIM Value = 2.95V	VCC_SIM Value = 1.8V

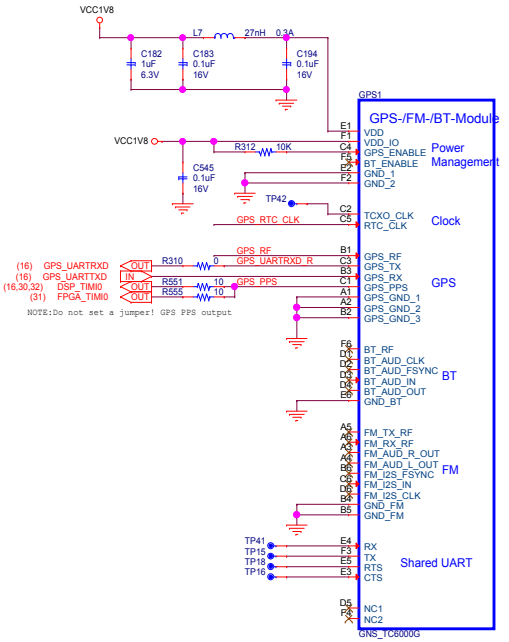


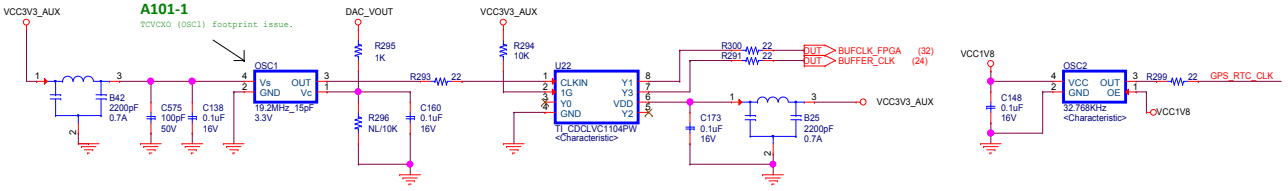


GPS

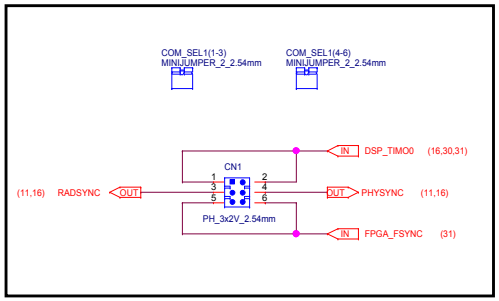




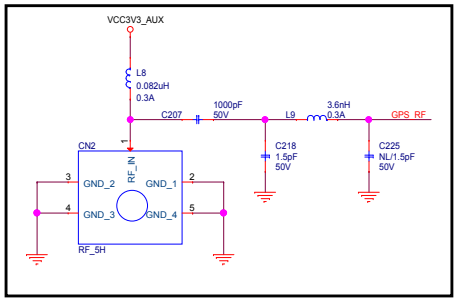




FOR PPS SELECT



FOR ANTENA CIRCUIR



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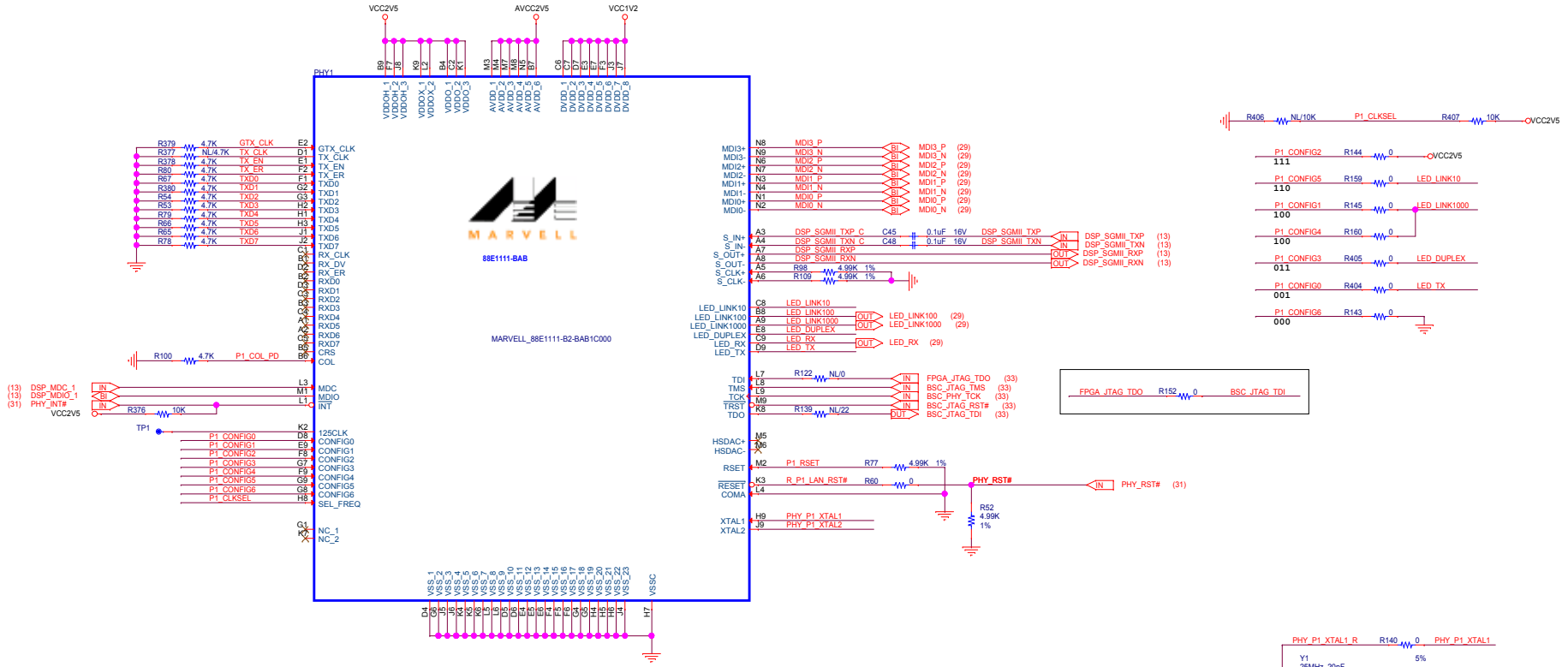

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

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TEXAS INSTRUMENTS ADVANTECH

Title: Gigabit Ethernet PHY

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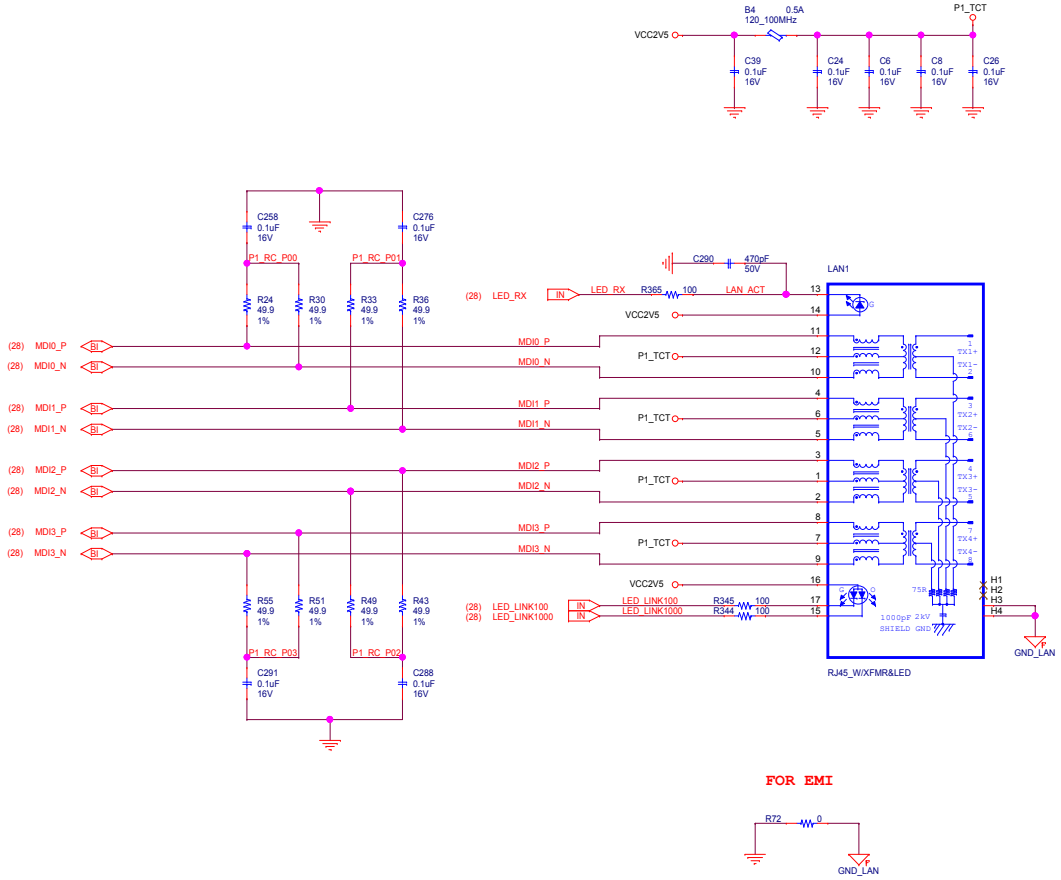
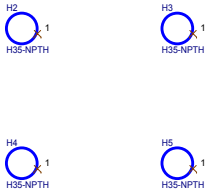
RJ-45

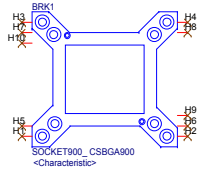


Heatsink Holes



AMC Hole

On board



(Bottom Side 3mm) Placed Capacitors

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Title: RJ45		
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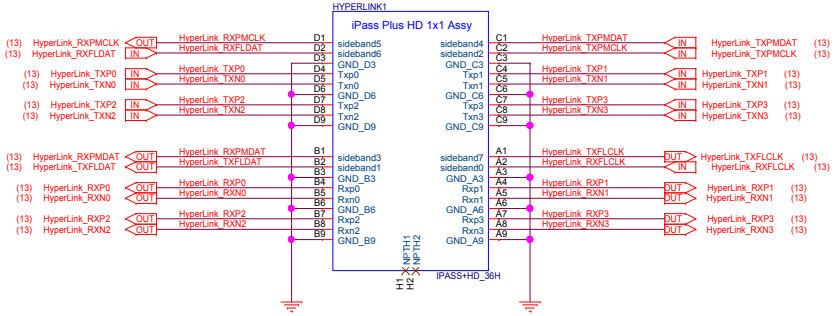
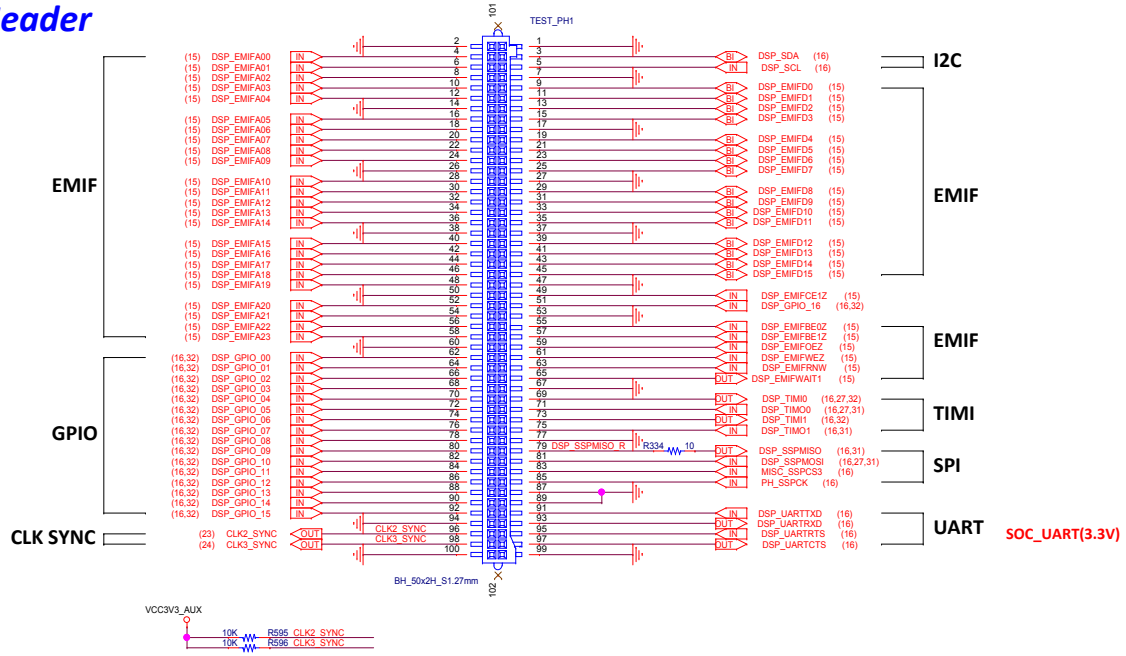
IPASS+HD for HyperLink Bus connection



100-pin Expansion Header

the interfaces on the 100-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS



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Title: Connectors for HyperLink & Debug

Size	Document Number	Rev
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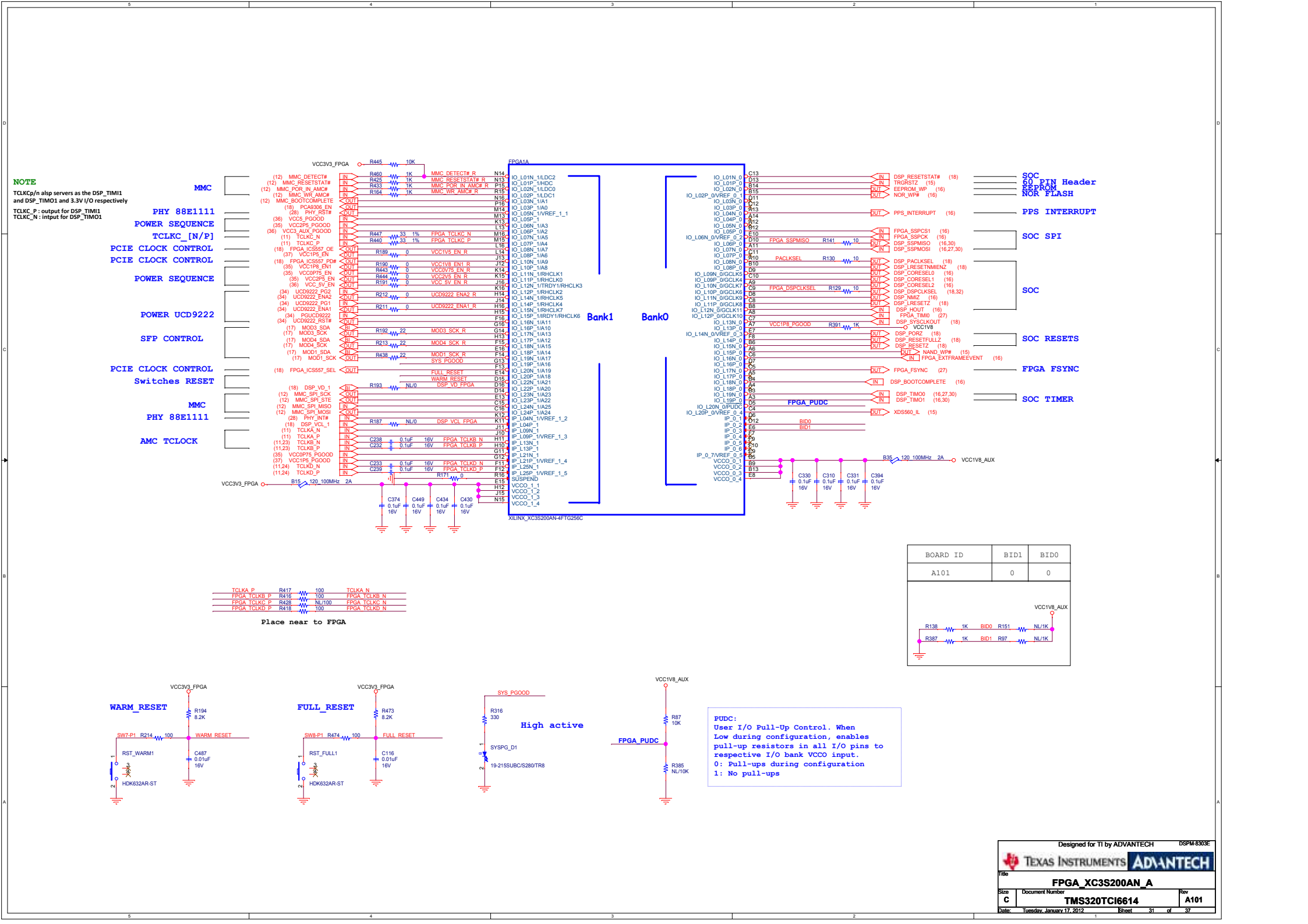
NOTE
TCLKCp/n alsp servers as the DSP_TIMI1 and DSP_TIMO1 and 3.3V I/O respectively
TCLKC_P : output for DSP_TIMI1
TCLKC_N : intput for DSP_TIMO1
MMC
PHY 88E1111
POWER SEQUENCE
TCLKC_[N/P]
PCIE CLOCK CONTROL
PCIE CLOCK CONTROL
POWER SEQUENCE
POWER UCD9222
SFP CONTROL
PCIE CLOCK CONTROL
Switches RESET
MMC
PHY 88E1111
AMC TCLOCK
FPGA1A
Bank1
Bank0
XILINX_XC3S200AN-4FTG256C
SOC
60 PIN Header
EEPROM
NOR FLASH
PPS INTERRUPT
SOC SPI
SOC
SOC RESETS
FPGA FSYNC
SOC TIMER
FPGA_PUDC
Place near to FPGA
WARM_RESET
FULL_RESET
High active
PUDC:
User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCCO input.
0: Pull-ups during configuration
1: No pull-ups
BOARD ID
BID1
BID0
A101
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TEXAS INSTRUMENTS ADVANTECH
FPGA_XC3S200AN_A
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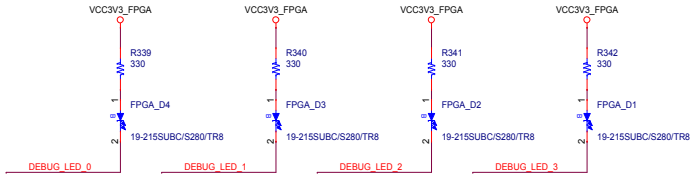
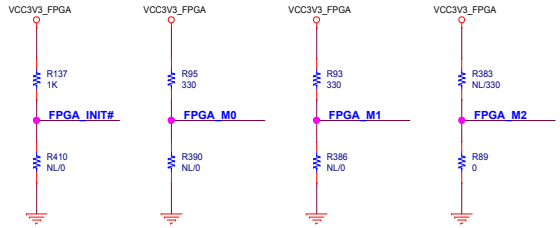
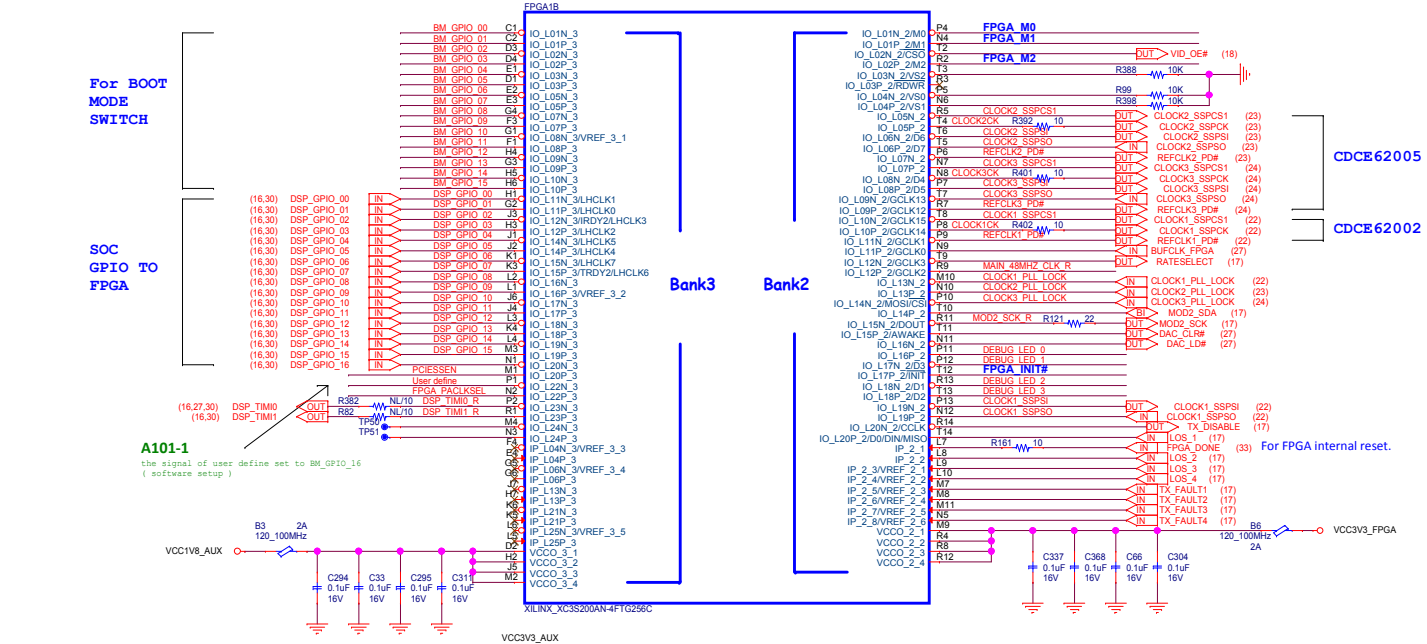
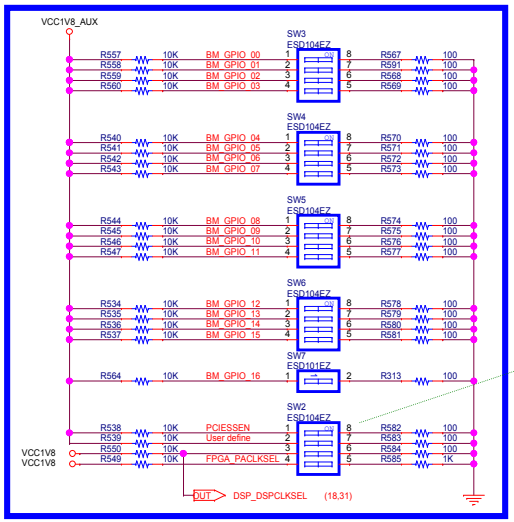


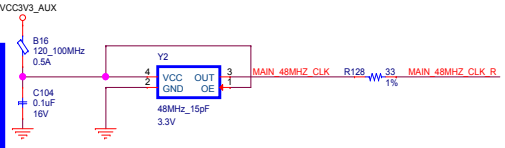
DEBUG_LED





BOOT STRAP CONFIGURATION





A101-1

BM_GPIO_16 is not connected to FPGA, and so we make a workaround on FPGA code to control GPIO16 with SW2(user define pin)

Boot Master

BM_GPIO16	Description
0	When the master bit of DEVSTAT is set to 0, the CorePac initiates boot.
1	When the master bit of DEVSTAT is set to 1, the ARM initiates boot

CorePac Boot Device

BM_GPIO 3 2 1	Boot Device	NOTE
0 0 0	NO BOOT/EMIF16	
0 0 1	sRIO	
0 1 0	SGMII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCIe	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

ARM Boot Device

BM_GPIO 10 9 8 7	1st Boot Device	2nd Boot Device
0 0 0 0	No Boot	N/A
0 0 0 1	UART	EMIF16
0 0 1 0	UART	EMIF16/wait
0 0 1 1	UART	NAND
0 1 0 0	Ethernet	EMIF16
0 1 0 1	Ethernet	EMIF16/wait
0 1 1 0	Ethernet	NAND
0 1 1 1	PCIe	EMIF16
1 0 0 0	PCIe	EMIF16/wait
1 0 0 1	PCIe	NAND
1 0 1 0	SPI	EMIF16
1 0 1 1	SPI	EMIF16/wait
1 1 0 0	SPI	NAND
1 1 0 1	EMIF16	NAND
1 1 1 0	NAND/I2C	EMIF16
1 1 1 1	NAND	EMIF16

CorePac Boot Configuration

DIP Switch	SOC	Boot Mode	Function
BM_GPIO_00	GPIO0	Endian	Endian
BM_GPIO [01:03]	GPIO[1:3]	BOOTMODE[00:02]	Boot Device
BM_GPIO [04:05]	GPIO[4:5]	BOOTMODE[03:04]	Reserved
BM_GPIO [06:10]	GPIO[6:10]	BOOTMODE[05:09]	Device Cfg
BM_GPIO [11:13]	GPIO[11:13]	BOOTMODE[10:12]	PLL Multiplier/I2C
BM_GPIO [14:15]	GPIO[14:15]	PCIESSMODE[0:1]	Endpt/RootComplex
BM_GPIO 16	GPIO16	BOOTMODE13	Master

ARM Boot Configuration

DIP Switch	SOC	Boot Mode	Function
BM_GPIO_00	GPIO0	Endian	Endian
BM_GPIO [01:02]	GPIO[1:2]	BOOTMODE[00:01]	Reserved
BM_GPIO [03:06]	GPIO[3:6]	BOOTMODE[02:05]	Boot Mode Config
BM_GPIO [07:10]	GPIO[7:10]	BOOTMODE[06:09]	Boot Mode Sequence
BM_GPIO [11:13]	GPIO[11:13]	BOOTMODE[10:12]	PLL Cfg
BM_GPIO [14:15]	GPIO[14:15]	PCIESSMODE[0:1]	Endpt/RootComplex
BM_GPIO 16	GPIO16	BOOTMODE13	Master

PCIe Mode selection(PCIESSMODE[1:0])

BM_GPIO[15:14] INPUT	Description
00b	PCIe in End-point mode
01b	PCIe in Legacy End-point mode(no support for MSI)
10b	PCIe in Legacy Root complex mode

PLL Settings

BM_GPIO 13 12 11	INPUT CLK (MHz)	CorePac System PLL Configuration
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

PCIESSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIE subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIE subsystem is enabled

CLK Mode

Clock	Input	Description
Default_Down SYSCLK / ALTCORECLK	DSP_DSPCLKSELL = 0	SYSCLK used to clock the core PLL.
	DSP_DSPCLKSELL = 1	ALTCORECLK is used to clock the core PLL
Default_Down PASSCLK	FPGA_PACLKSEL = 0	PASSCLK is not used and should be tied to a static state.
	FPGA_PACLKSEL = 1	PASSCLK is used as a source for the PA_SS PLL. It must be present before the PA_SS PLL is removed from reset and programmed

Designed for TI by ADVANTECH DSPM-8303E

TEXAS INSTRUMENTS ADVANTECH

Title: FPGA_XC3S200AN_B

Size	Document Number	Rev
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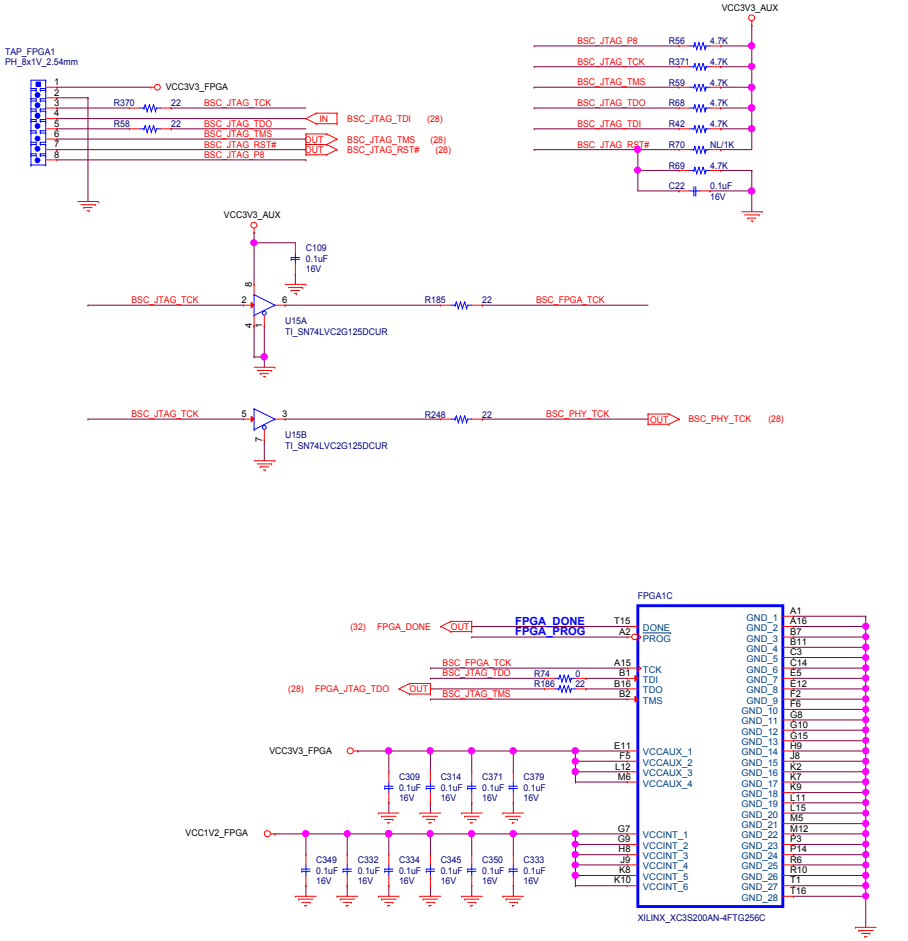

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DSPM-8303E

TEXAS INSTRUMENTS ADVANTECH

Title	FPGA_XC3S200AN_C	
Size: C	Document Number: TMS320TCI6614	Rev: A101
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CVDD

note: he caps on BPCAP and V33A/ V33D pins need to be placed at the same side with UCD9222 and keep the caps as close as possible.

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Parallel the 0.1uF capacitor at the R102 and R103 for VCC1P0 DC load failure

Remove other JTAG pins from the boundary scan chain.

PMBUS Address
=> 6*12+6 = 78
=> 0x4Eh

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--

SOC

UCD9222

Series resistors on EA nets to be placed at the load for proper voltage feedback.

SOC Vcore @TBD

VCC1V0

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DSPM-8303E

Title: Smart_Reflex AVS

Size	Document Number	Rev
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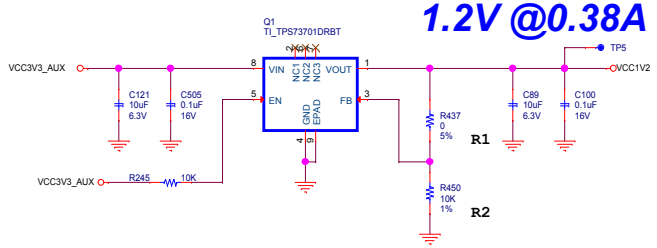
VCC1V2

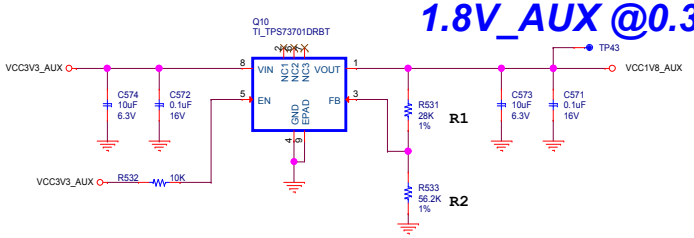
1.2V @0.38A



Vout=(R1+R2)/R2*1.204
1.204V = (0+10k)/10k*1.204

VCC1V8_AUX

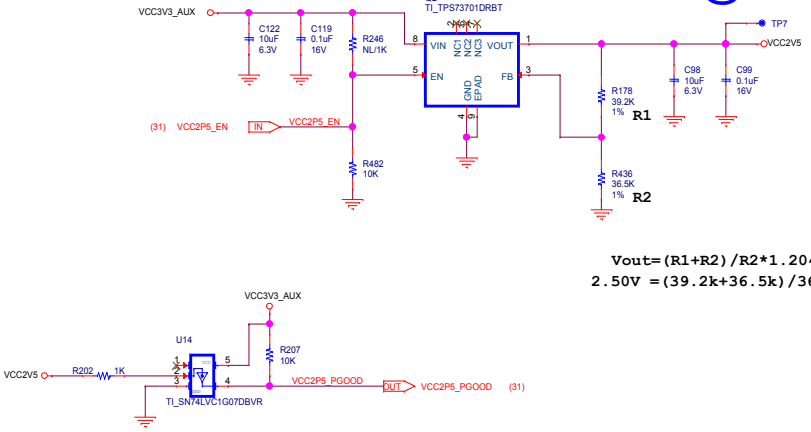
1.8V_AUX @0.3A



Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC2V5

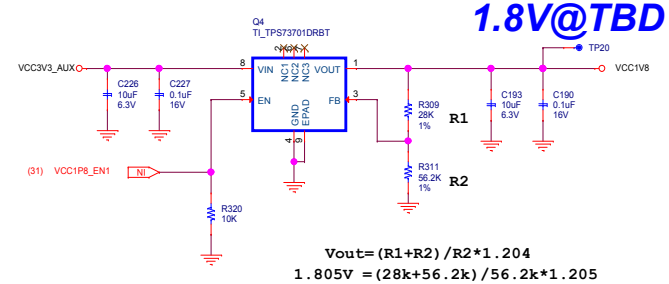
2.5V @0.21A



Vout=(R1+R2)/R2*1.204
2.50V =(39.2k+36.5k)/36.5k*1.204

VCC1V8

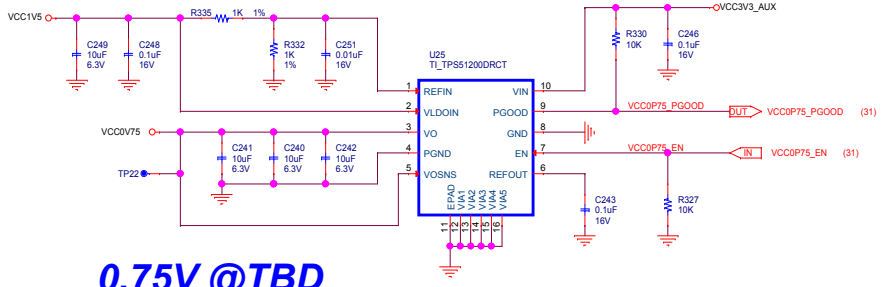
1.8V@TBD



Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC0V75

0.75V @TBD



Designed for TI by ADVANTECH DSPM-8303E

Title	Power_1.2V/1.8V/2.5V/0.75V	
Size C	Document Number TMS320TCI6614	Rev A101
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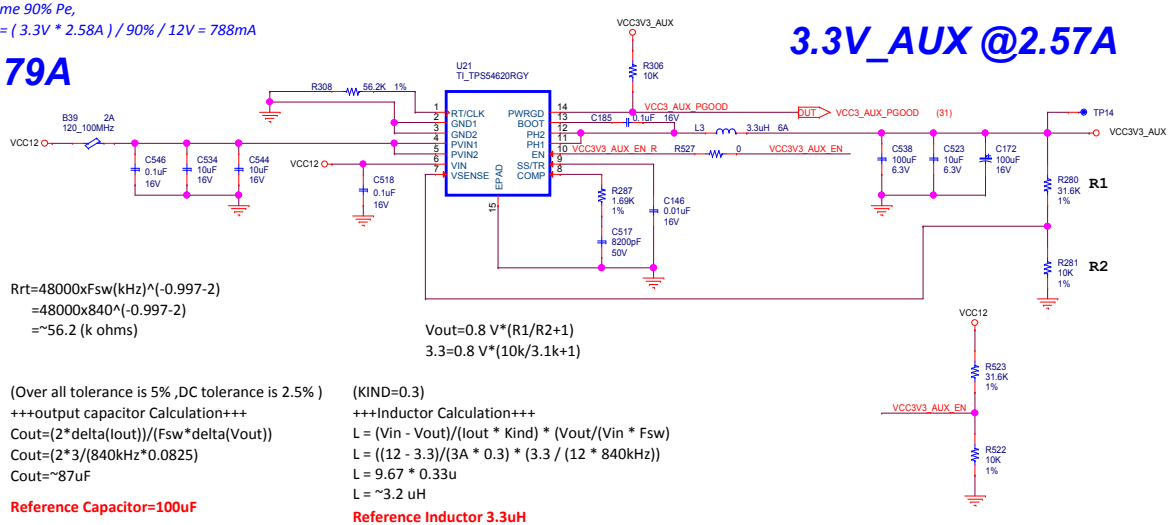
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.57A



Rrt=48000xFsw(kHz)^(-0.997-2)
=48000x840^(-0.997-2)
=~56.2 (k ohms)

Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*3/(840kHz*0.0825)
Cout=~87uF

Reference Capacitor=100uF

(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3A * 0.3) * (3.3 / (12 * 840kHz))
L = 9.67 * 0.33u
L = ~3.2 uH

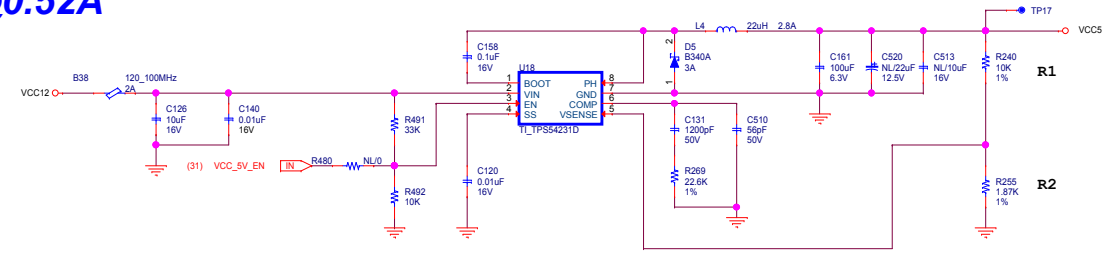
Reference Inductor 3.3uH

VCC5

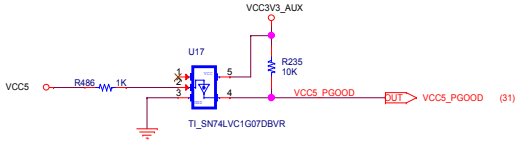
Assume 80% Pe,
*Iin = (5V * 1A) / 80% / 12V = 520mA*

12V@0.52A

5V @1A



Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)



+++output capacitor Calculation+++

$$C_{O\_min} = 1/(2 \times \pi \times R_0 \times F_{CO\_max})$$

Cout=1/(2 * 3.14 * 5 * 25K)
Cout=1.3 uf
Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12.6 - 5)/1 * Kind) * (5 / (12.7 * 570K))
L = ((7.6/ 0.3) * (5 / (7239K))
L = (25.3) * (0.69M)
L = 17.5uH
Reference Inductor 22uH

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Title	Power_VCC5 / VCC3V3_AUX	
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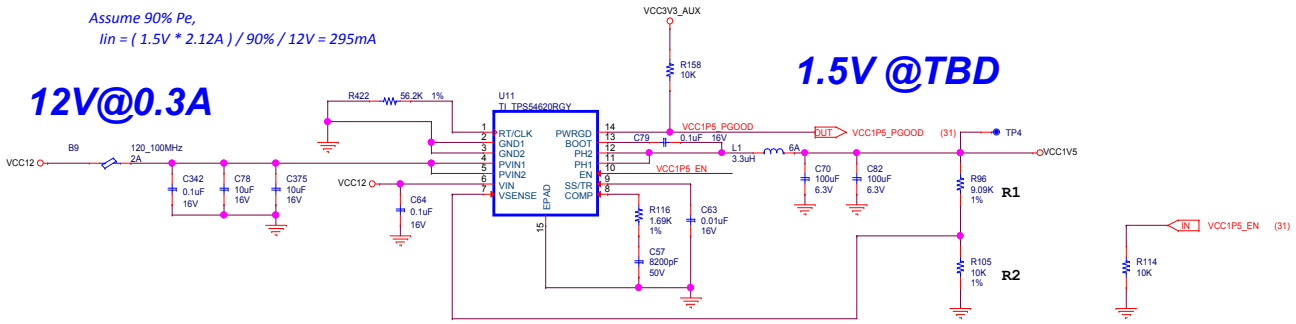
VCC1V5



Vout=0.8 V*(R1/R2+1)

1.52=0.8 V*(9.09k/10k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2A)/(840kHz*0.0375)
Cout= 4/31.5k
Cout=~127uF
Reference Capacitor=200uF

+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * Vout/(Vin * Fsw)
L = (12 - 1.5)/(2A * 0.3) * 1.5 / (12 * 840kHz)
L = (17.5) * (0.15u)
L = ~2.63uH
Reference Inductor 3.3uH

Designed for TI by ADVANTECH DSPM-8303E

TEXAS INSTRUMENTS ADVANTECH

Title		
Power VCC1V5		
Size: C	Document Number: TMS320TCI6614	Rev: A101
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