

TMDXEVM6670L EVM

Technical Reference Manual

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Preface

About this Document

This document is a Technical Reference Manual for the TMS320C6670 Evaluation Module (TMDXEVM6670) designed and developed by Advantech Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono spaced font. Examples use bold for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

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Document Revision History

| Release | Chapter | Description of Change |
|---------|---------|--|
| 1.0 | All | First Release for Beta1 and Beta2 EVMs |
| 2.0 | All | Second Release for production |
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Acronyms

| Acronym | Description |
|--------------------------|---|
| AMC or <i>AdvancedMC</i> | Advanced Mezzanine Card |
| AIF2 | Antenna Interface 2 |
| CCS | Code Composer Studio |
| DDR3 | Double Data Rate 3 Interface |
| DSP | Digital Signal Processor |
| DTE | Data Terminal Equipment |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| EMAC | Ethernet Media Access Controller |
| EMIF | External Memory Interface |
| EVM | Evaluation Module |
| FPGA | Field Programmable Gate Array |
| I2C | Inter Integrated Circuit |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| JTAG | Joint Test Action Group |
| LED | Light Emitting Diode |
| MCH | MicroTCA Carrier Hub |
| MTCA or <i>MicroTCA</i> | Micro Telecommunication Computing Architecture |
| MMC | Module Management Controller |
| PICMG [®] | PCI Industrial Computer Manufacturers Group |
| RFU | Reserved for Future Use |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SERDES | Serializer-Deserializer |
| SGMII | Serial Gigabit Media Independent Interface |
| SRIO | Serial RapidIO |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| XDS560v2 | Texas Instruments' System Trace Emulator |

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1. Overview

This chapter provides an overview of the TMDXEVM6670L along with the key features and block diagram.

1.1 Key Features

1.2 Functional Overview

1.3 Basic Operation

1.4 Configuration Switch Settings

1.5 Power Supply

1.1 Key Features

The TMDXEVM6670L is a high-performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments TMS320C6670 Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320C6670 DSP. The EVM's form-factor is equivalent to a single-wide PICMG® AMC.0 R2.0 *AdvancedMC* module.

Schematics, code examples, and application notes are available to ease the hardware development process and to reduce the time to market.

The key features of the TMDXEVM6670L EVM are:

- Texas Instruments multicore DSP – TMS320C6670
- 512 Mbytes of DDR3-1333 memory
- 64 Mbytes of NAND Flash
- 16MB SPI NOR FLASH
- Two Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate – one on AMC connector and one RJ-45 connector
- 170-pin B+ style AMC interface
- High Performance connector for the HyperLink interface
- 128K-byte I2C EEPROM for booting
- 2 User LEDs, 5 Banks of DIP Switches and 4 Software-controlled LEDs
- RS232 Serial interface on 3-pin header or UART over mini-USB connector
- Timer, SPI, GPIO and UART signals on the 80-pin expansion header
- Onboard XDS100 type emulation using high-speed USB 2.0 interface

- TI 60-Pin JTAG header to support all external emulator types
- Optional XDS560v2 System Trace Emulation Mezzanine Card
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12 V/3.0 A) or AMC carrier backplane
- PICMG® AMC.0 R2.0 single width, full height *AdvancedMC* module

1.2 Functional Overview

The TMS320C6670 Communications Infrastructure KeyStone SoC is a member of the C66xx SoC family based on TI's new KeyStone Multicore SoC Architecture designed specifically for high-performance wireless infrastructure applications. The TMS320C6670 provides a very high performance macro basestation platform for developing all wireless standards including WCDMA/HSPA/HSPA+, TD-SCDMA, GSM, TDD-LTE, FDD-LTE, and WiMAX. The C6670 also sets a new standard for clock speed with operating frequencies up to 1.2 GHz.

TI's SoC architecture provides a programmable platform integrating various subsystems (C66x cores, IP network, radio layers 1 and 2, and transport processing) and uses a queue-based communication system that allows the SoC resources to operate efficiently and seamlessly. This unique SoC architecture also includes a TeraNet Switch that enables the wide mix of system elements, from programmable cores to dedicated coprocessors and high-speed IO, to operate at maximum efficiency with no blocking or stalling.

The functional block diagram of TMDXEVM6670L is shown in the figure below:

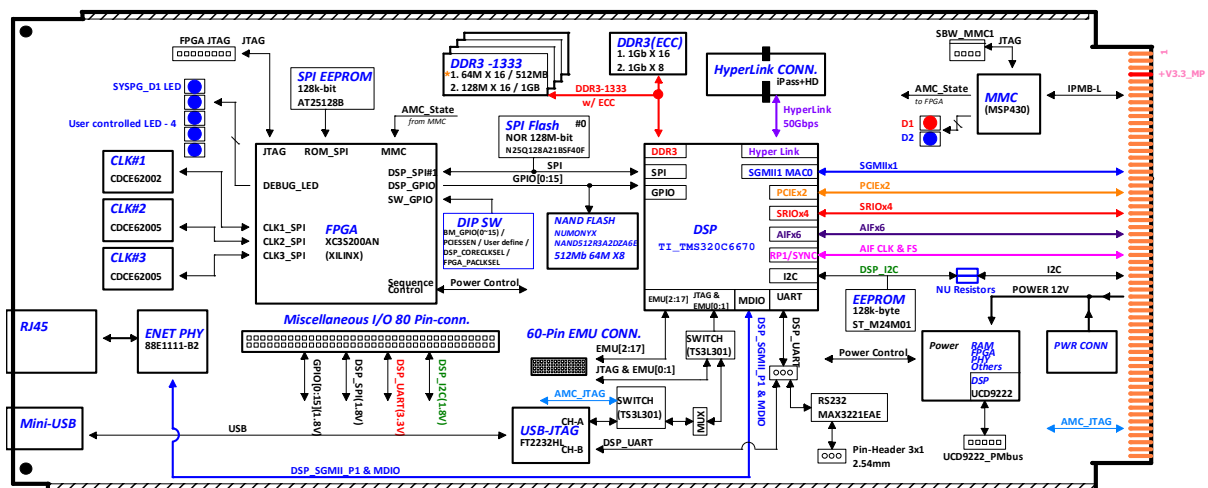


Figure 1.1: Block Diagram of TMDXEVM6670L EVM

1.3 Basic Operation

The TMDXEVM6670L platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interface with the board via on-board emulation circuitry using the USB cable supplied

with this EVM or through an external emulator.

The EVM comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. The MCSDK also includes an out-of-box demonstration; see the "MCSDK Getting Started Guide".

To start operating the board, follow instructions in the Quick Start Guide. This guide provides instruction for proper connections and configuration for running the POST and OOB Demos. After completing the POST and OOB Demos, proceed with installing CCS and the EVM support files by following the instructions on the DVD. This process will install all the necessary development tools, drivers and documentation.

After the installation has completed, follow the steps below to run Code Composer Studio.

1. Power-on the board using the power brick adaptor (12 V/3.0 A) supplied with this EVM or insert this EVM board into a MicroTCA chassis or AMC carrier backplane.
2. Connect the USB cable from host PC to the EVM board.
3. Launch Code Composer Studio from the host PC by double clicking on its icon on the PC desktop.

Detailed information about the EVM including examples and reference materials are available in the DVD included with this EVM kit.

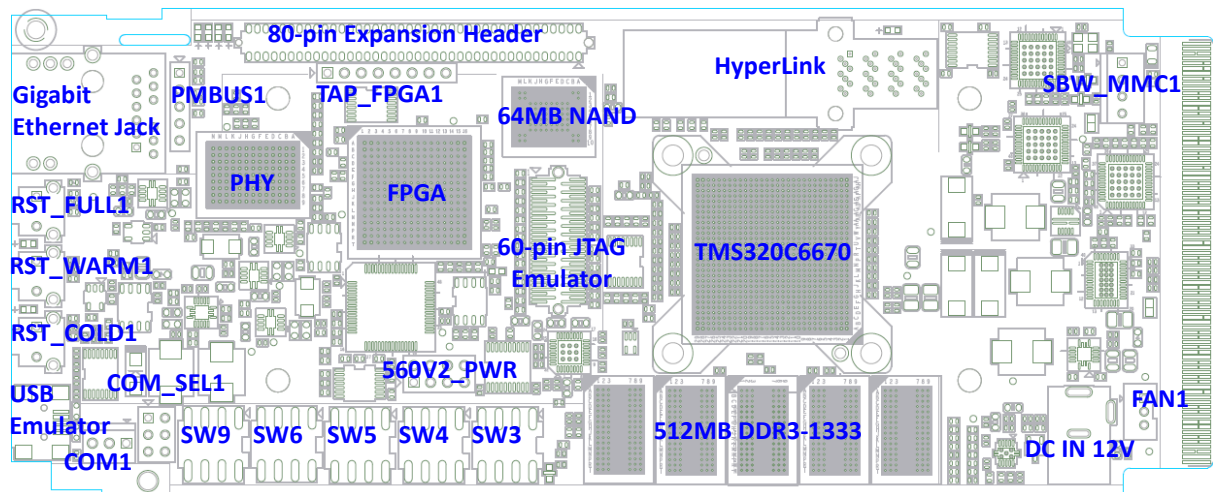


Figure 1.2: TMDXEVM6670L EVM Layout

1.4 Boot Mode and Boot Configuration Switch Setting

The TMDXEVM6670L has 20 sliding DIP switches (Board Ref. SW3 to SW6 and SW9) to determine boot mode, boot configuration, device number, endian mode, CorePac PLL clock selection, and PCIe Mode selection options at the POR stage of the DSP.

1.5 Power Supply

The TMDXEVM6670L can be powered from a single +12V / 3.0A DC (36W) external power supply connected to the DC power jack (DC_IN1). Internally, +12-V input is converted into required voltage levels using local DC-DC converters.

- CVDD (+0.70 V~+1.10 V) is used for the DSP core logic
- +1.0 V is used for internal memory and HyperLink / SRIO / SGMII / PCIe / AIF2 termination of DSP
- +1.5 V is used for DDR3 of DSP, Supplying HyperLink / SRIO / SGMII / PCIe / AIF2 regulators in DSP and RAM chips
- +1.8 V is used for DSP PLLs, DSP LVCMOS I/Os, FPGA I/Os driving the DSP
- +2.5 V is used for the Gigabit Ethernet PHY core
- +1.2 V is used for FPGA core and Gigabit Ethernet PHY core
- +3.3 V is used for the FPGA I/Os
- +5 V and +3.3 V is used to power the XDS560v2 mezzanine card
- The DC power jack connector is a 2.5mm barrel-type plug with positive polarity on the center tip

The TMDXEVM6670L can also draw power from the AMC edge connector (AMC1). If the board is inserted into a PICMG® MicroTCA.0 R1.0-compliant system chassis or AMC Carrier backplane, an external +12 V supply from DC jack (DC_IN1) is not required.

2. Introduction to the TMDXEVM6670L board

This chapter provides an introduction and details of interfaces for the TMDXEVM6670L board. It contains:

- 2.1 Memory Map
- 2.2 EVM Boot mode and Boot configuration switch settings
- 2.3 JTAG - Emulation Overview
- 2.4 Clock Domains
- 2.5 None-Volatile Memories (I²C EEPROM / SPI NOR Flash / NAND flash)
- 2.6 FPGA Functions
- 2.7 Gigabit Ethernet Connections
- 2.8 Serial RapidIO (SRIO) Interface
- 2.9 DDR3 External Memory Interface
- 2.10 HyperLink Interface
- 2.11 PCI express interface
- 2.12 Antenna Interface (AIF2)
- 2.13 UART Interfaces
- 2.14 Module Management Controller for IPMI
- 2.15 Expansion Headers

2.1 Memory Map

The memory map of the TMS320C6670 device is as shown in Table 2.1. The external memory configuration register address ranges in the TMS320C6670 device begin at the hex address location 0x8000 0000 for the DDR3 Memory Controller.

Table 2.1: TMS320C6670 Memory Map

| Logical 32 bit Address | | Physical 36 bit Address | | Bytes | Description |
|------------------------|-----------|-------------------------|-------------|-------|--|
| Start | End | Start | End | | |
| 0080 0000 | 008F FFFF | 0 0080 0000 | 0 008F FFFF | 1M | L2 SRAM |
| 00E0 0000 | 00E0 7FFF | 0 00E00000 | 0 00E0 7FFF | 32K | L1P SRAM |
| 00F0 0000 | 00F0 7FFF | 0 00F00000 | 0 00F0 7FFF | 32K | L1D SRAM |
| 0100 0000 | 01BF FFFF | 0 0100 0000 | 0 01BF FFFF | 12 M | C66x CorePac Registers |
| 01D0 0000 | 01D0 007F | 0 01D0 0000 | 0 01D0 007F | 128 | Tracer 0 |
| 01D0 8000 | 01D0 807F | 0 01D0 8000 | 0 01D0 807F | 128 | Tracer 1 |
| 01D1 0000 | 01D1 007F | 0 01D1 0000 | 0 01D1 007F | 128 | Tracer 2 |
| 01D1 8000 | 01D1 807F | 0 01D1 8000 | 0 01D1 807F | 128 | Tracer 3 |
| 01D2 0000 | 01D2 007F | 0 01D2 0000 | 0 01D2 007F | 128 | Tracer 4 |
| 01D2 8000 | 01D2 807F | 0 01D2 8000 | 0 01D2 807F | 128 | Tracer 5 |
| 01D3 0000 | 01D3 007F | 0 01D3 0000 | 0 01D3 007F | 128 | Tracer 6 |
| 01D3 8000 | 01D3 807F | 0 01D3 8000 | 0 01D3 807F | 128 | Tracer 7 |
| 01D4 0000 | 01D4 007F | 0 01D4 0000 | 0 01D4 007F | 128 | Tracer 8 |
| 01D4 8000 | 01D4 807F | 0 01D4 8000 | 0 01D4 807F | 128 | Tracer 9 |
| 01D5 0000 | 01D5 007F | 0 01D5 0000 | 0 01D5 007F | 128 | Tracer 10 |
| 01D5 8000 | 01D5 807F | 0 01D5 8000 | 0 01D5 807F | 128 | Tracer 11 |
| 01D6 0000 | 01D6 007F | 0 01D6 0000 | 0 01D6 007F | 128 | Tracer 12 |
| 01D6 8000 | 01D6 807F | 0 01D6 8000 | 0 01D6 807F | 128 | Tracer 13 |
| 01D7 0000 | 01D7 007F | 0 01D7 0000 | 0 01D7 007F | 128 | Tracer 14 |
| 01D7 8000 | 01D7 807F | 0 01D7 8000 | 0 01D7 807F | 128 | Tracer 15 |
| 01F0 0000 | 01F7 FFFF | 0 01F0 0000 | 0 01F7 FFFF | 512k | AIF2 Control |
| 0200 0000 | 0208 FFFF | 0 0200 0000 | 0 0208 FFFF | 576K | Packet Accelerator Configuration |
| 0209 0000 | 020B FFFF | 0 0209 0000 | 0 020B FFFF | 192K | Ethernet Switch Subsystem Configuration |
| 020C 0000 | 020F FFFF | 0 020C 0000 | 0 020F FFFF | 256K | Security Accelerator Subsystem Configuration |
| 021C 0000 | 021C 03FF | 0 021C 0000 | 0 021C 03FF | 1K | TCP3d-A |
| 021C 8000 | 021C 83FF | 0 021C 8000 | 0 021C 83FF | 1K | TCP3d-B |
| 021D 0000 | 021D 00FF | 0 021D 0000 | 0 021D 00FF | 256 | VCP2_A |
| 021D 4000 | 021D 40FF | 0 021D 4000 | 0 021D 40FF | 256 | VCP2_B |
| 021D 8000 | 021D 80FF | 0 021D 8000 | 0 021D 80FF | 256 | VCP2_C |
| 021D C000 | 021D C0FF | 0 021D C000 | 0 021D C0FF | 256 | VCP2_D |
| 021E 0000 | 021E 0FFF | 0 021E 0000 | 0 021E 0FFF | 4K | TCP3e |
| 021F 0000 | 021F 07FF | 0 021F 0000 | 0 021F 07FF | 2K | FFTC-A Configuration |
| 021F 4000 | 021F 47FF | 0 021F 4000 | 0 021F 47FF | 2K | FFTC-B Configuration |
| 0220 0000 | 0220 007F | 0 0220 0000 | 0 0220 007F | 128 | Timer0 |
| 0221 0000 | 0221 007F | 0 0221 0000 | 0 0221 007F | 128 | Timer1 |
| 0222 0000 | 0222 007F | 0 0222 0000 | 0 0222 007F | 128 | Timer2 |
| 0223 0000 | 0223 007F | 0 0223 0000 | 0 0223 007F | 128 | Timer3 |
| 0224 0000 | 0224 007F | 0 0224 0000 | 0 0224 007F | 128 | Timer4 |
| 0225 0000 | 0225 007F | 0 0225 0000 | 0 0225 007F | 128 | Timer5 |
| 0226 0000 | 0226 007F | 0 0226 0000 | 0 0226 007F | 128 | Timer6 |
| 0227 0000 | 0227 007F | 0 0227 0000 | 0 0227 007F | 128 | Timer7 |
| 0231 0000 | 0231 01FF | 0 0231 0000 | 0 0231 01FF | 512 | PLL Controller |
| 0232 0000 | 0232 00FF | 0 0232 0000 | 0 0232 00FF | 256 | GPIO |
| 0233 0000 | 0233 03FF | 0 0233 0000 | 0 0233 03FF | 1K | SmartReflex |
| 0235 0000 | 0235 0FFF | 0 0235 0000 | 0 0235 0FFF | 4K | Power Sleep Controller |
| 0236 0000 | 0236 03FF | 0 0236 0000 | 0 0236 03FF | 1K | Memory Protection Unit (MPU) 0 |

| | | | | | |
|-----------|-----------|-------------|-------------|-----|--|
| 0236 8000 | 0236 83FF | 0 0236 8000 | 0 0236 83FF | 1K | Memory Protection Unit (MPU) 1 |
| 0237 0000 | 0237 03FF | 0 0237 0000 | 0 0237 03FF | 1K | Memory Protection Unit (MPU) 2 |
| 0237 8000 | 0237 83FF | 0 0237 8000 | 0 0237 83FF | 1K | Memory Protection Unit (MPU) 3 |
| 0244 0000 | 0244 3FFF | 0 0244 0000 | 0 0244 3FFF | 16K | DSP Trace Formatter 0 |
| 0245 0000 | 0245 3FFF | 0 0245 0000 | 0 0245 3FFF | 16K | DSP Trace Formatter 1 |
| 0246 0000 | 0246 3FFF | 0 0246 0000 | 0 0246 3FFF | 16K | DSP Trace Formatter 2 |
| 0247 0000 | 0247 3FFF | 0 0247 0000 | 0 0247 3FFF | 16K | DSP Trace Formatter 3 |
| 0253 0000 | 0253 007F | 0 0253 0000 | 0 0253 007F | 128 | I2C Data & Control |
| 0254 0000 | 0254 003F | 0 0254 0000 | 0 0254 003F | 64 | UART |
| 0260 0000 | 0260 1FFF | 0 0260 0000 | 0 0260 1FFF | 8K | Secondary Interrupt Contoller (INTC) 0 |
| 0260 4000 | 0260 5FFF | 0 0260 4000 | 0 0260 5FFF | 8K | Secondary Interrupt Contoller (INTC) 1 |
| 0260 8000 | 0260 9FFF | 0 0260 8000 | 0 0260 9FFF | 8K | Secondary Interrupt Contoller (INTC) 2 |
| 0262 0000 | 0262 03FF | 0 0262 0000 | 0 0262 03FF | 1K | Chip-Level Registers |
| 0264 0000 | 0264 07FF | 0 0264 0000 | 0 0264 07FF | 2K | Semaphore |
| 0270 0000 | 0270 7FFF | 0 0270 0000 | 0 0270 7FFF | 32K | EDMA Channel Controller (TPCC) 0 |
| 0272 0000 | 0272 7FFF | 0 0272 0000 | 0 0272 7FFF | 32K | EDMA Channel Controller (TPCC) 1 |
| 02740000 | 0274 7FFF | 0 02740000 | 0 0274 7FFF | 32K | EDMA Channel Controller (TPCC) 2 |
| 0276 0000 | 0276 03FF | 0 0276 0000 | 0 0276 03FF | 1K | EDMA TPCC0 Transfer Controller (TPTC) 0 |
| 0276 8000 | 0276 83FF | 0 0276 8000 | 0 0276 83FF | 1K | EDMA TPCC0 Transfer Controller (TPTC) 1 |
| 0277 0000 | 0277 03FF | 0 0277 0000 | 0 0277 03FF | 1K | EDMA TPCC1 Transfer Controller (TPTC) 0 |
| 0277 8000 | 0277 83FF | 0 0277 8000 | 0 0277 83FF | 1K | EDMA TPCC1 Transfer Controller (TPTC) 1 |
| 0278 0000 | 0278 03FF | 0 0278 0000 | 0 0278 03FF | 1K | EDMA TPCC1 Transfer Controller (TPTC) 2 |
| 0278 8000 | 0278 83FF | 0 0278 8000 | 0 0278 83FF | 1K | EDMA TPCC1 Transfer Controller (TPTC) 3 |
| 0279 0000 | 0279 03FF | 0 0279 0000 | 0 0279 03FF | 1K | EDMA TPCC2 Transfer Controller (TPTC) 0 |
| 0279 8000 | 0279 83FF | 0 0279 8000 | 0 0279 83FF | 1K | EDMA TPCC2 Transfer Controller (TPTC) 1 |
| 027A 0000 | 027A 03FF | 0 027A 0000 | 0 027A 03FF | 1K | EDMA TPCC2 Transfer Controller (TPTC) 2 |
| 027A 8000 | 027A 83FF | 0 027A 8000 | 0 027A 83FF | 1K | EDMA TPCC2 Transfer Controller (TPTC) 3 |
| 027D 0000 | 027D 3FFF | 0 027D 0000 | 0 027D 3FFF | 16k | TI Embedded Trace Buffer (TETB) - Core 0 |
| 027E 0000 | 027E 3FFF | 0 027E 0000 | 0 027E 3FFF | 16k | TI Embedded Trace Buffer (TETB) - Core 1 |
| 027F 0000 | 027F 3FFF | 0 027F 0000 | 0 027F 3FFF | 16k | TI Embedded Trace Buffer (TETB) - Core 2 |
| 0280 0000 | 0280 3FFF | 0 0280 0000 | 0 0280 3FFF | 16k | TI Embedded Trace Buffer (TETB) - Core 3 |
| 0285 0000 | 0285 7FFF | 0 0285 0000 | 0 0285 7FFF | 32k | TI Embedded Trace Buffer |

| | | | | | |
|-----------|-----------|-------------|-------------|------|--|
| | | | | | (TETB) - System |
| 0290 0000 | 0290 7FFF | 0 0290 0000 | 0 0290 7FFF | 32K | Serial RapidIO Configuration |
| 02A0 0000 | 02AF FFFF | 0 02A0 0000 | 0 02AF FFFF | 1M | Queue Manager Subsystem Configuration |
| 0800 0000 | 0800 FFFF | 0 0800 0000 | 0 0800 FFFF | 64k | Extended Memory Controller (XMC) Configuration |
| 0BC0 0000 | 0BCF FFFF | 0 0BC0 0000 | 0 0BCF FFFF | 1M | Multicore Shared Memory Controller (MSMC) Config |
| 0C00 0000 | 0C1F FFFF | 0 0C00 0000 | 0 0C1F FFFF | 2M | Multicore Shared Memory (MSM) |
| 1080 0000 | 108F FFFF | 0 1080 0000 | 0 108F FFFF | 1M | Core 0 L2 SRAM |
| 10E0 0000 | 10E0 7FFF | 0 10E0 0000 | 0 10E0 7FFF | 32k | Core 0 L1P SRAM |
| 10F0 0000 | 10F0 7FFF | 0 10F0 0000 | 0 10F0 7FFF | 32k | Core 0 L1D SRAM |
| 1180 0000 | 118F FFFF | 0 1180 0000 | 0 118F FFFF | 1M | Core 1 L2 SRAM |
| 11E0 0000 | 11E0 7FFF | 0 11E0 0000 | 0 11E0 7FFF | 32k | Core 1 L1P SRAM |
| 11F0 0000 | 11F0 7FFF | 0 11F0 0000 | 0 11F0 7FFF | 32k | Core 1 L1D SRAM |
| 1280 0000 | 128F FFFF | 0 1280 0000 | 0 128F FFFF | 1M | Core 2 L2 SRAM |
| 12E0 0000 | 12E0 7FFF | 0 12E0 0000 | 0 12E0 7FFF | 32k | Core 2 L1P SRAM |
| 12F0 0000 | 12F0 7FFF | 0 12F0 0000 | 0 12F0 7FFF | 32k | Core 2 L1D SRAM |
| 1380 0000 | 1388 FFFF | 0 1380 0000 | 0 1388 FFFF | 1M | Core 3 L2 SRAM |
| 13E0 0000 | 13E0 7FFF | 0 13E0 0000 | 0 13E0 7FFF | 32k | Core 3 L1P SRAM |
| 13F0 0000 | 13F0 7FFF | 0 13F0 0000 | 0 13F0 7FFF | 32k | Core 3 L1D SRAM |
| 2000 0000 | 200F FFFF | 0 2000 0000 | 0 200F FFFF | 1M | System Trace Manager (STM) Configuration |
| 2060 0000 | 206F FFFF | 0 2060 0000 | 0 206F FFFF | 1M | TCP3d-B Data |
| 2080 0000 | 208F FFFF | 0 2080 0000 | 0 208F FFFF | 1M | TCP3d-A Data |
| 2090 0000 | 2090 1FFF | 0 2090 0000 | 0 2090 1FFF | 8K | TCP3e Data Write Port |
| 2090 2000 | 2090 3FFF | 0 2090 2000 | 0 2090 3FFF | 8K | TCP3e Data Read Port |
| 20B0 0000 | 20B1 FFFF | 0 20B0 0000 | 0 20B1 FFFF | 128k | Boot ROM |
| 20BF 0000 | 20BF 03FF | 0 20BF 0000 | 0 20BF 03FF | 1k | SPI |
| 2100 0000 | 2100 00FF | 0 2100 0000 | 0 2100 00FF | 256 | DDR3 EMIF Configuration |
| 2140 0000 | 2140 03FF | 0 2140 0000 | 0 2140 03FF | 1K | HyperLink Config |
| 2180 0000 | 2180 7FFF | 0 2180 0000 | 0 2180 7FFF | 32K | PCIe Config |
| 22A0 0000 | 22A0 FFFF | 0 22A0 0000 | 0 22A0 FFFF | 64K | VCP2_A |
| 22B0 0000 | 22B0 FFFF | 0 22B0 0000 | 0 22B0 FFFF | 64K | VCP2_B |
| 22C0 0000 | 22C0 FFFF | 0 22C0 0000 | 0 22C0 FFFF | 64K | VCP2_C |
| 22D0 0000 | 22D0 FFFF | 0 22D0 0000 | 0 22D0 FFFF | 64K | VCP2_D |
| 3400 0000 | 341F FFFF | 0 3400 0000 | 0 341F FFFF | 2M | Queue Manager Subsystem Data |
| 4000 0000 | 4FFF FFFF | 0 4000 0000 | 0 4FFF FFFF | 256M | HyperLink Data |
| 6000 0000 | 6FFF FFFF | 0 6000 0000 | 0 6FFF FFFF | 256M | PCIe Data |
| 8000 0000 | FFFF FFFF | 8 8000 0000 | 8 FFFF FFFF | 2G | DDR3 EMIF Data |

2.2 EVM Boot Mode and Boot Configuration Switch Settings

The TMDXEVM6670L has five configuration switches: SW3, SW4, SW5, SW6 and SW9 that contain 19 individual values latched when reset is released. This occurs when power is applied on the board, after the user presses the FULL_RESET push button or after a POR reset is requested from the MMC.

SW3 determines the general DSP configuration, Little or Big Endian mode, and boot device selection.

SW4, SW5, SW6 and SW9 determine the DSP boot device configuration, CorePac PLL setting and PCIe mode selection.

More information about using these DIP switches is contained in Section 3.3 of this document. For more information on DSP supported Boot Modes, refer to [TMS320C6670 Data Manual](#) and [C66x Bootloader User Guide](#).

2.3 JTAG - Emulation Overview

The TMDXEVM6670L has onboard embedded JTAG emulation circuitry; users do not require an external emulator to connect the EVM with Code Composer Studio. Users can connect CCS with the target DSP in the EVM through the USB cable supplied along with this board.

In case users wish to connect an external emulator to the EVM, the TI 60-pin JTAG header (EMU1) is provided for high speed real-time emulation. The TI 60-pin JTAG supports all standard TI DSP emulators. An adapter will be required for use with some emulators.

The on-board embedded JTAG emulator is the default connection to the DSP. However when an external emulator is connected to EVM, the board circuitry switches automatically to give emulation control to the external emulator.

When the on-board emulator and external emulator are connected at the same time, the external emulator has priority and the onboard emulator is disconnected from the DSP.

The third way of accessing the DSP is through the JTAG port on the AMC edge connector, users can connect the DSP through the AMC backplane if they don't use the XDS100 on-board emulator and the 60-pin header with the external emulator.

The JTAG interface among the DSP, on-board emulator, external emulator and the AMC edge connector is shown in the below figure:

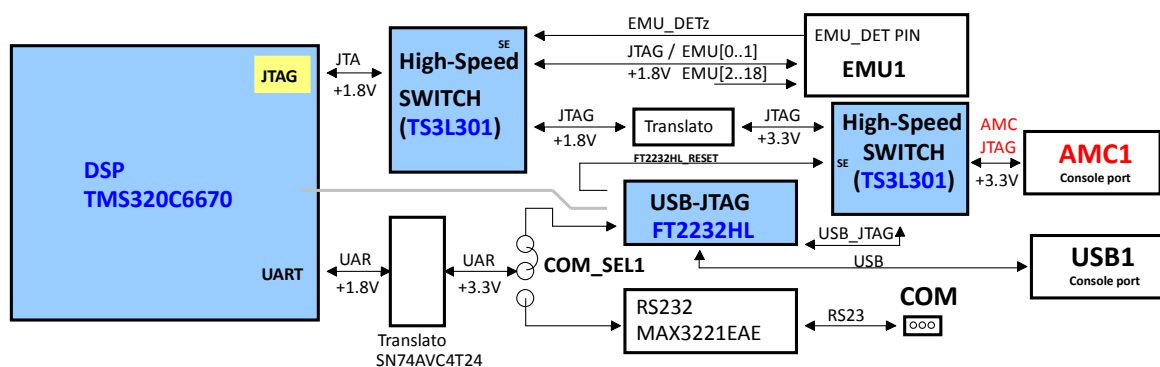


Figure 2.1: TMDXEVM6670L EVM JTAG emulation

2.4 Clock Domains

The EVM incorporates a variety of clocks to the TMS320C6670 DSP as well as other devices that are configured automatically during the power up configuration sequence. The figure below illustrates clocking for the system in the EVM module.

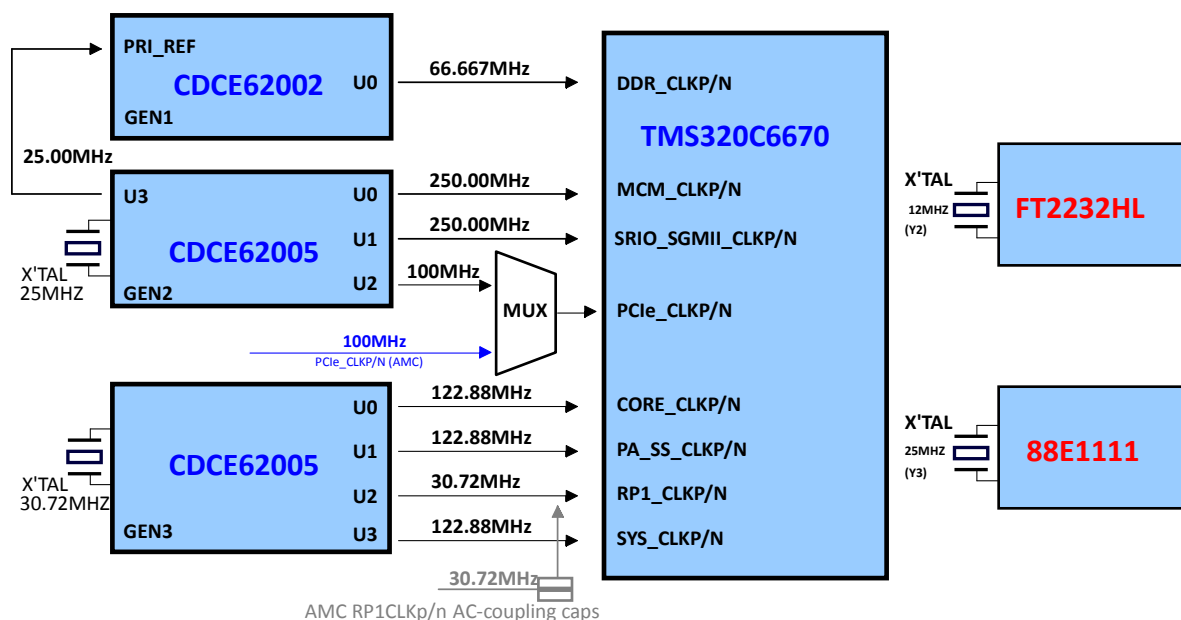


Figure 2.2: TMDXEVM6670L EVM Clock Domains

2.5 Non-Volatile Memories (SEEPROM / SPI NOR Flash / NAND flash)

The I2C modules on the TMS320C6670 may be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one SEEPROM and to the 80-pin expansion header (TEST_PH1). There are two banks in the I2C SEEPROM which respond separately at addresses 0x50 and 0x51. These banks can be loaded with demonstration programs. Currently, the bank at 0x50 contains the I2C boot code and PLL initialization procedure and the bank at 0x51 contains the second level boot-loader program. The second level boot-loader can be used to run the POST program or launch the OOB demonstration from NOR flash memory.

The serial peripheral interconnect (SPI) module provides an interface between the DSP and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on TMS320C6670 is supported only in Master mode.

The NOR FLASH attached to CS0z on the TMS320C6670 is a NUMONYX N25Q128A21. This NOR FLASH size is 16MB. It can contain demonstration programs such as POST or the OOB demonstration. The CS1z of the SPI is used by the DSP to access registers within the FPGA.

The NAND flash is connected by the TMS320C6670 GPIO pins to access the 64M bytes NAND flash, the GPIO pins on the TMS320C6670 connected to the FPGA are only used to boot

configurations during the Power-on period on the EVM. The function block and pin connections are shown in the following figure and table.

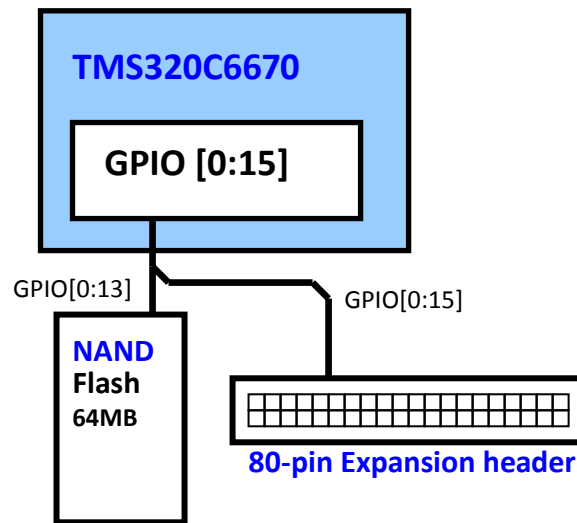


Figure 2.3: TMDXEVM6670L EVM NAND flash connections

| DSP GPIO | NAND Flash | Pin Description |
|-----------------------------|------------|--|
| GPIO[7:0] | I/O[7:0] | The 8-bit data bus |
| GPIO8 | CL | The Command Latch Enable pin |
| GPIO9 | AL | The Address Latch Enable pin |
| GPIO10 | WE# | The Write Enable pin |
| GPIO11 | R/B# | The Ready/Busy# pin |
| GPIO12 | RE# | The Read Enable pin |
| GPIO13 | CE# | The Chip Enable pin |
| NAND_WP# Driving by FPGA | WP# | The Write Protect pin (It's controlled by the FPGA) |

Table 2.2: TMDXEVM6670L EVM NAND flash connections

2.6 FPGA Functions

The FPGA (Xilinx XC3S200AN) controls the reset mechanism of the DSP and provides boot mode and boot configuration data to the DSP through SW3, SW4, SW5, SW6 and SW9. The FPGA also provides the transformation of TCLK[A:D] from AMC connector for the Timer of the DSP, user LEDs control, and one user switch through control registers. All FPGA registers are accessible over the SPI interface.

The figure below shows the interface between TMS320C6670 DSP and FPGA.

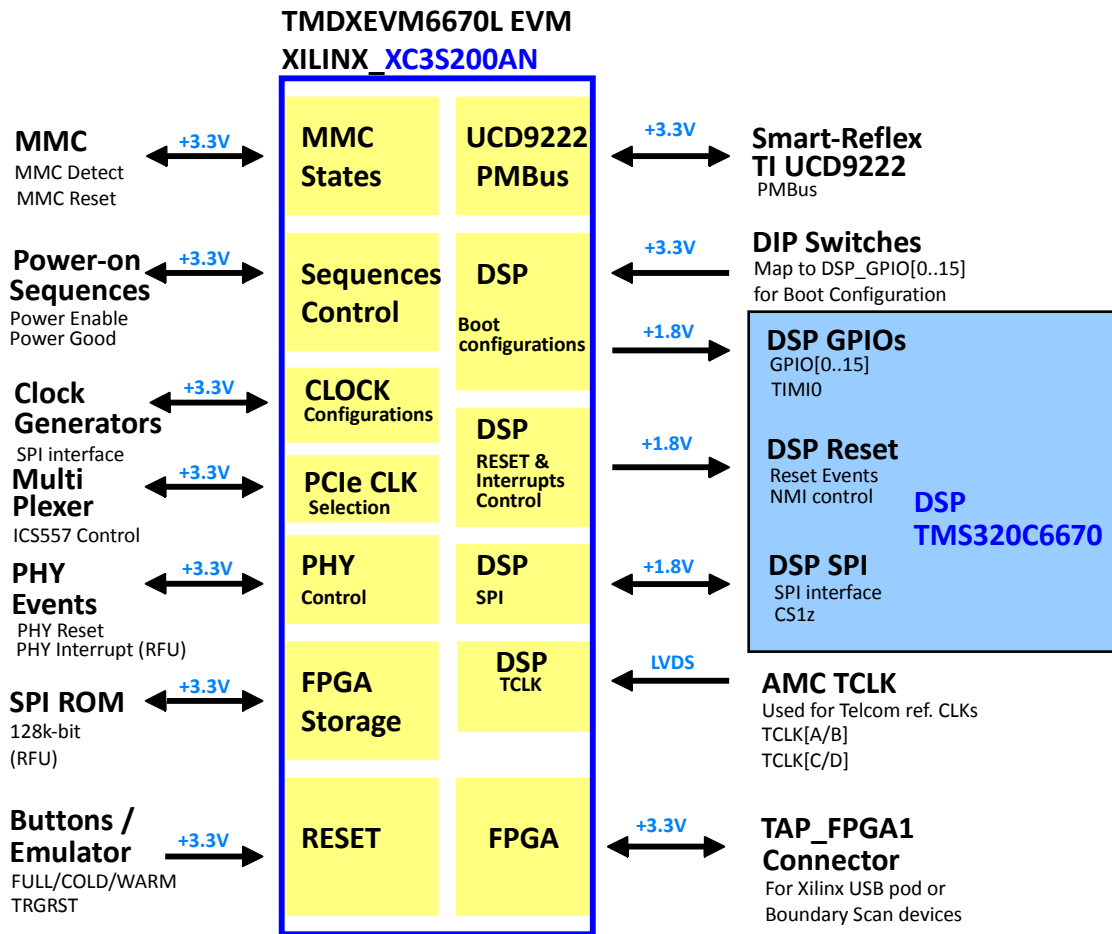


Figure 2.4: TMDXEVM6670L EVM FPGA Connections

2.7 Gigabit Ethernet Connections

The TMDXEVM6670L provides connectivity for both SGMII Gigabit Ethernet ports on the EVM. These are shown in figure below:

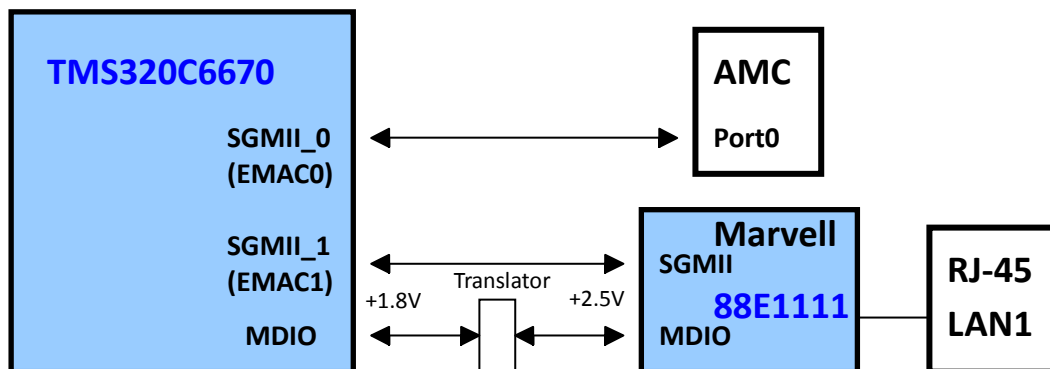


Figure 2.5: TMDXEVM6670L EVM Ethernet Routing

The Ethernet PHY (PHY1) is connected to DSP EMAC1 to provide a copper interface and routed to a Gigabit RJ-45 connector (LAN1). The EMAC0 of DSP is routed to Port0 of the AMC edge connector backplane interface.

2.8 Serial RapidIO (SRIO) Interface

The TMDXEVM6670L supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total 4 RapidIO ports available on TMS320C6670. All SRIO ports are routed to AMC edge connector on board. Below figure shows RapidIO connections between the DSP and AMC edge connector.

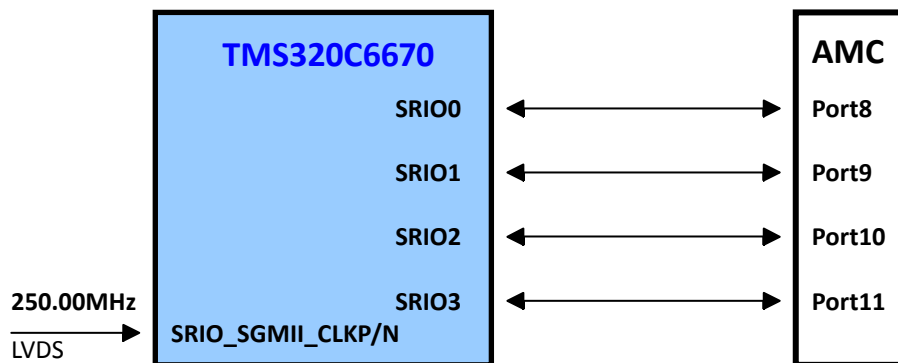


Figure 2.6: TMDXEVM6670L EVM SRIO Port Connections

2.9 DDR3 External Memory Interface

The TMS320C6670 DDR3 interface connects to four 1Gbit (64Meg x 16) DDR3 1333 devices. This configuration allows the use of both “narrow (16-bit)”, “normal (32-bit)”, and “wide (64-bit)” modes of the DDR3 EMIF.

SAMSUNG DDR3 K4B1G1646x-BCH9 SDRAMs (64Mx16; 667Mhz) are used on the DDR3 EMIF.

Below figure illustrates the implementation for the DDR3 SDRAM memory.

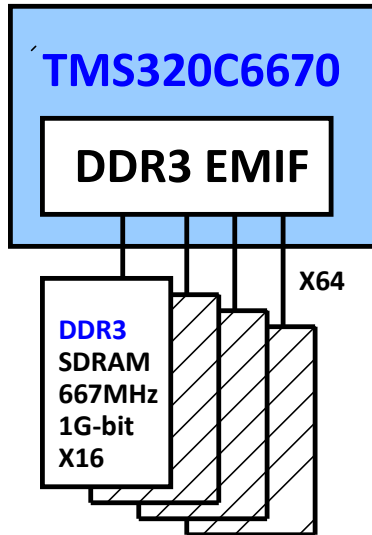


Figure 2.7: TMDXEVM6670L EVM SDRAM

2.10 HyperLink interface

The TMS320C6670 provides the HyperLink bus for companion chip/die interfaces. This is a four-lane SerDes interface designed to operate at 12.5 Gbps per lane. The interface is used to connect with external accelerators.

The interface includes the Serial Station Management Interfaces used to send power management and flow messages between devices. This consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire output buses and two 2-wire input buses. Each 2-wire bus includes a data signal and a clock signal.

Below figure illustrates the HyperLink bus connections on the TMDXEVM6670L EVM.

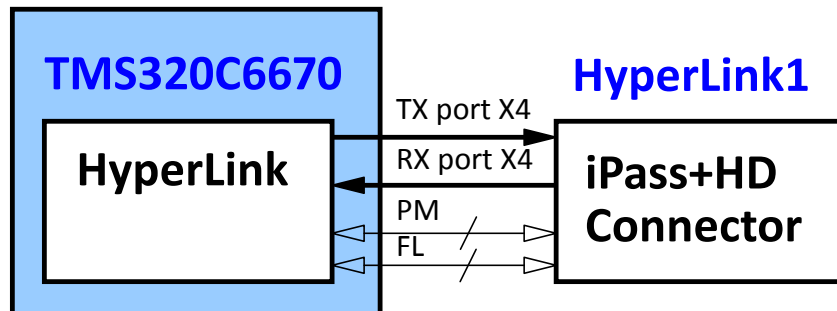


Figure 2.8: TMDXEVM6670L EVM HyperLink connections

2.11 PCI express interface

The 2 lane PCI express (PCIe) interface on TMDXEVM6670L provides a connection between the DSP and AMC edge connector. The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide (literature number SPRUGS6).

The TMDXEVM6670L provides the PCIe connectivity to AMC backplane on the EVM, this is shown in below figure.

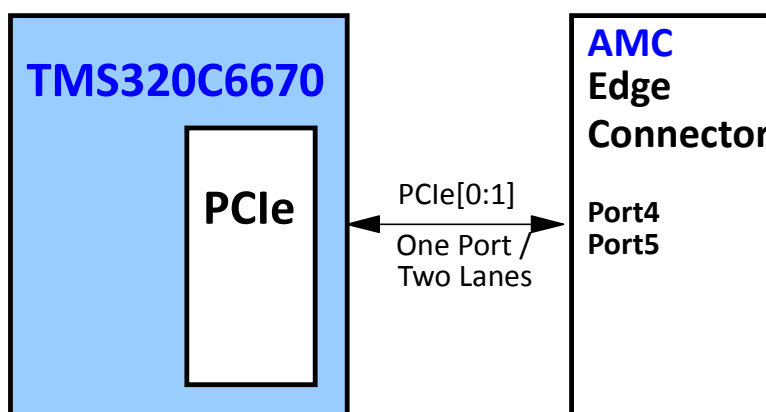


Figure 2.9: TMDXEVM6670L EVM PCIE Port Connections

2.12 Antenna Interface (AIF2)

The TMS320C6670 supports a high-speed SERDES-based Antenna Interface (AIF2) that operates up to 6.144Gbps. A six-lane SerDes-based Antenna Interface is available on the TMDXEVM6670. All Antenna Interface ports are routed to the AMC edge connector on the board.

Below figure shows the AIF connections on the TMDXEVM6670L EVM.

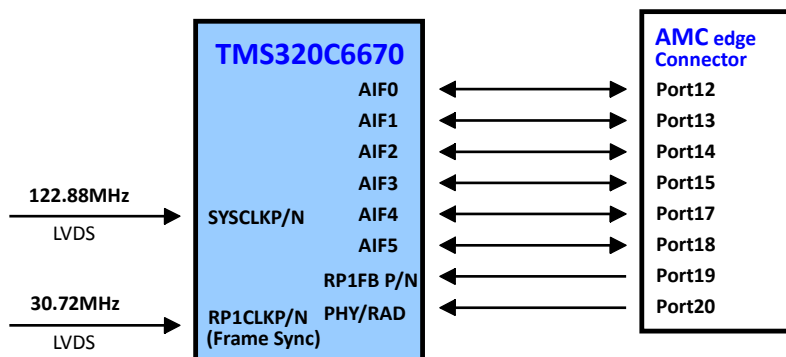


Figure 2.10: TMDXEVM6670L EVM AIF Port Connections

2.13 UART Interface

A serial port is provided for UART communication by the TMS320C6670. This serial port can be accessed either through the USB connector (USB1) or through the three-pin (Tx, Rx, and GND) serial port header (COM1). The selection can be made through the UART Route Select shunt-post COM_SEL1 as follows:

- UART over mini-USB Connector - Shunts installed over COM_SEL1.3- COM_SEL1.1 and COM_SEL1.4 - COM_SEL1.2 **(Default)**
- UART over 3-Pin Header (COM1) - Shunts installed over COM_SEL1.3- COM_SEL1.5 and COM_SEL1.4 –COM_SEL1.6

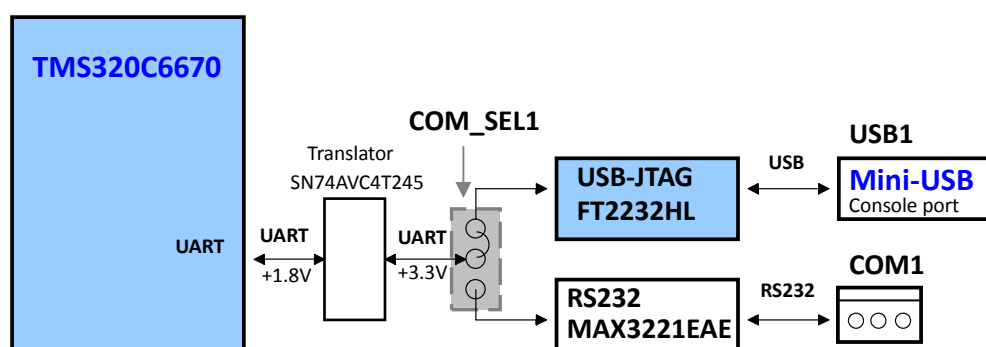


Figure 2.11: TMDXEVM6670L EVM UART Connections

2.14 Module Management Controller (MMC) for IPMI

The TMDXEVM6670L supports a limited set of Intelligent Platform Management Interface (IPMI) commands using the Module Management Controller (MMC) based on Texas Instruments MSP430F5435 mixed-signal processor.

The MMC communicates with the MicroTCA Carrier Hub (MCH) over the IPMB (Intelligent Platform Management Bus) when inserted into an AMC slot of a PICMG® MTCA.0 R1.0-compliant chassis. The primary purpose of the MMC is to provide necessary information to the MCH, to enable the payload power to the TMDXEVM6670L EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED (D2) and Red LED (D1) on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of the initialization process when the MMC receives management power.

Blue LED (D2):

The blue LED comes ON when MicroTCA chassis is powered ON and an EVM is inserted into it. The blue LED goes OFF when payload power is enabled to the EVM by the MCH.

Red LED (D1):

Red colored (D1) will normally be OFF. It will turn ON to provide basic feedback about failures and out of service.

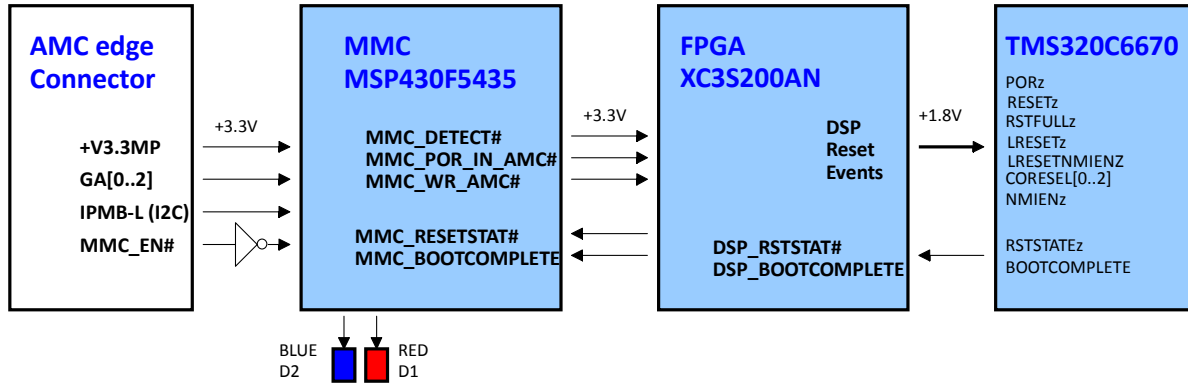


Figure 2.12: TMDXEV6670L EVM MMC Connections for IPMI

2.15 Expansion Headers

The TMDXEV6670L contains an 80-pin header (TEST_PH1) which has I²C, TIMI[0:1], TIMO[0:1], SPI, GPIO[15:0], and UART signal connections. It should be noted that I²C, TIMI[1:0], TIMO[0:1], and SPI GPIO[15:0] connections to this header (TEST_PH1) are 1.8 V whereas UART signals are 3.3 V level.

3. TMDXEVM6670L Board Physical Specifications

This chapter describes the physical layout of the TMDXEVM6670L board and its connectors, switches, and test points. It contains:

3.1 Board Layout

3.2 Connector Index

3.3 Switches

3.4 Test Points

3.5 System LEDs

3.1 Board Layout

The TMDXEVM6670L board dimension is 7.11" x 2.89" (180.6mm x 73.5mm). It is a 12-layer board and powered through connector DC_IN1. Figure 3.1 and 3.2 show assembly layout of the TMDXEVM6670L EVM Board.

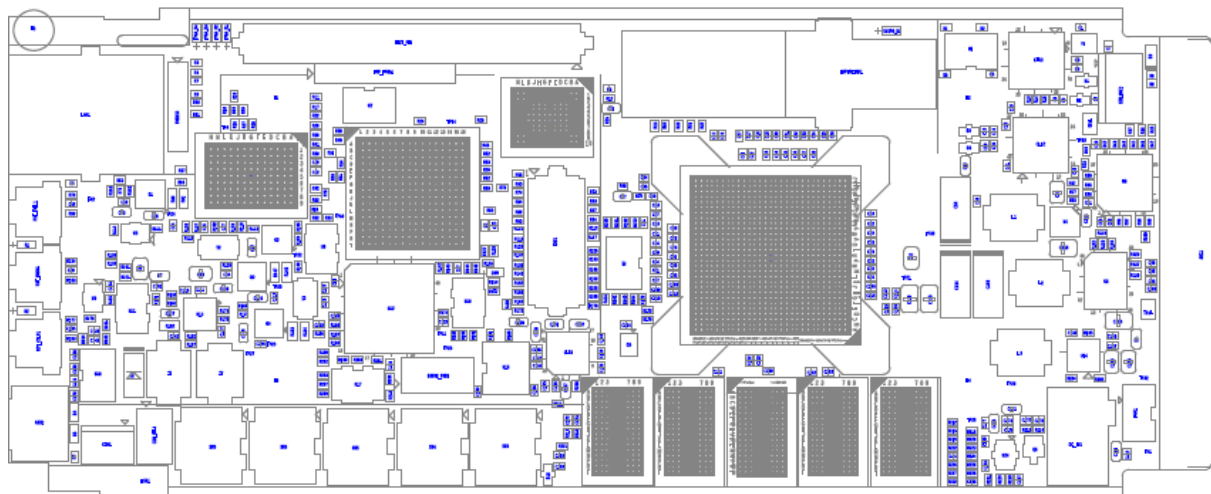


Figure 3.1: TMDXEVM6670L EVM Board Assembly Layout – TOP view

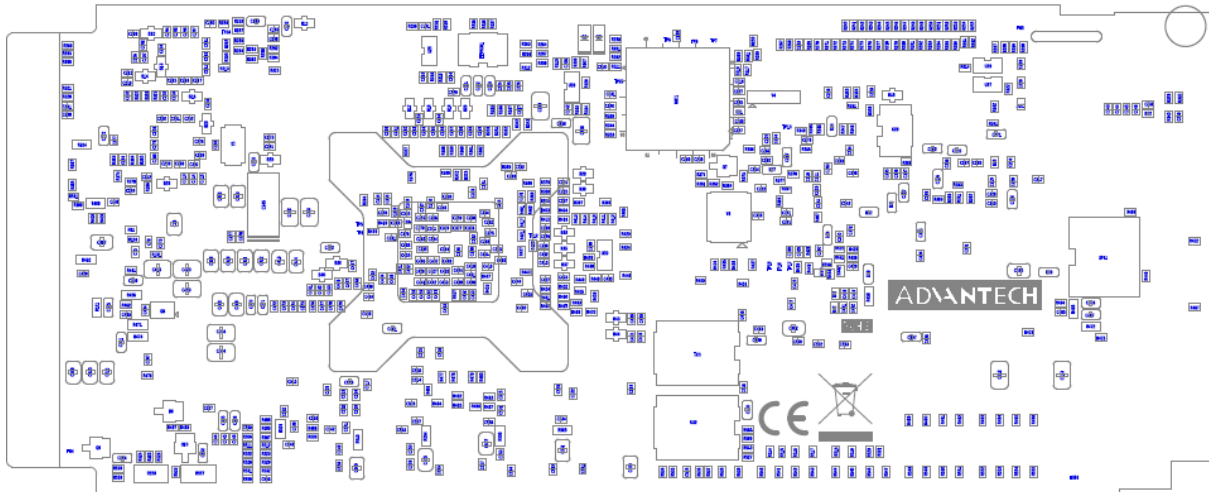


Figure 3.2: TMDXEVM6670L EVM Board layout – Bottom view

3.2 Connector Index

The TMDXEVM6670L Board has several connectors that provide access to various interfaces on the board.

Table 3.1: TMDXEVM6670L EVM Board Connectors

| Connector | Pins | Function |
|------------|------|--|
| 560V2_PWR1 | 8 | XDS560v2 Mezzanine Power Connector |
| AMC1 | 170 | AMC Edge Connector |
| COM1 | 3 | UART 3-Pin Connector |
| COM_SEL1 | 6 | UART Route Select Jumper |
| DC_IN1 | 3 | DC Power Input Jack Connector |
| EMU1 | 60 | TI 60-Pin DSP JTAG Connector |
| FAN1 | 3 | FAN connector for +12V DC FAN |
| HyperLink1 | 36 | HyperLink connector for companion chip/die interface |
| LAN1 | 12 | Gigabit Ethernet RJ-45 Connector |
| PMBUS1 | 5 | PMBUS for Smart-Reflex connected to UCD9222 |
| TAP_FPGA1 | 8 | FPGA JTAG Connector |
| SBW_MMC1 | 4 | MSP430 Spy-Bi-Wire Connector -- For Factory Use Only |
| TEST_PH1 | 80 | SPI, I ² C, GPIO, TIMI[1:0], TIMO[1:0], and UART1 connections |
| USB1 | 5 | Mini-USB Connector |

3.2.1 560V2_PWR1, XDS560v2 Mezzanine Power Connector

560V2_PWR1 is an 8-pin power connector for the XDS560v2 mezzanine emulator board. The pin out of the connector is shown in the table below:

Table 3.2: XDS560v2 Power Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | +5VSupply |
| 2 | +5VSupply |
| 3 | XDS560V2_IL |
| 4 | Ground |
| 5 | +3.3VSupply |
| 6 | +3.3VSupply |
| 7 | Ground |
| 8 | Ground |

3.2.2 AMC1, AMC Edge Connector

The AMC card-edge connector plugs into an AMC compatible carrier board and provides 4 Serial RapidIO lanes, 2 PCIe lanes, 1 SGMII port, 6 AIF2 lanes and the system interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below:

Table 3.3: AMC Edge Connector

| Pin | Signal | Pin | Signal |
|-----|-------------------|-----|-------------------|
| 1 | GND | 170 | GND |
| 2 | VCC12 | 169 | AMC_JTAG_TDI |
| 3 | MMC_PS_N1# | 168 | AMC_JTAG_TDO |
| 4 | VCC3V3_MP_AMC | 167 | AMC_JTAG_RST# |
| 5 | MMC_GA0 | 166 | AMC_JTAG_TMS |
| 6 | RSVD | 165 | AMC_JTAG_TCK |
| 7 | GND | 164 | GND |
| 8 | RSVD | 163 | AMC_RP1CLKP |
| 9 | VCC12 | 162 | AMC_RP1CLKN |
| 10 | GND | 161 | GND |
| 11 | AMC0_SGMII0_TX_DP | 160 | AMC_EXP_SCL |
| 12 | AMC0_SGMII0_TX_DP | 159 | AMC_EXP_SDA |
| 13 | GND | 158 | GND |
| 14 | AMC0_SGMII0_RX_DP | 157 | RP1FBP |
| 15 | AMC0_SGMII0_RX_DN | 156 | RP1FBN |
| 16 | GND | 155 | GND |
| 17 | MMC_GA1 | 154 | PHYSYNC |
| 18 | VCC12 | 153 | RADSYNC |
| 19 | GND | 152 | GND |
| 20 | NC | 151 | AMCC_P18_AIF5_TXP |
| 21 | NC | 150 | AMCC_P18_AIF5_TXN |
| 22 | GND | 149 | GND |
| 23 | NC | 148 | AMCC_P18_AIF5_RXP |
| 24 | NC | 147 | AMCC_P18_AIF5_RXN |

| Pin | Signal | Pin | Signal |
|-----|--------------------|-----|--------------------|
| 25 | GND | 146 | GND |
| 26 | MMC_GA2 | 145 | AMCC_P17_AIF4_TXP |
| 27 | VCC12 | 144 | AMCC_P17_AIF4_TXN |
| 28 | GND | 143 | GND |
| 29 | NC | 142 | AMCC_P17_AIF4_RXP |
| 30 | NC | 141 | AMCC_P17_AIF4_RXN |
| 31 | GND | 140 | GND |
| 32 | NC | 139 | TCLKD_P |
| 33 | NC | 138 | TCLKD_N |
| 34 | GND | 137 | GND |
| 35 | NC | 136 | TCLKC_P |
| 36 | NC | 135 | TCLKC_N |
| 37 | GND | 134 | GND |
| 38 | NC | 133 | AMCC_P15_AIF3_TXP |
| 39 | NC | 132 | AMCC_P15_AIF3_TXN |
| 40 | GND | 131 | GND |
| 41 | MMC_ENABLE_N | 130 | AMCC_P15_AIF3_RXP |
| 42 | VCC12 | 129 | AMCC_P15_AIF3_RXN |
| 43 | GND | 128 | GND |
| 44 | AMCC_P4_PCl_e_TX1P | 127 | AMCC_P14_AIF2_TXP |
| 45 | AMCC_P4_PCl_e_TX1N | 126 | AMCC_P14_AIF2_TXN |
| 46 | GND | 125 | GND |
| 47 | AMCC_P4_PCl_e_RX1P | 124 | AMCC_P14_AIF2_RXP |
| 48 | AMCC_P4_PCl_e_RX1N | 123 | AMCC_P14_AIF2_RXN |
| 49 | GND | 122 | GND |
| 50 | AMCC_P5_PCl_e_TX2P | 121 | AMCC_P13_AIF1_TXP |
| 51 | AMCC_P5_PCl_e_TX2N | 120 | AMCC_P13_AIF1_TXN |
| 52 | GND | 119 | GND |
| 53 | AMCC_P5_PCl_e_RX2P | 118 | AMCC_P13_AIF1_RXP |
| 54 | AMCC_P5_PCl_e_RX2N | 117 | AMCC_P13_AIF1_RXN |
| 55 | GND | 116 | GND |
| 56 | SMB_SCL_IPMBL | 115 | AMCC_P12_AIF0_TXP |
| 57 | VCC12 | 114 | AMCC_P12_AIF0_TXN |
| 58 | GND | 113 | GND |
| 59 | NC | 112 | AMCC_P12_AIF0_RXP |
| 60 | NC | 111 | AMCC_P12_AIF0_RXN |
| 61 | GND | 110 | GND |
| 62 | NC | 109 | AMCC_P11_SRIO4_TXP |
| 63 | NC | 108 | AMCC_P11_SRIO4_TXN |
| 64 | GND | 107 | GND |
| 65 | NC | 106 | AMCC_P11_SRIO4_RXP |
| 66 | NC | 105 | AMCC_P11_SRIO4_RXN |
| 67 | GND | 104 | GND |
| 68 | NC | 103 | AMCC_P10_SRIO3_TXP |
| 69 | NC | 102 | AMCC_P10_SRIO3_TXN |

| Pin | Signal | Pin | Signal |
|-----|----------------|-----|--------------------|
| 70 | GND | 101 | GND |
| 71 | SMB_SDA_IPMBL | 100 | AMCC_P10_SRIO3_RXP |
| 72 | VCC12 | 99 | AMCC_P10_SRIO3_RXN |
| 73 | GND | 98 | GND |
| 74 | TCLKA_P | 97 | AMCC_P9_SRIO2_TXP |
| 75 | TCLKA_N | 96 | AMCC_P9_SRIO2_TXN |
| 76 | GND | 95 | GND |
| 77 | TDM_CLKB_P | 94 | AMCC_P9_SRIO2_RXP |
| 78 | TDM_CLKB_N | 93 | AMCC_P9_SRIO2_RXN |
| 79 | GND | 92 | GND |
| 80 | PCIE_REF_CLK_P | 91 | AMCC_P8_SRIO1_TXP |
| 81 | PCIE_REF_CLK_N | 90 | AMCC_P8_SRIO1_TXN |
| 82 | GND | 89 | GND |
| 83 | MMC_PS_N0 | 88 | AMCC_P8_SRIO1_RXP |
| 84 | VCC12 | 87 | AMCC_P8_SRIO1_RXN |
| 85 | GND | 86 | GND |

3.2.3 COM1, UART 3-Pin Connector

COM1 is a 3-pin male connector for RS232 serial interface. A 3-pin female to 9-pin DTE female cable is supplied with the TMDXEVM6670L to connect with the PC.

Table 3.4: UART Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | Receive |
| 2 | Transmit |
| 3 | Ground |

3.2.4 COM_SEL1, UART Route Select Connector

The UART port can be accessed through the mini-USB connector (USB1) or the three-pin RS232 Serial port header (COM1). The selection can be made through the UART route select connector COM_SEL1 as follows:

- UART over USB Connector(**Default**): Shunts installed over COM_SEL1.3-COM_SEL1.1 and COM_SEL1.4-COM_SEL1.2
- UART over three-pin Header LAN1-Shunts installed over COM_SEL1.3-COM_SEL1.5 and COM_SEL1.4-COM_SEL1.6

The pin out for the connector is shown in the table below:

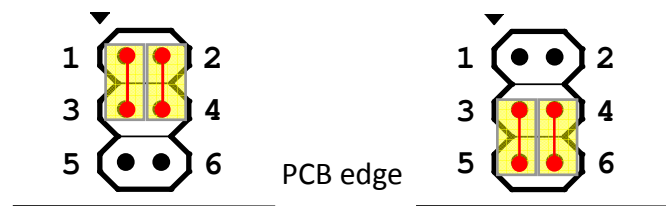
Table 3.5: UART Path Select Connector pin out

| Pin # | Signal Name | Pin # | Signal Name |
|-------|--------------------------------|-------|-------------------------------|
| 1 | FT2232H (USB Chip) Transmit | 2 | FT2232H (USB Chip) Receive |
| 3 | UART Transmit | 4 | UART Receive |
| 5 | MAX3221 Transmit | 6 | MAX3221 Receive |

Figure 3.3: COM_SEL1 Jumper setting

Wire pin1-3 and pin2-4
UART over the XDS100v1

Wire pin3-5 and pin4-6
UART over the 3-pin terminal



3.2.5 DC_IN1, DC Power Input Jack Connector

DC_IN1 is a DC Power-in jack Connector for the stand-alone application of TMDXEVM6670L. It is a 2.5 mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into the MicroTCA chassis or the AMC carrier backplane.

3.2.6 EMU1, TI 60-Pin DSP JTAG Connector

EMU1 is a high speed system trace capable TI 60-pin JTAG connector for XDS560v2 type of DSP emulation. The on board switch multiplexes this interface with the on board XDS100 type emulator. Whenever an external emulator is plugged into EMU1, the external emulator connection will be switched to the DSP. The I/O voltage level on these pins is 1.8 V. So any 1.8V compatible emulator can be used to interface with the TMS320C6670 DSP. It should be noted that when an external emulator is plugged into this connector (EMU1), on board XDS100 type emulation circuitry will be disconnected from the DSP. The pin out for the connector is shown in the table below:

Table 3.6: TI 60-pin DSP JTAG Connector pin out

| Pin # | Signal Name | Pin # | Signal Name |
|-------|-------------|-------|-------------|
| A1 | EMU_DET | C1 | ID2 (GND) |
| A2 | Ground | C2 | EMU18 |
| A3 | Ground | C3 | TRST# |
| A4 | Ground | C4 | EMU16 |
| A5 | Ground | C5 | EMU15 |
| A6 | Ground | C6 | EMU13 |
| A7 | Ground | C7 | EMU11 |
| A8 | Type0 (NC) | C8 | TCLKRTN |
| A9 | Ground | C9 | EMU10 |
| A10 | Ground | C10 | EMU8 |
| A11 | Ground | C11 | EMU6 |
| A12 | Ground | C12 | EMU4 |
| A13 | Ground | C13 | EMU3 |
| A14 | Ground | C14 | EMU1 |
| A15 | TRGRST# | C15 | ID3 (GND) |
| B1 | ID0 (GND) | D1 | NC |
| B2 | TMS | D2 | Ground |
| B3 | EMU17 | D3 | Ground |
| B4 | TDI | D4 | Ground |
| B5 | EMU14 | D5 | Ground |
| B6 | EMU12 | D6 | Ground |
| B7 | TDO | D7 | Ground |
| B8 | TVD (+1.8V) | D8 | Type1 (GND) |
| B9 | EMU9 | D9 | Ground |
| B10 | EMU7 | D10 | Ground |
| B11 | EMU5 | D11 | Ground |
| B12 | TCLK | D12 | Ground |
| B13 | EMU2 | D13 | Ground |
| B14 | EMU0 | D14 | Ground |
| B15 | ID1 (GND) | D15 | Ground |

3.2.7 FAN1, FAN Connector

The EVM incorporates a dedicated cooling fan. This fan has the capability of easily being removed when the EVM is inserted into an AMC backplane which uses forced air cooling. The fan selected provides maximum cooling (CFM) and operates on 12Vdc. FAN1 will be connected to provide 12Vdc to the fan.

Table 3.7: FAN1 Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | GND |
| 2 | +12Vdc |
| 3 | NC |

3.2.8 HyperLink1, HyperLink Connector

The EVM provides a HyperLink connection by a mini-SAS HD+ 4i connector. The connector contains 8 SERDES pairs and 4 sideband sets to carry full HyperLink signals. The connector is shown in Figure 3.4. and its pin out is shown in Table 3.8.

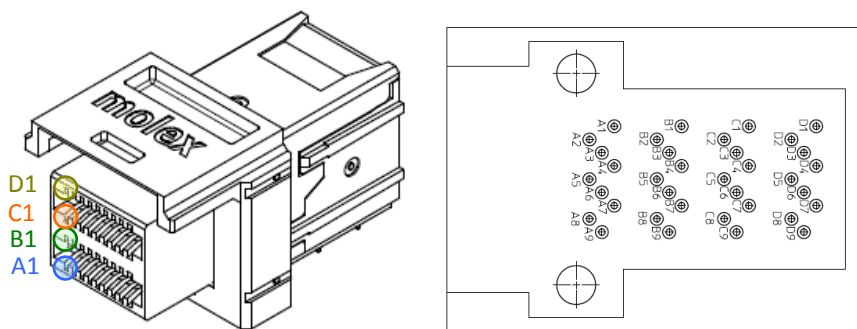


Figure 3.4: The HyperLink Connector

Table 3.8: The HyperLink Connector

| Pin# | Net | Pin# | Net |
|------|-------------------|------|-------------------|
| A1 | HyperLink_TXFLCLK | B1 | HyperLink_RXPMDAT |
| A2 | HyperLink_RXFLCLK | B2 | HyperLink_TXFLDAT |
| A3 | GND | B3 | GND |
| A4 | HyperLink_RXP1 | B4 | HyperLink_RXP0 |
| A5 | HyperLink_RXN1 | B5 | HyperLink_RXN0 |
| A6 | GND | B6 | GND |
| A7 | HyperLink_RXP3 | B7 | HyperLink_RXP2 |
| A8 | HyperLink_RXN3 | B8 | HyperLink_RXN2 |
| A9 | GND | B9 | GND |
| C1 | HyperLink_TXPMDAT | D1 | HyperLink_RXPMCLK |
| C2 | HyperLink_TXPMCLK | D2 | HyperLink_RXFLDAT |
| C3 | GND | D3 | GND |
| C4 | HyperLink_TXP1 | D4 | HyperLink_TXP0 |
| C5 | HyperLink_TXN1 | D5 | HyperLink_TXN0 |
| C6 | GND | D6 | GND |
| C7 | HyperLink_TXP3 | D7 | HyperLink_TXP2 |
| C8 | HyperLink_TXN3 | D8 | HyperLink_TXN2 |
| C9 | GND | D9 | GND |

3.2.9 LAN1, Ethernet Connector

LAN1 is a Gigabit RJ45 Ethernet connector with integrated magnetics. It is driven by Marvell Gigabit Ethernet transceiver 88E1111. The connections are shown in the table below:

Table 3.9: Ethernet Connector pin out

| Pin # | Signal Name |
|-------|----------------|
| 1 | Center Tap2 |
| 2 | MD2- |
| 3 | MD2+ |
| 4 | MD1- |
| 5 | MD1+ |
| 6 | Center Tap1 |
| 7 | Center Tap3 |
| 8 | MD3+ |
| 9 | MD3- |
| 10 | MD0- |
| 11 | MD0+ |
| 12 | Center Tap0 |
| 13 | ACT_LED1- |
| 14 | ACT_LED1+ |
| 15 | LINK1000_LED2- |
| 16 | LINK_LED2+ |
| 17 | LINK100_LED2- |
| H3 | Shield 1 |
| H4 | Shield 2 |

3.2.10 PMBUS1, PMBUS Connector for Smart-Reflex Control

The TMS320C6670 DSP core power is supplied by a Smart-Reflex power controller UCD9222 with the Integrated FET Driver UCD74110 and UCD74106. PMBUS1 provides a connection between UCD9222 and remote connection during development. Through the USB to GPIO pod provided by TI, the user can trace and configure the parameters in UCD9222 with the Smart-Fusion GUI. The pin out of PMBUS1 is shown in table 3.10.

Table 3.10: PMBUS1 Pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | PMBUS_CLK |
| 2 | PMBUS_DAT |
| 3 | PMBUS_ALT |
| 4 | PMBUS_CTL |
| 5 | GND |

3.2.11 TAP_FPGA1, FPGA JTAG Connector (For Factory Use Only)

TAP_FPGA1 is an 8-pin JTAG connector for the FPGA programming and the PHY boundary test of the factory only. The pin out for the connector is shown in the figure below:

Table 3.11: FPGA JTAG Connector pin out

| Pin # | Signal Name |
|-------|-----------------|
| 1 | VCC3V3_FPGA |
| 2 | GND |
| 3 | BSC_JTAG_TCK |
| 4 | BSC_JTAG_TDI |
| 5 | BSC_JTAG_TDO |
| 6 | BSC_JTAG_TMS |
| 7 | BSC_JTAG_RST# |
| 8 | BSC_JTAG_P8(PU) |

In FPGA debugging and programming mode, pin 8 of BSC_JTAG_P8 keep as PU pin to the EVM board.

The diagram of the boundary scan route is shown in Figure 3.4.

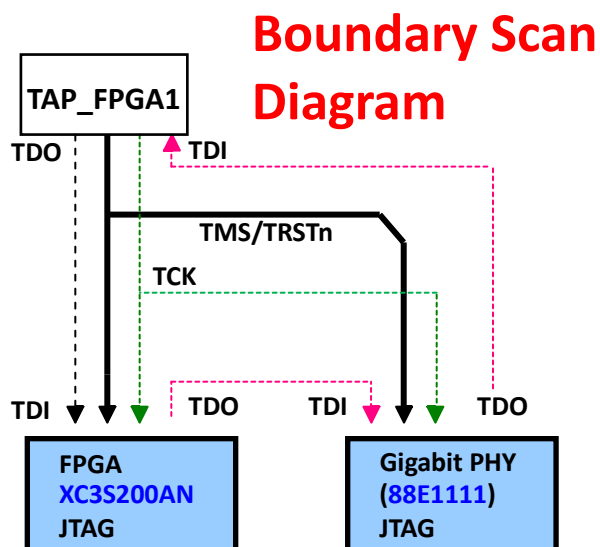


Figure 3.5: TAP_FPGA1 function diagram

3.2.12 SBW_MMC1, MSP430 SpyBiWire Connector (For Factory Use Only)

SBW_MMC1 is a 4-pin SpyBiWire connector for IPMI software loading into MSP430. The TMDXEVM6670L is supplied with IPMI software already loaded into MSP430. The pin out of the connector is shown in the table below:

Table 3.12: MSP430 SpyBiWire Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | GND |
| 2 | VCC3V3_MP |
| 3 | MMC_SBWTDIO |
| 4 | MMC_SBWTK |

3.2.13 TEST_PH1, Expansion Header (SPI, GPIO, Timer I/O, I²C, and UART)

TEST_PH1 is an expansion header for several interfaces on the DSP; there are SPI, GPIO, Timer, I²C, and UART. The signal connections to the expansion header are shown in below table:

Table 3.13: TEST_PH1, The Expansion Header pin out

| Pin | Signal | Description | Pin | Signal | Description |
|-----|---------|---------------|-----|--------|-------------|
| 1 | GND | Ground | 2 | NC | |
| 3 | DSP_SDA | DSP I2C data | 4 | NC | |
| 5 | DSP_SCL | DSP I2C clock | 6 | NC | |
| 7 | NC | | 8 | NC | |
| 9 | NC | | 10 | NC | |
| 11 | NC | | 12 | NC | |
| 13 | NC | | 14 | NC | |
| 15 | NC | | 16 | NC | |
| 17 | NC | | 18 | NC | |
| 19 | NC | | 20 | NC | |
| 21 | NC | | 22 | NC | |
| 23 | NC | | 24 | NC | |
| 25 | NC | | 26 | NC | |
| 27 | NC | | 28 | NC | |
| 29 | NC | | 30 | NC | |
| 31 | NC | | 32 | NC | |
| 33 | NC | | 34 | NC | |
| 35 | NC | | 36 | NC | |
| 37 | NC | | 38 | NC | |
| 39 | NC | | 40 | NC | |
| 41 | NC | | 42 | NC | |

| | | | | | |
|----|-------------|------------------------------|----|-------------|------------|
| 43 | NC | | 44 | NC | |
| 45 | NC | | 46 | NC | |
| 47 | NC | | 48 | NC | |
| 49 | NC | | 50 | DSP_GPIO_00 | DSP GPIO0 |
| 51 | NC | | 52 | DSP_GPIO_01 | DSP GPIO1 |
| 53 | NC | | 54 | DSP_GPIO_02 | DSP GPIO2 |
| 55 | DSP_TIMI0 | Timer input 0 | 56 | DSP_GPIO_03 | DSP GPIO3 |
| 57 | DSP_TIMO0 | Timer output 0 | 58 | DSP_GPIO_04 | DSP GPIO4 |
| 59 | DSP_TIMI1 | Timer input 1 | 60 | DSP_GPIO_05 | DSP GPIO5 |
| 61 | DSP_TIMO1 | Timer output 1 | 62 | DSP_GPIO_06 | DSP GPIO6 |
| 63 | DSP_SSPMISO | SPI data input | 64 | DSP_GPIO_07 | DSP GPIO7 |
| 65 | DSP_SSPMOSI | SPI data output | 66 | DSP_GPIO_08 | DSP GPIO8 |
| 67 | DSP_SSPCS1 | SPI chip select | 68 | DSP_GPIO_09 | DSP GPIO9 |
| 69 | PH_SSPCK | SPI clock | 70 | DSP_GPIO_10 | DSP GPIO10 |
| 71 | DSP_UARTTXD | UART Serial Data Out(+3.3v) | 72 | DSP_GPIO_11 | DSP GPIO11 |
| 73 | DSP_UARTRXD | UART Serial Data In (+3.3v) | 74 | DSP_GPIO_12 | DSP GPIO12 |
| 75 | DSP_UARTRTS | UART Request To Send (+3.3v) | 76 | DSP_GPIO_13 | DSP GPIO13 |
| 77 | DSP_UARTCTS | UART Cear To Send (+3.3v) | 78 | DSP_GPIO_14 | DSP GPIO14 |
| 79 | GND | Ground | 80 | DSP_GPIO_15 | DSP GPIO15 |

3.2.14 USB1, Mini-USB Connector

USB1 is a five-pin mini-USB connector to connect Code Composer Studio with the TMS320C6670 DSP using XDS100 type on-board emulation circuitry. The following table shows the Pin out of the mini-USB connector.

Table 3.14: Mini-USB Connector pin out

| Pin # | Signal Name |
|-------|-------------|
| 1 | VBUS |
| 2 | USB D- |
| 3 | USB D+ |
| 4 | ID (NC) |
| 5 | Ground |

3.3 DIP and Pushbutton Switches

The TMDXEVM6670L has 3 push button switches and 5 sliding actuator DIP switches. The RST_FULL1, RST_COLD1, and RST_WARM1 are push button switches while SW3, SW4, SW5, SW6 and SW9 are DIP switches. The function of each of the switches is listed in the table below:

Table 3.15: TMDXEVM6670L EVM Board Switches

| Switch | Function |
|-----------|---|
| RST_FULL1 | Full Reset Event |
| RST_COLD1 | Cold Reset Event (RFU) |
| RST_WARM1 | Warm Reset Event |
| SW3 | DSP Boot mode, DSP Configuration |
| SW4 | DSP boot Configuration |
| SW5 | DSP boot Configuration |
| SW6 | DSP boot Configuration, PLL setting, PCIe mode Selection |
| SW9 | PCIESS Enable/Disable, User Switch DSPCLKSEL and PASSCLKSEL |

3.3.1 RST_FULL1, Full Reset

Pressing the RST_FULL1 button switch will issue a RESETFULL# to TMS320C6670 by the FPGA. It'll reset DSP and other peripherals.

3.3.2 RST_COLD1, Cold Reset

The button is reserved for future use.

3.3.3 RST_WARM1, Warm Reset

Pressing the RST_WARM1 button switch will issue a RESET# to TMS320C6670 by the FPGA. The FPGA will assert the RESET# signal to the DSP and the DSP will execute either a HARD or SOFT resets by the configuration in the RSCFG register in PLLCTL.

Note: Users may refer to the [TMS320C6670 Data Manual](#) to check the difference between assertion of DSP RESET# and DSP POR# signals.

3.3.4 SW3, SW4, SW5 and SW6 DSP Boot Configurations

SW3, SW4, SW5, and SW6 are four-position DIP switches, which are used for DSP ENDIAN, Boot Device, Boot Configuration, and PCI Express subsystem configuration.

For the details about the DSP Boot modes and their configuration, please refer to the

The diagram of the default setting on these switches is shown below:

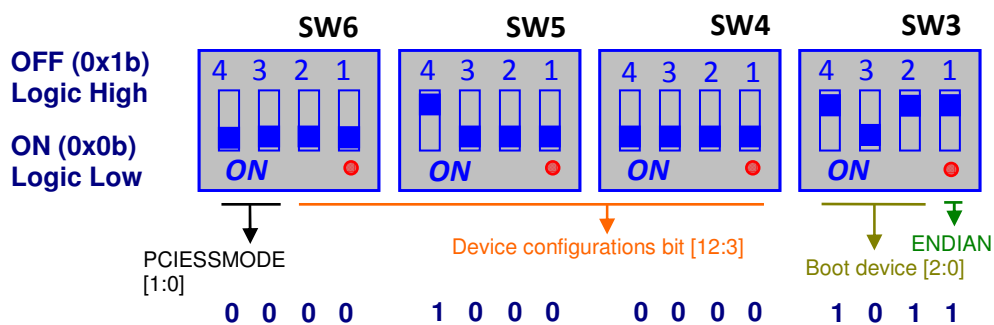


Figure 3.6: SW3, SW4, SW5, and SW6 default settings

The following table describes the positions and corresponding functions on SW.

Table 3.16: SW3-SW6, DSP Configuration Switch

| SW3 | Description | Default Value | Function |
|--------------------|--|--------------------------------|---|
| SW3[1] | ENDIAN | 0x1b (OFF) | Device endian mode (LENDIAN). 0 = Device operates in big endian mode 1 = Device operates in little endian mode |
| SW3[4:2] | Boot device Bit[2:0] | 0x101b (OFF,ON,OFF) | Boot Device 000b = None 001b = Serial Rapid I/O 010b = SGMII (PA driven from core clk) 011b = SGMII (PA driver from PA clk) 100b = PCI Express 101b = I2C 110b = SPI 111b = HyperLink |
| SW5[1] SW4[4:1] | Parameter Index [4:0] / Boot Mode [7:3] | 00000b (ON,ON,ON, ON,ON) | These 5 bits are the Parameter Index when I2C is the boot device. They have other definitions for other boot devices. For the details about the device configuration, For the details about the device configuration, please refer to the TMS320C6670 Data Manual . |
| SW5[2] | Mode / Boot Mode [8] | 0 (ON) | Mode (I2C Boot Device) 0 = Master 1 = Slave |
| SW5[3] | Reserved / Boot Mode [9] | 0 (ON) | Bit reserved with I2C Boot Device |
| SW5[4] | Address / Boot Mode [10] | 1 (OFF) | Address (I2C Boot Device) 0 = Boot from address 0x50 1 = Boot from address 0x51 |

| | | | |
|----------|---------------------------|----------------|---|
| SW6[1] | Speed / Boot Mode [11] | 0 (ON) | Speed (I2C Boot Device) 0 = Low speed 1 = High Speed |
| SW6[2] | Reserved / Boot Mode [12] | 0 (ON) | Bit reserved with I2C Boot Device |
| SW6[4:3] | PCIESSMODE [1:0] | 00b (ON,ON) | PCIe Subsystem mode selection. 00b = PCIe in end point mode 01b = PCIe legacy end point (no support for MSI) 10b = PCIe in root complex mode 11b = Reserved |

3.3.5 SW9, DSP PCIe Enable / User Defined and DSP_DSPCLKSEL / FPGA_PACLKSEL Switch Configuration

SW9 is a 4-position DIP switch. The first position is used for enabling the PCI Express Subsystem within the DSP. The second position is undefined by hardware and available for application software use. The third and fourth positions are used by selecting the PLL sources for CORECLK and PASSCLK of the DSP. A diagram of the SW9 switch (with factory default settings) is shown below:

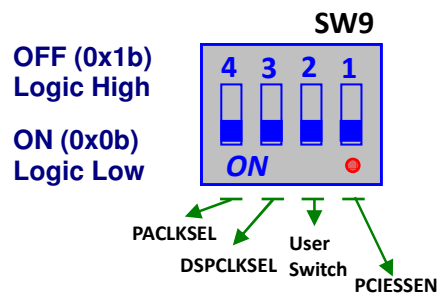


Figure 3.7: SW9 default settings

The following table describes the positions and corresponding functions on SW9.

Table 3.17: SW9, DSP PCIENSEN and User Switch /DSPCLKSEL/PACLKSEL

| SW9 | Description | Default Value | Function |
|--------|-------------|---------------|--|
| SW9[1] | PCIENSEN | 0x0b (ON) | PCIe module enable. 0 = PCIe module disabled 1 = PCIe module enabled |
| SW9[2] | User Switch | 0x0b (ON) | Application software defined |
| SW9[3] | DSPCLKSEL | 0x0b (ON) | CORECLKSEL : RFU, Reserved for Future Use |
| SW9[4] | PACLKSEL | 0x0b (ON) | PACLKSEL : RFU, Reserved for Future Use |

3.4 Test Points

The TMDXEVM6670L EVM Board has 27 test points. The position of each test point is shown in the figures below:

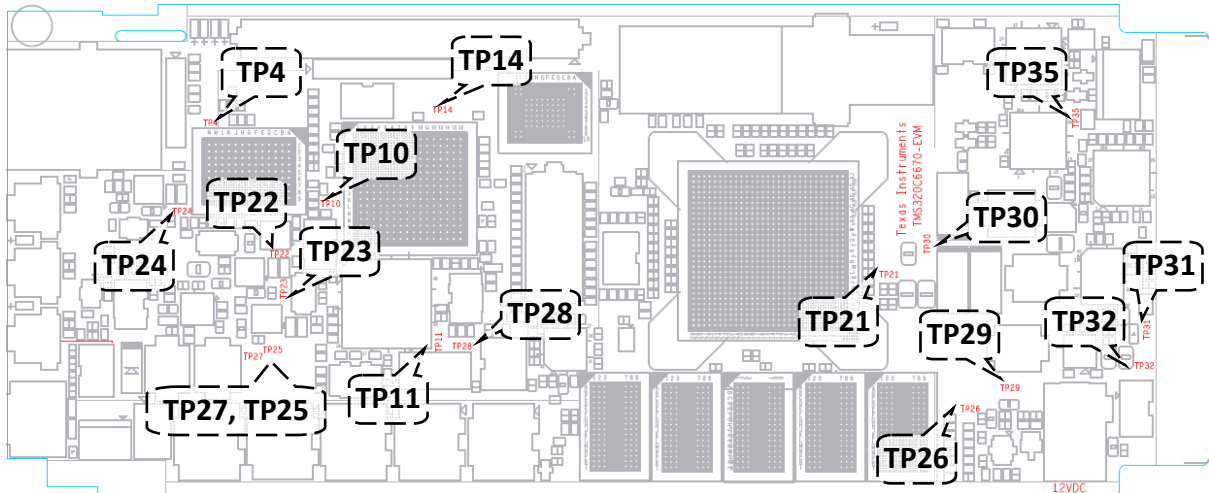


Figure 3.8: TMDXEVM6670L test points on top side

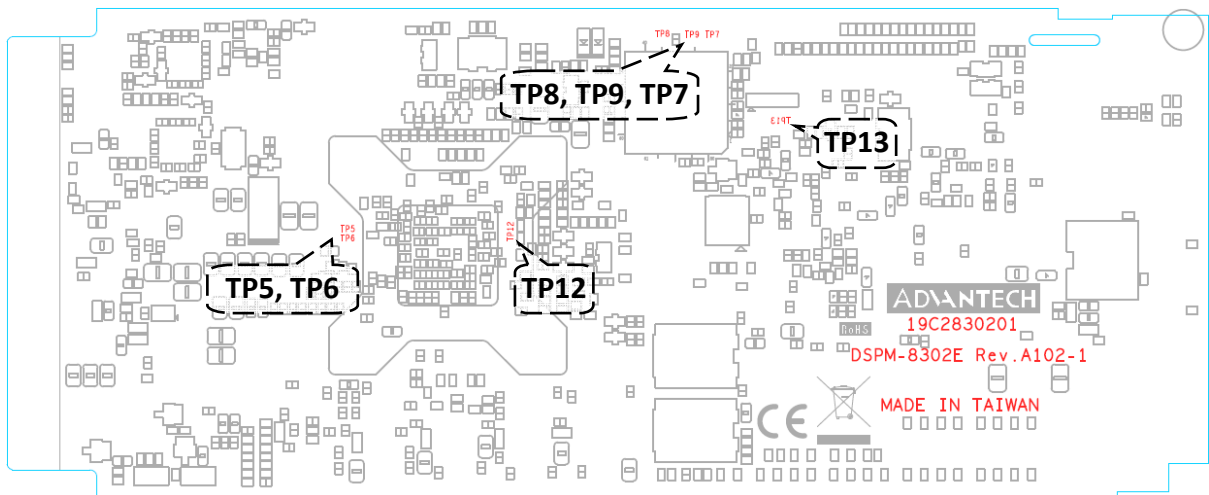


Figure 3.9: TMDXEVM6670L test points on the bottom side

Table 3.18: TMDXEVM6670L EVM Board Test Points

| Test Point | Signal |
|------------|---|
| TP7 | Reserved for MMC1 pin23 |
| TP8 | Reserved for MMC1 pin33 |
| TP9 | Reserved for MMC1 pin25 |
| TP5 | HyperLink_REFCLKOUTP |
| TP6 | HyperLink_REFCLKOUTN |
| TP12 | DSP_SYSCLKOUT |
| TP10 | Reserved for U12 (FT2232) pin60 (PWREN#) |
| TP11 | Reserved for U12 (FT2232) pin36 (SUSPEND#) |
| TP4 | PHY1 (88E1111) 125MHz clock (default: disable) |
| TP13 | Reserved for FPGA1 (XC3S200AN) pin C12 (+1.8V I/O). |
| TP14 | Reserved for FPGA1 (XC3S200AN) pin A13 (+1.8V I/O). |
| TP16 | Reserved for FPGA1 (XC3S200AN) pin T10 (+3.3V I/O). |
| TP17 | Reserved for FPGA1 (XC3S200AN) pin R11 (+3.3V I/O). |
| TP18 | Reserved for FPGA1 (XC3S200AN) pin T11 (+3.3V I/O). |
| TP21 | Test point for CVDD |
| TP22 | Test point for VCC1V2 |
| TP23 | Test point for VCC1V8_AUX |
| TP24 | Test point for VCC2V5 |
| TP25 | Test point for VCC1V8 |
| TP26 | Test point for VCC0V75 |
| TP27 | Test point for VCC3V3_AUX |
| TP28 | Test point for VCC5 |
| TP29 | Test point for VCC1V5 |
| TP30 | Test point for VCC1V0 |
| TP32 | Test point for VCC12 |
| TP31 | GND SHORT PAD |
| TP35 | GND SHORT PAD |

3.5 System LEDs

The TMDXEVM6670L board has 7 LEDs. Their positions on the board are indicated in figure 3.9. The description of each LED is listed in the table below:

Table 3.19: TMDXEVM6670L EVM Board LEDs

| LED# | Color | Description |
|------------|-------|--|
| D1 | Red | Failure and Out of service status in AMC chassis |
| D2 | Blue | Hot Swap status in AMC chassis |
| SYSPG_D1 | Blue | All Power rails are stable on AMC |
| FPGA_D1-D4 | Blue | Debug LEDs. |

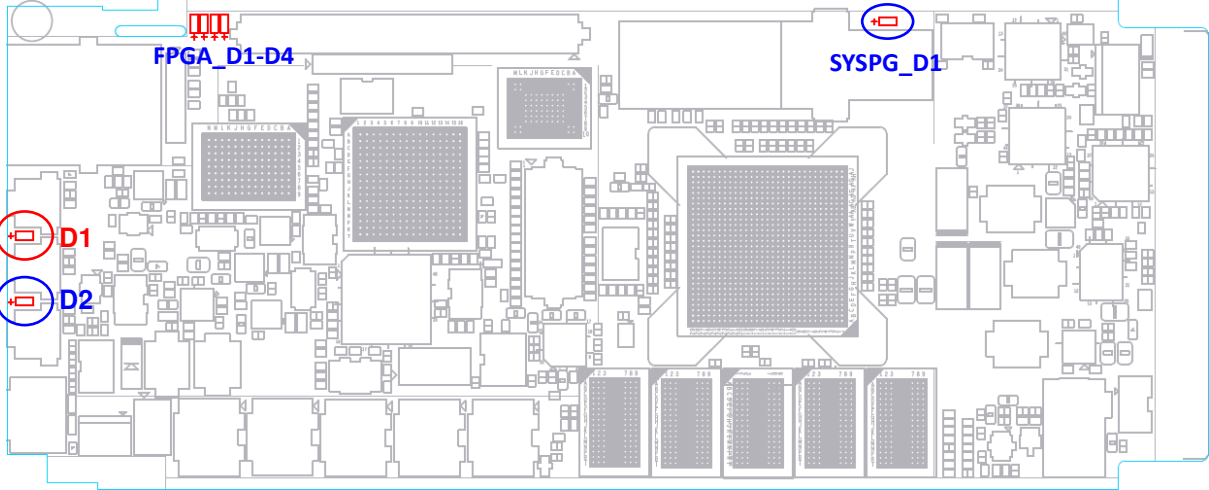


Figure 3.10: TMDXEVM6670L EVM Board LEDs

4. System Power Requirements

This chapter describes the power design of the TMDXEVM6670L board. It contains:

- 4.1 Power Requirements
- 4.2 Power Supply Distribution
- 4.3 Power Supply Boot Sequence

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units.

The maximum EVM power requirements are estimated to be:

- EVM FPGA – 0.65 W;
- DSP Cooling Fans – 1.2 W (+12 VDC/0.1 A);
- Clock Generators & clock sources – 4.95 W;
- DSP – 14.90 W; [worse case]
 - Core: 13.0 W;
 - Peripherals I/O: 1.90 W;
- DDR3 – 2.63 W;
 - 5 SDRAMs to support 64-bit with ECC of DSP
- Misc – 0.33 W;
- USB – 0.84 W;
- SGMII PHY – 1.14 W;

EVM board total: 32.64 W.

The selected AC/DC 12-V adapter should be rated for a minimum of 36 Watts.

The power planes in TMDXEVM6670L are identified in the following table:

Table 4.1: EVM Voltage Table

| Device | Net name | Voltage | Description |
|-----------------|-------------|-------------|---|
| Input | 3.3V_MP_AMC | +3.3 V | Management Power for MMC |
| | VCC12 | +12 V | Payload Power to AMC |
| Management | VCC3V3_AUX | +3.3 V | 3.3 V Power Rail for all support devices on EVM |
| | VCC1V2 | +1.2 V | 1.2 V Power Rail for all support devices on EVM |
| | VCC1V8_AUX | +1.8V | 1.8V Power Rail for all support devices on EVM |
| TMS320C6670 | CVDD | +0.6V~1.10V | DSP Core Power |
| | VCC1V0 | +1.0V | DSP Fixed Core Power |
| | VCC1V8 | +1.8V | DSP I/O power |
| | VCC1V5 | +1.5V | DSP DDR3 and SERDES Power |
| DDR3 Memory | VCC1V5 | +1.5V | DDR3 RAM Power |
| | VCC0V75 | +0.75V | DDR3 RAM Termination Power |
| NAND Flash | VCC1V8 | +1.8V | NAND Flash Power |
| NOR Flash (SPI) | VCC1V8 | +1.8V | SPI NOR Flash Power |
| CDCE62002 | VCC3V3_AUX | +3.3V | Clock Gen Power |
| CDCE62005 | VCC3V3_AUX | +3.3V | Clock Gen Power |
| PHY (88E111) | VCC2V5 | +2.5V | PHY Analog and I/O Power |
| | VCC1V2 | +1.2V | PHY Core Power (instead of 1.0V) |
| USB Emulator | VCC3V3_AUX | +3.3V | USB Emulation Power (FT2232H) |
| | VCC1V8_AUX | +1.8V | USB Emulation Power (FT2232H) |
| MMC (MPS430) | VCC3V3_MP | +3.3V | MMC Power |
| FPGA | VCC1V2 | +1.2V | FPGA Core Power |
| | VCC3V3_AUX | +3.3V | FPGA I/O Power for +3.3V bank |
| | VCC1V8_AUX | +1.8V | FPGA I/O Power for +1.8V bank |
| Misc. Logic | VCC3V3_AUX | +3.3V | Translator and Logic Power |
| | VCC1V8_AUX | +1.8V | Translator and Logic Power |

The following table identifies the expected power requirements for each power plane of the devices on the TMDXEVM6670L EVM.

Table 4.2: Each Current Requirements on each device of EVM board

| TMS320C6670 | V(V) | I(A) | Qty | Pd (W) | |
|---------------|------|-------|-----|--------|-------|
| CVDD (Core) | 1.00 | 9.75 | 1 | 9.75 | 14.88 |
| VCC1V0 (I/O) | 1.00 | 4.52 | 1 | 4.52 | |
| VCC1V8(I/O) | 1.80 | 0.116 | 1 | 0.21 | |
| VCC1V5(I/O) | 1.50 | 0.266 | 1 | 0.40 | |
| DDR3 | V(V) | I(A) | Qty | Pd(W) | |
| VCC1V5 | 1.50 | 0.30 | 5 | 2.25 | 2.63 |
| VCC0V75 | 0.75 | 0.10 | 5 | 0.38 | |
| FPGA | V(V) | I(A) | Qty | Pd(W) | |
| VCC3V3_AUX | 3.30 | 0.03 | 1 | 0.10 | 0.62 |
| VCC1V2 | 1.20 | 0.13 | 1 | 0.16 | |
| VCC1V8_AUX | 1.80 | 0.20 | 1 | 0.36 | |
| XDS560V2 | V(V) | I(A) | Qty | Pd(W) | |
| VCC5 | 5.00 | 1.00 | 1 | 5.00 | 5.99 |
| VCC3V3_AUX | 3.30 | 0.30 | 1 | 0.99 | |
| CDCE62005 | V(V) | I(A) | Qty | Pd(W) | |
| VCC3V3_AUX | 3.30 | 0.50 | 2 | 3.30 | 3.30 |
| CDCE62002 | V(V) | I(A) | Qty | Pd(W) | |
| VCC3V3_AUX | 3.30 | 0.50 | 1 | 1.65 | 1.65 |
| PHY (88E1111) | V(V) | I(A) | Qty | Pd(W) | |
| VCC2V5_AUX | 3.30 | 0.21 | 1 | 0.69 | 1.14 |
| VCC1V2_AUX | 1.80 | 0.25 | 1 | 0.45 | |
| FT2232 | V(V) | I(A) | Qty | Pd(W) | |
| VCC3V3_AUX | 3.30 | 0.21 | 1 | 0.69 | 0.84 |
| VCC1V8_AUX | 1.80 | 0.08 | 1 | 0.14 | |
| MMC (MSP430) | V(V) | I(A) | Qty | Pd(W) | |
| VCC3V3_MP | 3.30 | 0.02 | 1 | 0.07 | 0.07 |

4.2 Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1 as well as on the schematic.

In Figure 4.1, the Auxiliary power rails are always on after payload power is supplied. These regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX
- VCC1V8_AUX
- VCC1V2
- VCC5_AUX

The maximum allowable power is 36 W from the external AC brick supply or from the 8 AMC header pins.

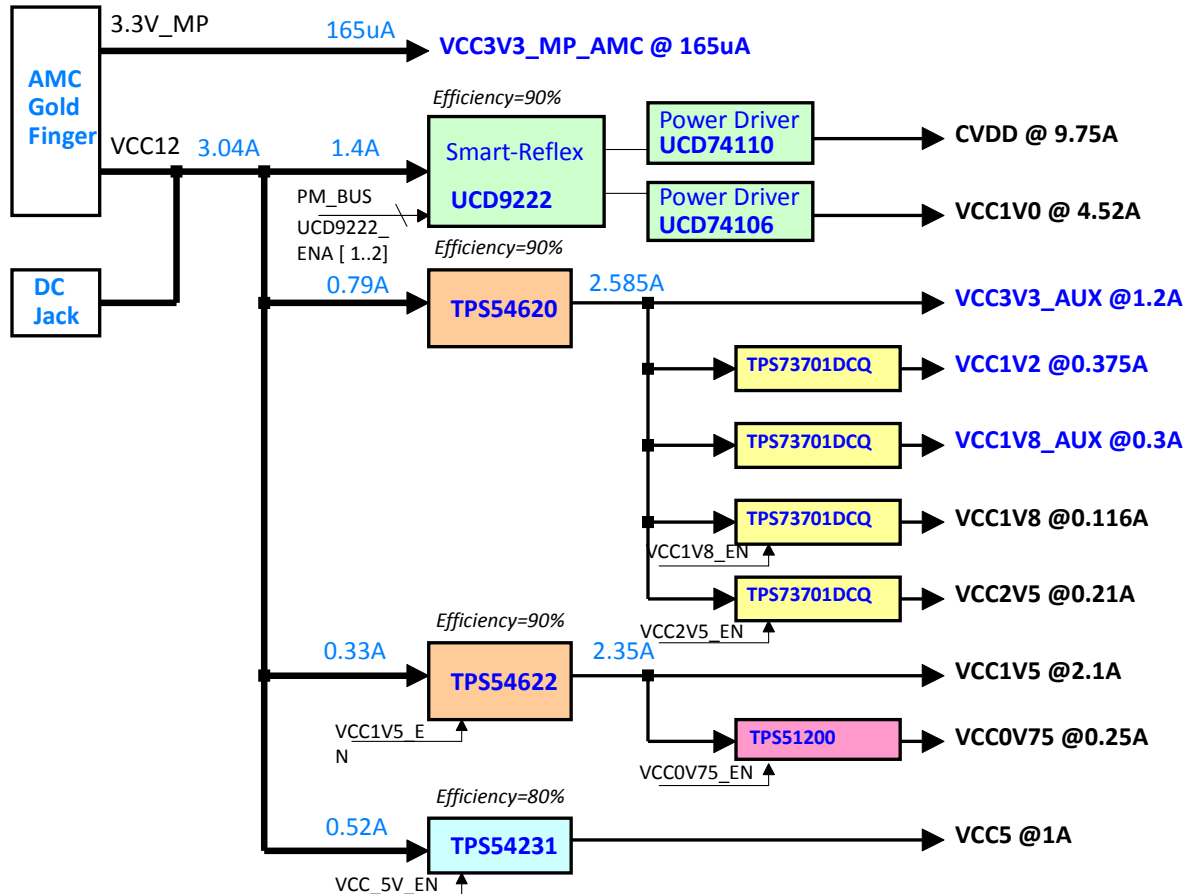


Figure 4.1: All the AMC power supply on TMDXEVM6670L EVM

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (See section 4.3 for specific details). The goal of all power supply designs is to support a minimum temperature range of 0°C to 45°C.

The TMS320C6670 core power is supplied using a dual digital controller coupled to a high performance FET driver IC. Additional DSP supply voltages are provided by discrete TI Swift power supplies. The TMS320C6670 supports a VID interface to enable Smart-Reflex® power supply control for its primary core logic supply. Refer to the TMS320C6670 Data Manual and other documentation for an explanation of the Smart-Reflex® control.

Figure 4.1 shows that the EVM power supplies are a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching supplies are implemented for larger loads. The switching supplies are listed below followed

by explanations of critical component selection:

- CVDD (AVS core power for TMS320C6670)
- VCC1V0 (1.0V fixed core power for TMS320C6670)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC1V5 (1.5V DDR3 power for TMS320C6670 and DDR3 memories)
- VCC5 (5.0V power for the XDS520V2 mezzanine card)

The **CVDD** and **VCC1V0** power rails are regulated by TI Smart-Reflex controller UCD9222 and the synchronous-buck power driver UCD74110 and UCD74106 to supply DSP AVS core and CVDD1 core power.

The **VCC3V3_AUX** and **VCC1V5** power rails are regulated by two TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources and the DSP DDR3 EMIF and DDR3 memory chips respectively.

The **VCC5** power rail is regulated by TI 2A Step Down SWIFT™ DC/DC Converter, TPS54231, to supply the power of the XDS560V2 mezzanine card on TMDXEVM6670L.

The high level diagrams and output components are shown in figure 4.2, figure 4.3, figure 4.4 and figure 4.5 as well as choosing the proper inductors and buck capacitors.

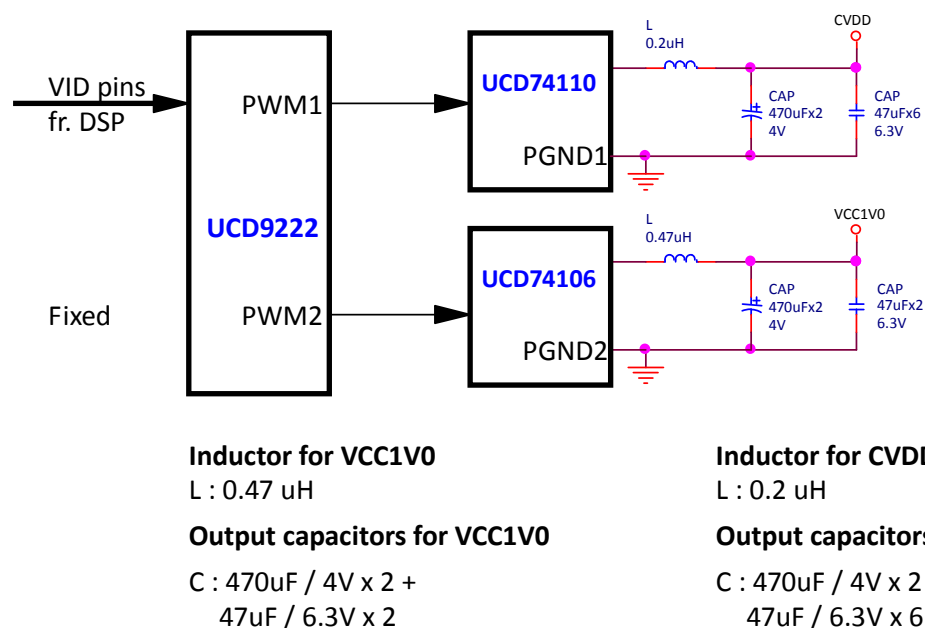
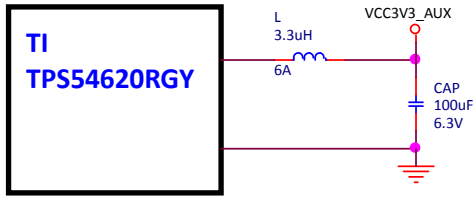


Figure 4.2: The CVDD and VCC1V0 (CVDD1) power design on TMDXEVM6670L EVM



(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

Output capacitor Calculation

$$C_{out} > (2 \times \Delta I_{out}) / (F_{sw} \times \Delta V_{out})$$

$$C_{out} > (2 \times 3) / (840\text{KHz} \times 0.0825)$$

$$C_{out} > (6) / (69300)$$

$$C_{out} > 87\mu\text{F}$$

Reference Capacitor : 100uF

Inductor Calculation

$$L = ((V_{in(max)} - V_{out}) / I_{out} \times Kind) \times (V_{out} / (V_{in(max)} \times F_{sw}))$$

$$L = ((12.6 - 3.3) / 3 \times Kind) \times (3.3 / (12 \times 840\text{KHz}))$$

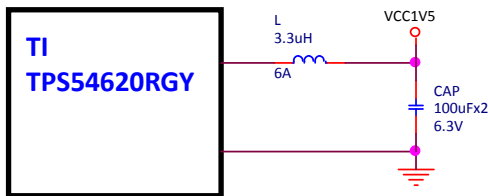
$$L = ((8.7/3 \times 0.3) \times (3.3 / (10.08\text{M})))$$

$$L = (9.67) \times (0.33\mu)$$

$$L \sim 3.2\mu\text{H}$$

Reference Inductor 3.3uH

Figure 4.3: The VCC3_AUX power esign on TMDXEVM6670L EVM



(Over all tolerance is 5% ,DC tolerance is 2.5%)

Output capacitor Calculation

$$C_{out} > (2 \times \Delta I_{out}) / (F_{sw} \times \Delta V_{out})$$

$$C_{out} > (2 \times 2.5) / (840\text{KHz} \times 0.0375)$$

$$C_{out} > (5) / (31500)$$

$$C_{out} > 159\mu\text{F}$$

Reference Capacitor : 100uF x 2=200uF

Inductor Calculation (KIND=0.3)

$$L = ((V_{in(max)} - V_{out}) / I_{out} \times Kind) \times (V_{out} / (V_{in(max)} \times F_{sw}))$$

$$L = ((12 - 1.5) / 2.5 \times Kind) \times (1.5 / (12 \times 840\text{KHz}))$$

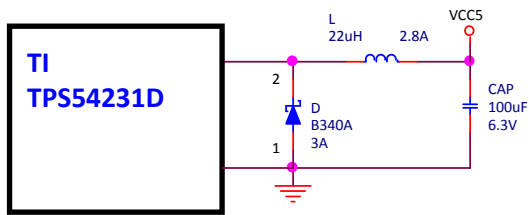
$$L = ((10.5/2.5 \times 0.3) \times (1.5 / (10.08\text{M})))$$

$$L = (10.51/0.75) \times (0.1488\text{M})$$

$$L = 2.09\mu\text{H}$$

Reference Inductor 3.3uH

Figure 4.4: The VCC1V5 power design on TMDXEVM6670L EVM



Output capacitor Calculation

$$C_{O_min} = 1 / (2 \times \pi \times R_O \times F_{CO_max})$$

Cout : $1 / (2 \times 3.14 \times 5 \times 25K)$

Cout : 1.3 uf

Reference Capacitor : 100uF

Inductor Calculation (KIND=0.3)

$$L : ((V_{in(max)} - V_{out}) / I_{out} \times Kind) \times (V_{out} / (V_{in(max)} \times F_{sw}))$$

$$L : ((12.6 - 5) / 1 \times Kind) \times (5 / (12.7 \times 570K))$$

$$L : ((7.6 / 0.3) \times (5 / (7239K)))$$

$$L : (25.3) \times (0.69M)$$

$$L : 17.5uH$$

Reference Inductor 22uH

Figure 4.5: The VCC5 power design on TMDXEVM6670L EVM

4.3 The Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The TMS320C6670 DSP requires specific power up and power down sequencing. Figure 4.6 and Figure 4.7 illustrate the correct boot up and down sequence. Table 4.3 provides the timing details for Figure 4.6 and Figure 4.7.

Refer to the TMS320C6670 DSP Data Manual for confirmation of specific sequencing and timing requirements.

| Step | Power rails | Timing | Descriptions |
|-----------------|--|--------|---|
| Power-Up | | | |
| 1 | VCC12 (AMC Payload power), VCC3V3_AUX, VCC1V8_AUX VCC1V2 VCC5 | Auto | When the 12V power supplied to the TMDXEVM6670L, the 3.3V, 1.8V and 1.2V supplies to the FPGA power will turn on. The 1.8V outputs on the FPGA to the DSP will be locked (held at ground). |
| 2 | VCC2V5 | 10mS | Turn on VCC2V5 after VCC3V3 stable for 10mS. |
| 3 | CVDD (DSP AVS core power) | 5mS | Enable the CVDD and VCC1V0, the UCD9222 power rail#1 is for CVDD and go first after both of VCC5 and VCC2V5 are stable for 5mS. |
| 4 | VCC1V0 (DSP CVDD1 fixed core power) | 5mS | Turn on VCC1V0, the UCD222 power rail#2. The VCC1V0 will start the regulating power rail after enable it after 5mS, the start-delay time is set by the UCD9222 configuration file. |
| 5 | VCC1V8 (DSP IO power) | 5mS | Turn on VCC1V8 after VCC1V0 stable for 5mS. |
| 6 | CDCE62005#2/#3 initiations CDCE62002#1 initiations FPGA 1.8V outputs | 5mS | Unlock the 1.8V outputs and initiate the CDCE62005s and CDCE62002 after VCC1V8 stable for 5mS. De-asserted CDCE62005s and CDCE62002 power down pins (PD#), initial the clock generators. |
| 7 | VCC1V5 (DSP DDR3 power) | 5mS | Turn on VCC1V5 after initiation of the clock generators for 5mS. |
| 8 | VCC0V75 | 5mS | Turn on VCC0V75 after VCC1V5 stable for 5mS. When VCC1V5 is valid, FPGA will de-assert the power down pin on |

| | | | |
|-------------------|--|-----|--|
| | | | the ICS557-08, the PCIE clock multiplexer. When the VCC0V75 is valid, FPGA will enable the ICS557-08 clock outputs by the OE# pin on it. |
| 9 | RESETz Other reset and NMI pins | 5mS | De-asserted RESETz and unlock other reset and NMI pins for the DSP after VCC0V75 stable and 3 clock generators' PLLs locked for 5mS. In the meanwhile, the FPGA will driving the boot configurations to the DSP GPIO pins. |
| 10 | PORz | 5mS | De-asserted PORz after RESETz de-asserted for 5mS. |
| 11 | RESETFULLz | 5mS | De-asserted RESETFULLz after PORz de-asserted for 5mS. |
| 12 | DSP GPIO pins for boot configurations | 1mS | Release the DSP GPIO pins after RESETFULLz de-asserted for 1mS |
| Power-Down | | | |
| 13 | RESETFULLz PORz | 0mS | If there is any power failure events or the AMC payload power off, the FPGA will assert the RESETFULLz and PORz signals to the DSP. |
| 14 | FPGA 1.8V outputs to DSP CDCE62005 and CDCE62002 PDz pins | 5mS | Locked 1.8V output pins on the FPGA and pull the CDCE62005 and CDCE62002 PDz pins to low to disable the DSP clocks. |
| 15 | CVDD VCC1V0 VCC1V8 VCC1V5 VCC0V75 VCC2V5 ICS557-08 PD# and OE# | 0mS | Turn off all main power rails. |

Table 4.3: The power-up and down timing on the TMDXEVM6670L

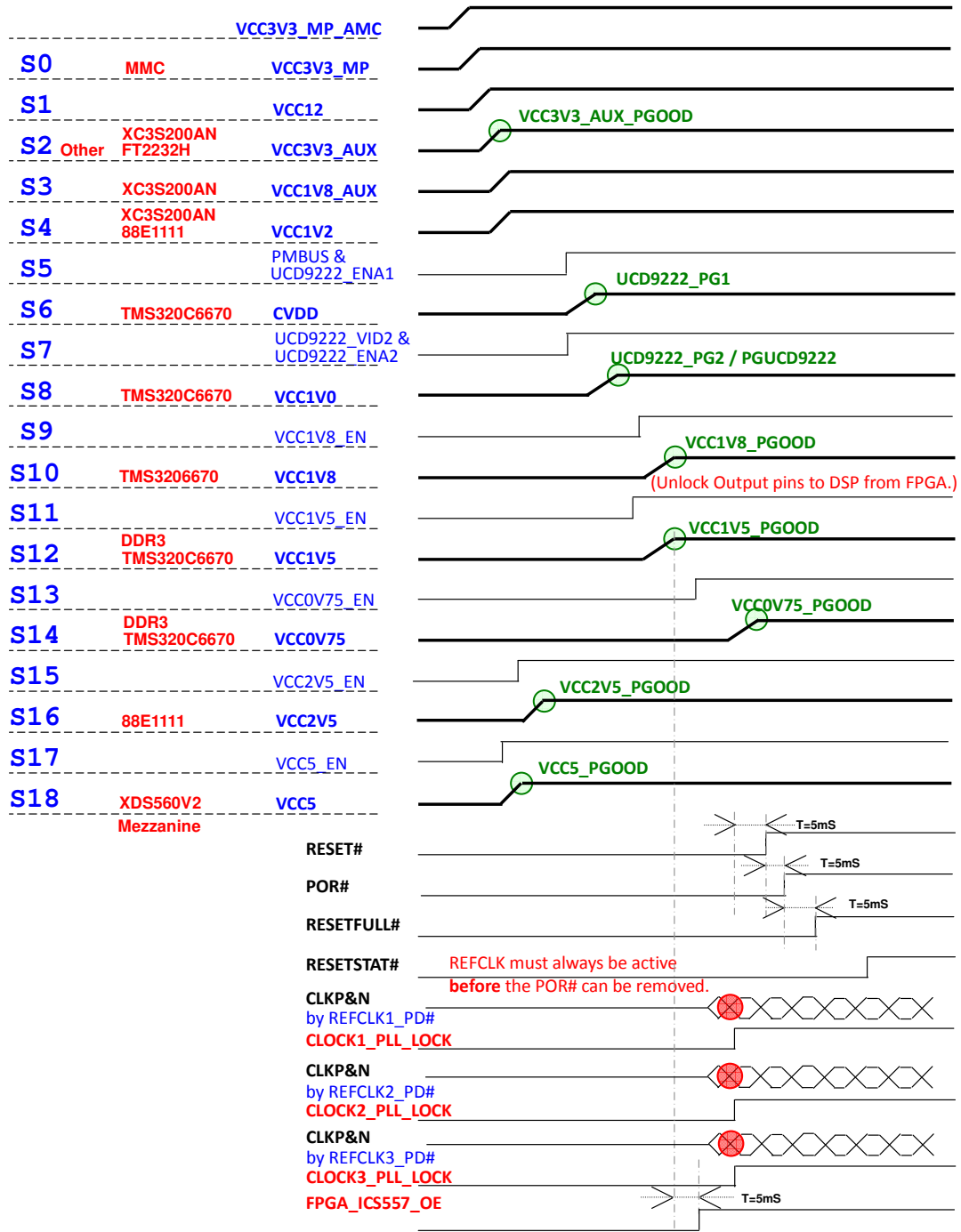


Figure 4.6: Initial Power-on Sequence Timing Diagram

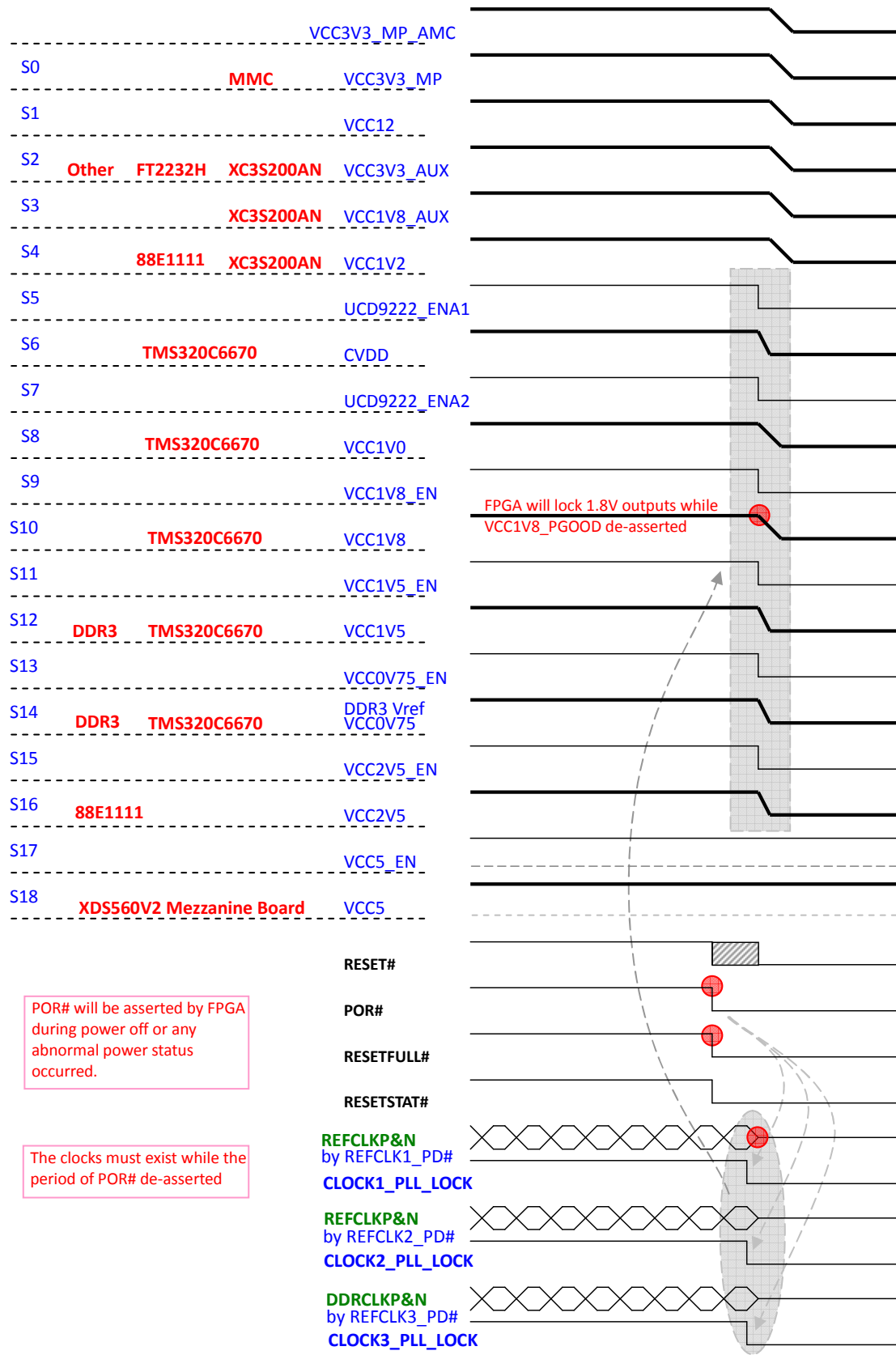


Figure 4.7: Power Down Sequence Timing Diagram

5. TMDXEVM6670L FPGA FUNCTIONAL DESCRIPTION

This chapter contains,

- 5.1 FPGA overview
- 5.2 FPGA signals description
- 5.3 Sequence of operation
- 5.4 Reset definition
- 5.5 SPI protocol
- 5.6 CDCE62005 & CDCE62002 Programming Descriptions
- 5.7 FPGA Configuration Registers

5.1 FPGA overview

The FPGA (Xilinx XC3S200AN) controls the EVM power sequencing, reset mechanism, DSP boot mode configuration and clock initialization. The FPGA also provides the transformation of TDM Frame Synchronization signal and Reference Clock between the AMC connector and the DSP.

The FPGA also supports 4 user LEDs and 1 user switch through control registers. All the FPGA registers are accessible by the TMS320C6670 DSP.

The key features of the TMDXEVM6670L EVM FPGA are:

- TMDXEVM6670L EVM Power Sequence Control
- TMDXEVM6670L EVM Reset Mechanism Control
- TMDXEVM6670L EVM Clock Generator Initialization and Control
- TMS320C6670 DSP SPI Interface for accessing the FPGA Configurable Registers
- Provides Shadow Registers for TMS320C6670 DSP to Access the Clock Generator Configurations Registers
- Provides Shadow Registers for TMS320C6670 DSP to Access the UCD9222 Devices via the PM Bus (TBD)
- Provides TMS320C6670 DSP Boot Mode Configuration switch settings to DSP
- MMC Reset Events Initiation Interface
- Provides the TCLK transformation from the LVDS format to single ended 1.8V level signal between AMC edge connector and the DSP
- Provide Ethernet PHY Interrupt and Reset Control Interface

- Provides Reset Buttons, User Switches, and Debug LEDs
- FPGA Device and Packaging
XILINX XC3S200AN FPGA
256 Ball ftBGA (17x17 mm), 1.0mm pitch

5.2 FPGA signals description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. Throughout this manual, a '#' or 'Z' will be used at the end of a signal name to indicate that the active or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type.

| | |
|--------------|------------------------|
| I | Input pin |
| O | Output pin |
| I/O | Bi-directional pin |
| Differential | Differential Pair pins |
| PU | Internal Pull-Up |

Table 5.1: TMDXEVM6670L EVM FPGA Pin Description

| Pin Name | IO Type | Description |
|----------------------|---------|---|
| MMC Control : | | |
| MMC_DETECT# | I PU | MMC Detection on the insertion to an AMC Chassis: This signal is an insertion indication from the MMC. The MMC will drive logic low state when the EVM module is inserted into an AMC chassis. |
| MMC_RESETSTAT# | O | RESETSTAT# state to MMC: The FPGA will drive the same status of the DSP RESETSTAT# to the MMC via this signal. |
| MMC_POR_IN_AMC# | I PU | MMC POR Request: This signal is used by the MMC to request a Power-on reset sequence to DSP. A logic Low to High transition on this signal will complete the FPGA Full Reset sequence with a specified delay time. |
| MMC_WR_AMC# | I PU | MMC WARM Request: This signal is used by the MMC to initiate a warm reset request. A logic Low to High transition on this signal will complete the FPGA warm reset sequence with a specified delay time. |
| MMC_BOOTCOMPLETE | O | BOOTCOMPLETE state to MMC: The FPGA will drive the same status of the DSP BOOTCOMPLETE to the MMC via this signal. |

| Pin Name | IO Type | Description |
|----------------------------------|---------|---|
| Power Sequences Control : | | |
| VCC5_PGOOD | I | 5V Voltage Power Good Indication: This signal indicates the 5V power is valid. |
| VCC2P5_PGOOD | I | 2.5V Voltage Power Good Indication: This signal indicates the 2.5V power is valid. |
| VCC3_AUX_PGOOD | I | 3.3V Auxiliary Voltage Power Good Indication: This signal indicates the 3.3V auxiliary power is valid. |
| VCC0P75_PGOOD | I | 0.75V Voltage Power Good Indication: This signal indicates the 0.75V power is valid. |
| VCC1P5_PGOOD | I | 1.5V Voltage Power Good Indication: This signal indicates the 1.5V power is valid. |
| VCC1P8_PGOOD | I | 1.8V Voltage Power Good Indication: This signal indicates the 1.8V power is valid. |
| SYS_PGOOD | O | System Power Good Indication: This signal is indicated by the FPGA to the system when all the power supplies are valid. |
| VCC1P8_EN1 | O | 1.8V Voltage Power Supply Enable: VCC1P8_EN1 is for 1.8V power plane control. |
| VCC0P75_EN | O | 0.75V Voltage Power Supply Enable: VCC0P75_EN is for 0.75V power plane control. |
| VCC2P5_EN | O | 2.5V Voltage Power Supply Enable: VCC2P5_EN is for 2.5V power plane control. |
| VCC_5V_EN | O | 5V Voltage Power Supply Enable: VCC_5V_EN is for 5V power plane control. |
| VCC1P5_EN | O | 1.5V Voltage Power Supply Enable : VCC1P5_EN is for 1.5V power plane control. |
| CLOCK Configurations: | | |
| CLOCK[1:3]_SSPCS1 | O | SPI Chip Select Enable: This signal is connected to the TI CDCE62002 & CDCE62005 CLOCK Generators SPI_LE pin. The falling edge of the SSPCS1 initiates a transfer. If SSPCS1 is high, no data transfer can take place. |
| CLOCK[1:3]_SSPCK | O | SPI Serial Clock: This signal is connected to the TI CDCE62002 & CDCE62005 CLOCK Generators SPI_CLK pin. The FPGA SPI bus clocks data in and out on the rising edge of SSPCK. Data transitions therefore occur on the falling edge of the clock. |
| CLOCK[1:3]_SSPSI | O | SPI Serial Data MOSI: This signal is connected to the TI CDCE62002 & CDCE62005 CLOCK Generators MOSI pin. This signal is used for serial data transfers from the master (FPGA) output to the slave (62002)(62005) input. |

| Pin Name | IO Type | Description |
|----------------------------|---------|---|
| CLOCK[1:3]_SSPSO | I | SPI Serial Data MISO: This signal is connected to the TI CDCE62002 & CDCE62005 CLOCK Generators MISO pin. This signal is used for the serial data transfers from the slave (62002)(62005) output to the master (FPGA) input. |
| REFCLK[1:3]_PD# | O | TI CDCE62002 / 62005 CLOCK Generator Power Down: The power down pins each place the respective CDCE62002/62005 into the power down state forcing the differential clock output into the high-impedance state. |
| UCD9222 Interface : | | |
| UCD9222_PG1 | I | UCD9222 Power Good Indication for CVDD DSP Core Power: This signal indicates the CVDD DSP core power is valid. |
| UCD9222_ENA1 | O | UCD9222 Enable for CVDD DSP Core Power: UCD9222_ENA1 is for CVDD DSP core power plane control. |
| UCD9222_PG2 | I | UCD9222 Power Good Indication for VCC1V0 DSP Core Power: This signal indicates the VCC1V0 DSP core power is valid. |
| UCD9222_ENA2 | O | UCD9222 Enable for VCC1V0 DSP Core Power: UCD9222_ENA2 is for VCC1V0 DSP core power plane control. |
| PGUCD9222 | I | UCD9222 Power Good Indication: This signal indicates both the CVDD DSP and VCC1V0 DSP core power supplies are valid. |
| UCD9222_RST# | O | UCD9222 Reset: An active low signal will reset the UCD9222 device. |
| PM BUS: (RFU) | | |
| PMBUS_CLK | O | PM Bus Clock: The FPGA provides the clock source on the PM bus. |
| PMBUS_DAT | I/O | PM Bus Data: A PM Bus slave device can receive data provided by the master (FPGA), or it can also provide data to the master (FPGA) via this signal line. |
| PMBUS_ALT | I | PM Bus Alert: The PM Bus device may notify the host (FPGA) via this signal if a fault or warning is detected. |
| PMBUS_CTL | O PU | PM Bus Control: This signal is used to turn the device on and off in conjunction with UCD9222_ENA1 / UCD9222_ENA2 pins. |
| PHY Interface : | | |
| PHY_INT# | I | Interrupt Request from 88E1111 PHY(RFU) |

| Pin Name | IO Type | Description |
|---|---------|--|
| PHY_RST# | O | Reset to 88E1111 PHY: This signal is used to reset the 88E1111 PHY device. The PHY_RST# will be asserted during the active DSP_PORZ or DSP_RESETFULLz period. The PHY_RST# logic also can be configured by the DSP accessed register. |
| DSP SPI : | | |
| DSP_SSPCS1 | I | DSP SPI Chip Select 1: This signal is connected to the TMS320C6670 DSP SPISCS1 pin. The falling edge of the SSPCS1 from the DSP will initiate a transfer. If SSPCS1 is high, no data transfer can take place. |
| DSP_SSCLK | I | DSP SPI Serial Clock: This signal is connected to the TMS320C6670 DSP SPICLK pin. The FPGA SPI bus clocks data in on the falling edge of SSCLK. Data transitions therefore occur on the rising edge of the clock. |
| DSP_SSPMISO | O | DSP SPI Serial Data MISO: This signal is connected to the TMS320C6670 DSP SPIDIN pin. This signal is used for serial data transfers from the slave (FPGA) output to the master (DSP) input in the DSP_SSPCS1 asserted period. |
| DSP_SSPMOSI | I | DSP SPI Serial Data MOSI: This signal is connected to the DSP SPIDOUT pin. This signal is used for serial data transfers from the master (DSP) output to the slave (FPGA) input. |
| RESET Buttons and Requests : | | |
| FULL_RESET | I | Full Reset Button Input: This button input is used to initiate a Full Reset event. |
| WARM_RESET | I | Warm Reset Button Input: This button input is used to initiate a Warm Reset event. |
| COLD_RESET (RFU) | I | Cold Reset Button Input : Reserved for Future Use (RFU). |
| FPGA_JTAG_RST# (RFU) | I | FPGA JTAG Reset Input : Reserved for Future Use (RFU). |
| TRGRSTZ | I | Reset Request from the DSP Emulator Header: A warm Reset sequence will be initiated if an active TRGRSTZ event is recognized by the FPGA. |
| DSP Boot & Device configurations : | | |
| BM_GPIO[0: 15] | I | DSP Boot Mode Strap Configuration: These switch inputs are used to drive the DSP boot mode configuration during the EVM power up period. |

| Pin Name | IO Type | Description |
|---|---------|--|
| DSP_GPIO[0: 15] | I/O | DSP GPIO: In normal operation mode, these signals are not driven by the FPGA so that the DSP can use them as GPIO pins. During the EVM Power-on or during the RESETFULLz asserted period, the FPGA will output the BM_GPIO switch values to the DSP on these pins so the DSP can latch the boot mode configuration. |
| DSP RESET & Interrupts Control : | | |
| DSP_CORESEL[0:2] | O | DSP Core Selection Bit: The default value is 0000b and Register bits define the state of these pins.. |
| DSP_PACLKSEL | O | DSP PACLKSEL: This pin is used for the DSP PASS clock selection setting. The logic of this signal is derived from the BM_GPIO[13:11] state or configured by the FPGA registers. |
| FPGA_DSPCLKSEL | O | CORECLKSEL : RFU, Reserved for Future Use |
| FPGA_EXTFRAMEEVENT | I | EXTFRAMEEVENT : RFU, Reserved for Future Use |
| DSP_LRESETNMIENZ | O | Latch Enable for DSP Local Reset and NMI Inputs: The default value is 1b and a register bit defines the state of this pin. |
| DSP_NMIZ | O | DSP NMI. The default value is 1b and unlocked a register bit defines the state of this pin. |
| DSP_LRESETZ | O | DSP Local Reset. The default value is 1b and a register bit defines the state of this pin. |
| DSP_HOUT | I | DSP HOUT |
| DSP_BOOTCOMPLETE | I | DSP Boot Complete Indication |
| DSP_SYCLKOUT | I | DSP System Clock Output |
| DSP_PORZ | O | DSP Power-on Reset |
| DSP_RESETFULLz | O | DSP Full Reset. |
| DSP_RESETZ | O | DSP Reset |
| FPGA Storage (RFU): | | |
| FPGA_SPI_CS# | O | FPGA SPI Chip Select: (RFU) |
| FPGA_SPI_SI | O | FPGA SPI Serial Data MOSI: (RFU) |
| FPGA_SPI_SCK | O | FPGA SPI Clock Output: (RFU) |
| FPGA_SPI_SO | I | FPGA SPI Serial Data MISO: (RFU) |
| Telecom CLK : | | |
| TCLKA[p/n] | I, Diff | TCLKA Different Clock Input Pairs It's the Telecom reference clock from the AMC backplane. |

| Pin Name | IO Type | Description |
|------------------------|---------|---|
| TCLKB[p/n] | I, Diff | TCLKB Different Clock Input Pairs It's the Telecom reference clock from the AMC backplane. |
| TCLKC[p/n] | I, Diff | TCLKC Different Clock Input Pairs It's the Telecom reference clock from the AMC backplane. |
| TCLKD[p/n] | I, Diff | TCLKD Different Clock Input Pairs It's the Telecom reference clock from the AMC backplane. |
| DEBUG LED: | | |
| DEBUG_LED[1:4] | O | Debug LED: The LEDs are used for debugging purposes only. It can be configured by the registers in the FPGA. |
| Miscellaneous : | | |
| MAIN_48MHZ_CLK_R | I | FPGA Main Clock Source: A 48 MHz clock is used as the FPGA main clock source. |
| DSP_TIMI0 | O | DSP Time 0 Clock : The FPGA provides the clock to DSP time 0. During the EVM power on or PORZ/RESETFULLZ asserted period, the FPGA will drive the PCIESSEN switch state to DSP for the boot configuration strapping. The FPGA drives 24MHz to DSP_TIMI0 after the DSP Boot Configuration Strapping completed |
| DSP_TIMI1 | O | DSP Timer 1 Clock: The FPGA provides the clock to DSP time 1. The FPGA drives 24MHz to DSP_TIMI1 after the DSP Boot Configuration Strapping completed. |
| DSP_VCL_1 (RFU) | I | DSP Smart Reflex I2C Clock |
| DSP_VD_1 (RFU) | I/O | DSP Smart Reflex I2C Clock |
| PCA9306_EN (RFU) | O | PCA9306 Enable: This signal is used to enable the DSP Smart Reflex I2C buffer function. |
| NAND_WP# | O | NAND Flash Write Protect: This signal is used to control the NAND flash write-protect function. |
| NOR_WP# | O | NOR Flash Write Protect: This signal is used to control the NOR flash write-protect function. |
| EEPROM_WP | O | EEPROM Write Protect: This signal is used to control the EEPROM write-protect function. |
| PCIESSEN | I | PCI Subsystem Enable: This is used for the PCIESSEN switch input. |
| USER_DEFINE | I | User Defined Switch: This is reserved for the user defined switch input. |

| Pin Name | IO Type | Description |
|------------------------------------|---------|--|
| ICS557_SEL | O | PCIe clock multiplexor inputs selection: This pin is controlled by the register to select PCIe reference clock from the CDCE62005 or the AMC edge connector. The default is from the CDCE62005. |
| ICS557_PD# | O | PCIe clock multiplexor Power Down: This pin is used to control the ICS557-08 PD# pin, it's de-asserted after VCC1V5 valid. |
| ICS557_OE | O | PCIe clock multiplexor output enable: This pin enables the output of the ICS557-08. |
| VID_OE# | O | Smart-Reflex VID Enable: This pin enables the output of the Smart-Reflex VID from the DSP to the UCD9222. |
| FPGA JTAG TAP Control Port: | | |
| JTAG_FPGA_TCK | I | FPGA JTAG Clock Input |
| JTAG_FPGA_TDI | I | FPGA JTAG Data Input |
| JTAG_FPGA_TDO | O | FPGA JTAG Data Output |
| JTAG_FPGA_TMS | I | FPGA JTAG Mode Select Input |
| JTAG_FPGA_RST# | I | FPGA JTAG Reset (RFU) |

5.3 Sequence of operation

This section describes the FPGA sequence of operation on the EVM. It contains:

- 5.3.1 Power-on Sequence
- 5.3.2 Power down Sequence
- 5.3.3 Boot Configuration Timing
- 5.3.4 Boot Configuration Forced in I2C Boot

5.3.1 Power-on Sequence

The following section provides details of the FPGA Power-on sequence of operation.

1. After the EVM 3.3V and 1.2V auxiliary power rails (VCC3V3_AUX_PGOOD) are valid, the FPGA design code is loaded, the FPGA is ready for the Power-on sequence of operation. The 5V power is enabled when the POL of EVM supplied as well.
2. The FPGA starts to execute the Power-on sequence. Wait for 10 ms, the FPGA enable the 2.5V power.
3. Once the 5V and 2.5V voltages (VCC5_PGOOD and VCC2P5_PGOOD) are valid, wait for 5 ms (TBD), the FPGA asserts the UCD9222_ENA1 and UCD9222_ENA2 to enable the CVDD and VCC1V0 DSP core power.

4. After both the UCD9222_PG1 and UCD9222_PG2 are valid, wait for 5 ms, the FPGA enables the 1.8V power.
5. After the 1.8V voltage (VCC1P8_PGOOD) is valid, wait for 5 ms, the FPGA initialize the CDCE62005 clock generator – 2 and CDCE62005 clock generator – 3. Wait for 1 ms and the CDCE62005 clock generator – 2 and CDCE62005 clock generator – 3 PLL is locked, the FPGA initialize CDCE62002 clock generator – 1. Wait for 1 ms and the FPGA enables the 1.5V power.
6. After the 1.5V voltage (VCC1V5_PGOOD) is valid, wait for 5 ms, the FPGA enables the 0.75V power and Level shift component output and initialize the ICS557.
7. After the 0.75V voltage (VCC0V75_PGOOD) is valid, wait for 5 ms, the FPGA de-assert the DSP_RESETz and DSP_LRESETz. Keep DSP_PORz and DSP_RESETFULLz asserted.
8. After the DSP_RESETz and DSP_LRESETz have de-asserted, wait for 5 ms and check the PLL locked bits in two CDCE62005s to make sure all clocks are stable, the FPGA de-asserts the DSP_PORz and keeps the DSP_RESETFULLz still being asserted. Wait for another 5 ms, the FPGA de-asserts the DSP_RESETFULLz. The FPGA will drive the BM_GPIO switches value to the DSP for the DSP boot mode configuration strapping during the period from the VCC0P75_PGOOD is valid to the RESETSTAT# being de-asserted. The FPGA will also drive the PCIESSEN switch value to DSP_TIMIO for the DSP boot configuration strapping.
9. Wait for RESETSTAT# signal from DSP to go from low to high. The EVM Power-on sequence is completed.

5.3.2 Power Off Sequence

Following section provides details of FPGA power off sequence of operation.

1. Once the system powers on, any power failure events (any one of power good signals de-asserted) will trigger the FPGA to proceed to the power off sequence.
2. Once any de-asserted Power Good signals have been detected by the FPGA, the FPGA will assert the DSP_PORz to DSP immediately.
3. Wait for 5 ms, the FPGA will disable all the system power rails, assert all the other DSP resets to DSP, lock the +1.8V output pins from the FPGA to the DSP and also assert power down signals to the CDCE62005 and the CDCE62002 clock generators.
4. FPGA remains in the power failure state until main 12V power is removed and restored.

5.3.3 Boot Configuration Timing

The boot configuration timing of the power-up and the RESETFULLz event are shown below.

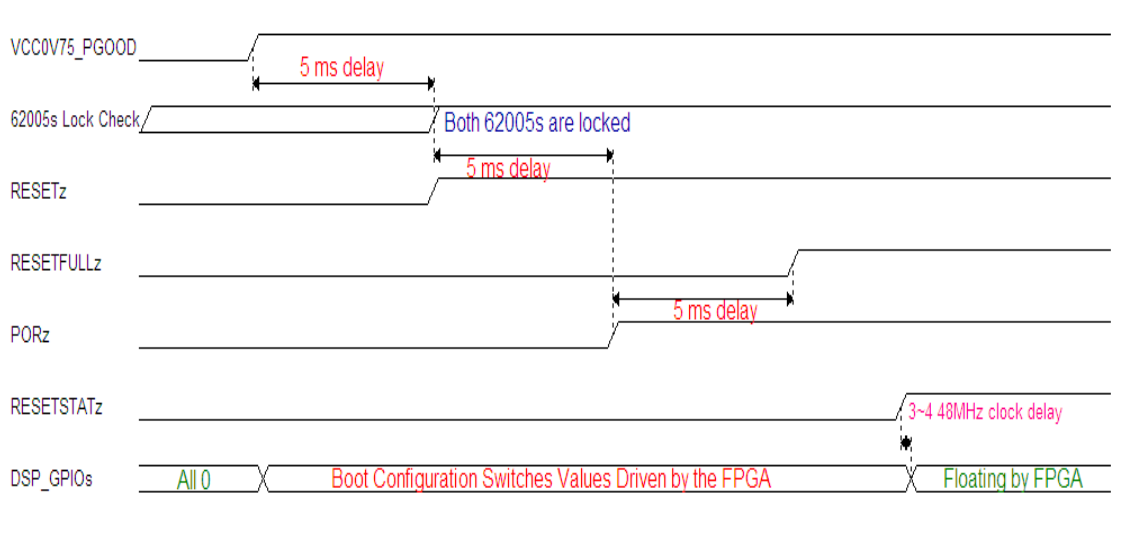


Figure: 5-1 Power-on Reset Boot Configuration Timing

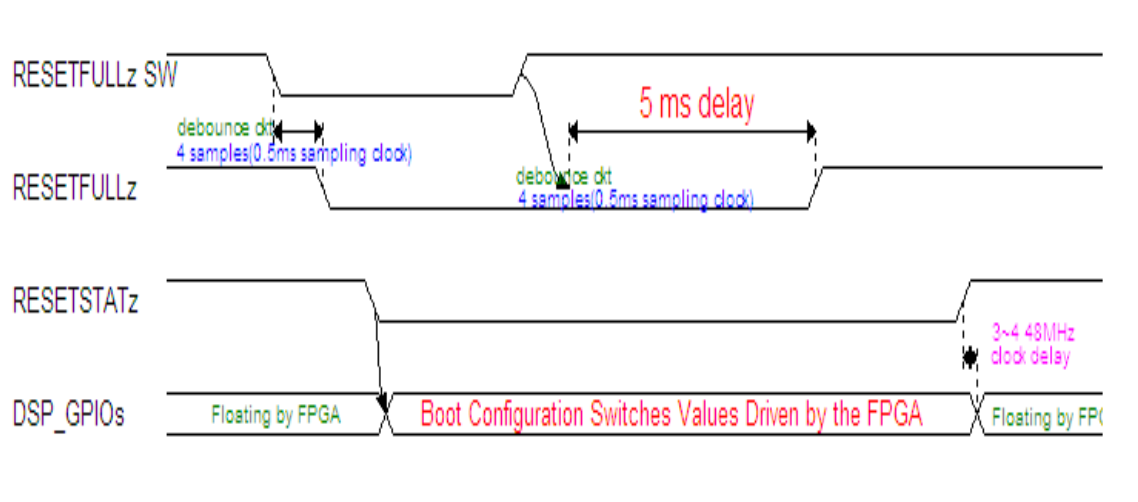


Figure: 5-2 Reset-Full Switch/Trigger Boot Configuration Timing

5.3.4 Boot Configuration Forced in I2C Boot

Note: This workaround is only needed with PG1.0 samples of the TMS320C6670 DSP.

For reliable PLL operation at boot-up, the FPGA will force the DSP to boot from the I2C by providing the boot configuration value as 0x0405 on the boot mode pins [12:0]. After the code in the I2C SEEPROM executes to initialize the PLLs, it will read the true values on the DIP switches from the registers in the FPGA and then boot as if the normal boot sequence had occurred.

The exception for the forced I2C boot is the emulation boot. The FPGA will not perform the I2C boot configuration override when the DIP switches have the following configuration: BOOTMODE[2:0] (GPIO[3:1]) = [000] and BOOTMODE[5:4] (GPIO[6:5]) = [00]. Therefore, the additional logic of the FPGA will allow the emulation boot to latch directly from the DIP switches.

5.4 Reset definition

5.4.1 Reset Behavior

- **Power-on:** The Power-on behavior includes initiating and sequencing the power sources, clock sources and then DSP startup. Please refer to the section 5.5.1 for detailed sequence and operations.
- **Full Reset:** The RESETFULLz is asserted low to the DSP. This causes RESETSTAT# to go low which triggers the boot configuration to be driven from the FPGA. Reset to the Marvell PHY is also asserted. POR# and RESET# to the DSP remain high. The power supplies and clocks operate without interruption. Please refer to the section 5.5.3 for detailed timing diagrams.
- **Warm Reset:** The RESETz is asserted low to the DSP. The PORz and RESETFULLz to the DSP remain high. The power supplies and clocks operate without interruption.

5.4.2 Reset Switches and Triggers

- **FULL_RESET** (RST_FULL1) – a logic low state with a low to high transition will trigger a Full Reset behavior event.

When the push button switch RST_FULL1 is pressed, FPGA on EVM will assert DSP's RESETFULL# input to issue a total reset of the DSP, everything on the DSP will be reset to its default state in response to this event, boot configurations will be latched and the ROM boot process will be initiated.

This is equivalent to a power cycle of the board but POR and will have following effects:

- * Reset DSP
 - * Reset Gigabit Ethernet PHY
 - * Reload boot parameters.
 - * Protect the contents in the I2C EEPROM, NAND flash and SPI NOR flash.
- **WARM_RESET** (RST_WARM1) – a logic low state with a low to high transition will trigger a warm reset behavior event.

When the push button Switch RST_WARM1 is pressed, FPGA will assert a DSP RESET#

input, which will reset the DSP. Software can program this to be either hard or soft. Hard reset is the default which resets almost everything. Soft Reset will behave like Hard Reset except that PCIe MMRs, EMIF16 MMRs, DDR3 EMIF MMRs, and External Memory contents are retained.

Boot configurations are not latched by Warm Reset. Also, Warm Reset will not reset blocks supporting Reset Isolation when they are appropriately configured previously by application software. Warm Reset must be used to wake from low-power sleep and hibernation modes.

In the case of a Soft Reset, the clock logic or the power control logic of the peripherals are not affected, and, therefore, the enabled/disabled state of the peripherals is not affected. The following external memory contents are maintained

During a Soft Reset:

- **DDR3 MMRs:** The DDR3 Memory Controller registers are *not* reset. In addition, the DDR3 SDRAM memory content is retained if the user places the DDR3 SDRAM in self-refresh mode before invoking the soft reset.
- **PCIe MMRs:** The contents of the memory connected to the EMIFA are retained. The EMIFA registers are *not* reset.
- **COLD_RESET (RST_COLD1)** – not used in current implementation.
- **MMC_POR_IN_AMC#** - a logic low state with a low to high transition will trigger a Full Reset behavior event.
- **MMC_WR_AMC#** - a logic low state with a low to high transition will trigger a warm reset behavior event.
- **TRGRSTz** - a logic low state with a low to high transition on the Target Reset signal from emulation header that will trigger a warm reset behavior event.
- **FPGA_JTAG_RST#** - not used in current implementation.

5.5 SPI protocol

This section describes the FPGA SPI bus protocol design specification for interfacing with TMS320C6670 DSP and CDCE62005 clock generators. It contains:

5.5.1 FPGA-DSP SPI Protocol

5.5.2 FPGA-CDCE62005(Clock Generator) SPI Protocol

5.5.1 FPGA-DSP SPI Protocol

The FPGA supports the simple write and read commands for the TMS320C6670 DSP to

access the FPGA configuration registers through the SPI interface. The FPGA SPI bus clocks data in on the falling edge of DSP SPI Clock. Data transitions therefore occur on the rising edge of the clock.

The figures below illustrate the DSP to FPGA SPI write operation.

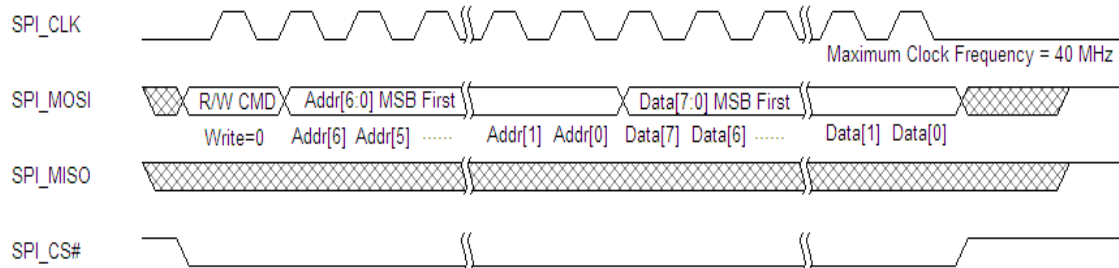


Figure 5-3: The SPI access form the TMS320C6670 to the FPGA (WRITE / high level)

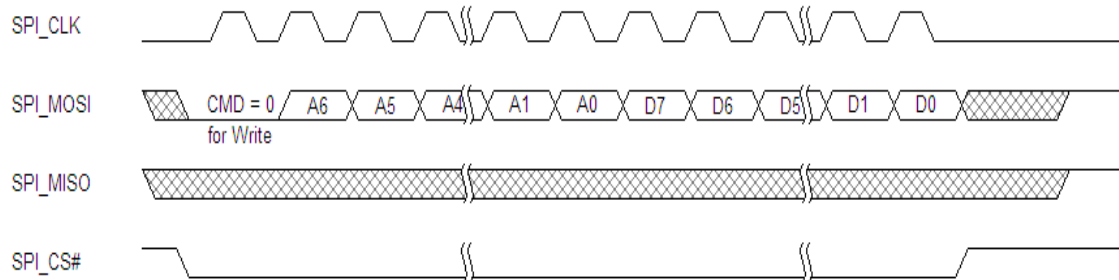


Figure 5-4: The SPI access form the TMS320C6670 to the FPGA (WRITE)

The figures below illustrate the DSP to FPGA SPI read operation.

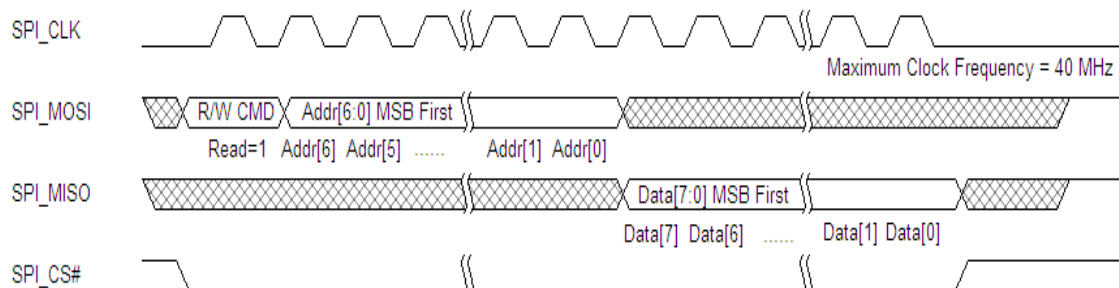


Figure 5-5: The SPI access form the TMS320C6670 to the FPGA (READ / high level)

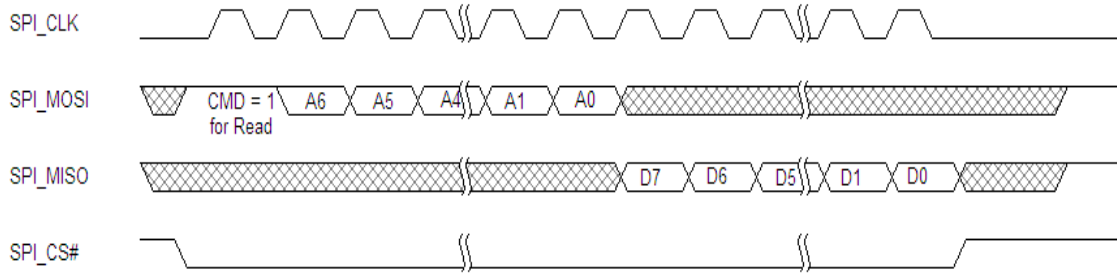


Figure 5-6: The SPI access form the TMS320C6670 to the FPGA (READ)

5.5.2 FPGA- CDCE62005(Clock Generator) SPI Protocol

The FPGA-Clock Generator SPI interface protocol is compatible to CDCE62005 SPI. The FPGA SPI bus clocks data in on the rising edge of DSP SPI Clock. Data transitions therefore occur on the falling edge of the clock.

The figure below illustrates a FPGA to CDCD62005 SPI write operation.

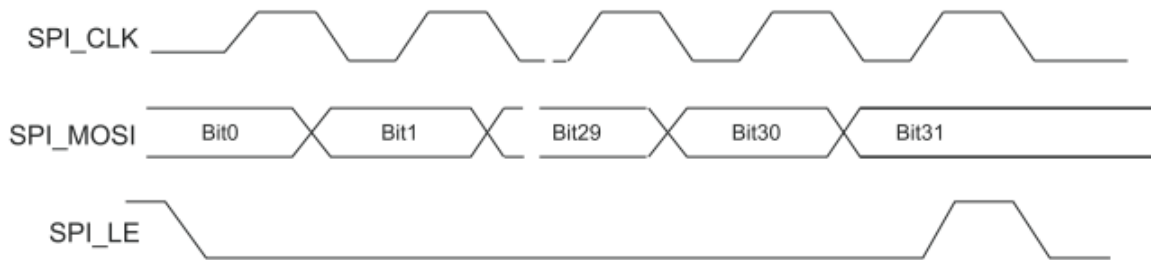


Figure 5-7: The SPI access form the FPGA to the CDCE62005 (WRITE)

The figure below illustrates a FPGA to CDCD62005 SPI read operation.

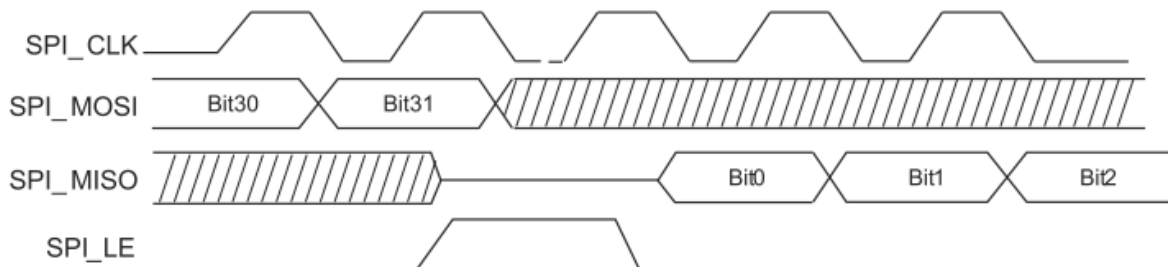


Figure 5-8: The SPI access form the FPGA to the CDCE62005 (READ)

5.6 FPGA Configuration Registers

The TMS320C6670 DSP communicates with the FPGA configuration registers through the SPI

interface. These registers are addressed by the memory mapped location and defined by the DSP SPI chip enable setting. The following tables list the FPGA configuration registers and the respective descriptions.

The TMS320C6670 DSP communicates with the FPGA configuration registers through the SPI interface. These registers are addressed by the memory mapped location and defined by the DSP SPI chip enable setting. The following tables list the FPGA configuration registers and the respective descriptions.

Table 5.2: TMDXEVM6670L EVM FPGA Memory Map

| Memory Map Base Address | Memory Map Offset Address | Memory |
|--|---------------------------|-------------------------|
| DSP SPI Chip Select 1 0x20BF0000-0x20BF03FF (TMS320C6670 DSP SPI Memory Map Address) | 0x00-0x4F | Configuration Registers |

5.6.1 FPGA Configuration Registers Summary

Table 5.3: FPGA Configuration Registers Summary

| Address Offset | Definition | Attribute (R/W) (RO: Read-Only) | Default Value |
|----------------|--|---------------------------------------|---------------|
| 00h | FPGA Device ID (Low Byte) | RO | 05h |
| 01h | FPGA Device ID (High Byte) | RO | 80h |
| 02h | FPGA Revision ID (Low Byte) | RO | ** |
| 03h | FPGA Revision ID (High Byte) | RO | 00h* |
| 04h | BM GPI Status (Low Byte) | RO | ---- |
| 05h | BM GPI Status (High Byte) | RO | ---- |
| 06h | DSP GPI Status (Low Byte) | RO | ---- |
| 07h | DSP GPI status (High Byte) | RO | ---- |
| 08h | Debug LED | R/W | 00h |
| 09h | MMC Control | RO | ---- |
| 0Ah | PHY Control | R/W | 03h |
| 0Bh | Reset Buttons Status | RO | 00h |
| 0Ch | Miscellaneous - 1 | R/W | 1Ch |
| 0Dh | Miscellaneous - 2 | RO | -- |
| 0Eh | FPGA FW Update SPI Interface Control Register | R/W | 00h |
| 0Fh | Scratch Register | R/W | 00h |
| 10h | CLK-GEN 2 Control Register | R/W | 00h |
| 11h | CLK-GEN 2 Interface Clock Setting | R/W | 03h |
| 13h~12h | Reserved | | 0s |
| 14h | CLK-GEN 2 Command Byte 0 | R/W | 00h |
| 15h | CLK-GEN 2 Command Byte 1 | R/W | 00h |

| Address Offset | Definition | Attribute (R/W) (RO: Read-Only) | Default Value |
|--|---------------------------------------|---------------------------------------|---------------|
| 16h | CLK-GEN 2 Command Byte 2 | R/W | 00h |
| 17h | CLK-GEN 2 Command Byte 3 | R/W | 00h |
| 18h | CLK-GEN 2 Read Data Byte 0 | RO | 00h |
| 19h | CLK-GEN 2 Read Data Byte 1 | RO | 00h |
| 1Ah | CLK-GEN 2 Read Data Byte 2 | RO | 00h |
| 1Bh | CLK-GEN 2 Read Data Byte 3 | RO | 00h |
| 1Fh~1Ch | Reserved | | 0s |
| 20h | CLK-GEN 3 Control Register | R/W | 00h |
| 21h | CLK-GEN 3 Interface Clock Setting | R/W | 03h |
| 23h~22h | Reserved | | 0s |
| 24h | CLK-GEN 3 Command Byte 0 | R/W | 00h |
| 25h | CLK-GEN 3 Command Byte 1 | R/W | 00h |
| 26h | CLK-GEN 3 Command Byte 2 | R/W | 00h |
| 27h | CLK-GEN 3 Command Byte 3 | R/W | 00h |
| 28h | CLK-GEN 3 Read Data Byte 0 | RO | 00h |
| 29h | CLK-GEN 3 Read Data Byte 1 | RO | 00h |
| 2Ah | CLK-GEN 3 Read Data Byte 2 | RO | 00h |
| 2Bh | CLK-GEN 3 Read Data Byte 3 | RO | 00h |
| 2Fh~2Ch | Reserved | | 0s |
| 3Fh~30h | PM Bus (RFU) | R/W | 0s |
| 40h | CLK-GEN 1 Control Register | R/W | 00h |
| 41h | CLK-GEN 1 Interface Clock Setting | R/W | 03h |
| 43h~42h | Reserved | | 0s |
| 44h | CLK-GEN 1 Command Byte 0 | R/W | 00h |
| 45h | CLK-GEN 1 Command Byte 1 | R/W | 00h |
| 46h | CLK-GEN 1 Command Byte 2 | R/W | 00h |
| 47h | CLK-GEN 1 Command Byte 3 | R/W | 00h |
| 48h | CLK-GEN 1 Read Data Byte 0 | RO | 00h |
| 49h | CLK-GEN 1 Read Data Byte 1 | RO | 00h |
| 4Ah | CLK-GEN 1 Read Data Byte 2 | RO | 00h |
| 4Bh | CLK-GEN 1 Read Data Byte 3 | RO | 00h |
| 4Fh~4Ch | Reserved | | 0s |
| 50h | ICS 557 Clock Select Control Register | R/W | 00h |
| Note : “*” means the value may be changed in the future FPGA FW update release. | | | |

5.6.2 FPGA Configuration Registers Descriptions

Register Address : **SPI Base + 00h**

Register Name : **FPGA Device ID (Low Byte) Register**

Default Value: 05h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | FPGA Device ID (Low Byte) This offset 01h field combined with this field identifies the particular device. This identifier is allocated by the FPGA design team. | RO |

Register Address : **SPI Base + 01h**

Register Name : **FPGA Device ID (High Byte) Register**

Default Value: 80h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | FPGA Device ID (High Byte) This field combined with the offset 00h field identifies the particular device. This identifier is allocated by the FPGA design team. | RO |

Register Address : **SPI Base + 02h**

Register Name : **FPGA Revision ID (Low Byte) Register**

Default Value: **

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | FPGA Revision ID (Low Byte) This offset 03h register combined with this register specifies the FPGA device specific revision identifier. The value may be changed in the future FPGA FW update release. | RO |

Register Address : **SPI Base + 03h**

Register Name : **FPGA Revision ID (High Byte) Register**

Default Value: 00h*

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | FPGA Revision ID (High Byte) This register combined with the offset 02h register specifies the FPGA device specific revision identifier. The value may be changed in the future FPGA FW update release. | RO |

Register Address : **SPI Base + 04h**

Register Name : **BM GPIO Status (07-00 Low Byte) Register**

Default Value: ----

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | BM GPIO 00: This bit reflects the state of the BM general purpose input signal GPIO 00 and writes will have no effect. 0: BM GPIO 00 state is low 1: BM GPIO 00 state is high | RO |
| 1 | BM GPIO 01: This bit reflects the state of the BM general purpose input signal GPIO 01 and writes will have no effect. | RO |

| | | |
|---|---|----|
| | 0: BM GPIO 01 state is low 1: BM GPIO 01 state is high | |
| 2 | BM GPIO 02: This bit reflects the state of the BM general purpose input signal GPIO 02 and writes will have no effect. 0: BM GPIO 02 state is low 1: BM GPIO 02 state is high | RO |
| 3 | BM GPIO 03: This bit reflects the state of the BM general purpose input signal GPIO 03 and writes will have no effect. 0: BM GPIO 03 state is low 1: BM GPIO 03 state is high | RO |
| 4 | BM GPIO 04: This bit reflects the state of the BM general purpose input signal GPIO 04 and writes will have no effect. 0: BM GPIO 04 state is low 1: BM GPIO 04 state is high | RO |
| 5 | BM GPIO 05: This bit reflects the state of the BM general purpose input signal GPIO 05 and writes will have no effect. 0: BM GPIO 05 state is low 1: BM GPIO 05 state is high | RO |
| 6 | BM GPIO 06: This bit reflects the state of the BM general purpose input signal GPIO 06 and writes will have no effect. 0: BM GPIO 06 state is low 1: BM GPIO 06 state is high | RO |
| 7 | BM GPIO 07: This bit reflects the state of the BM general purpose input signal GPIO 07 and writes will have no effect. 0: BM GPIO 07 state is low 1: BM GPIO 07 state is high | RO |

Register Address : **SPI Base + 05h**

Register Name : **BM GPI (15-08 High Byte) Status Register**

Default Value: ----

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | BM GPIO 08: This bit reflects the state of the BM general purpose input signal GPIO 08 and writes will have no effect. 0: BM GPIO 08 state is low 1: BM GPIO 08 state is high | RO |
| 1 | BM GPIO 09: This bit reflects the state of the BM general purpose input signal GPIO 09 and writes will have no effect. 0: BM GPIO 09 state is low 1: BM GPIO 09 state is high | RO |
| 2 | BM GPIO 10: This bit reflects the state of the BM general purpose input signal GPIO 10 and writes will have no effect. 0: BM GPIO 10 state is low 1: BM GPIO 10 state is high | RO |
| 3 | BM GPIO 11: This bit reflects the state of the BM general purpose input signal GPIO 11 and writes will have no effect. 0: BM GPIO 11 state is low | RO |

| | | |
|---|---|----|
| | 1: BM GPIO 11 state is high | |
| 4 | BM GPIO 12: This bit reflects the state of the BM general purpose input signal GPIO 12 and writes will have no effect. 0: BM GPIO 12 state is low 1: BM GPIO 12 state is high | RO |
| 5 | BM GPIO 13: This bit reflects the state of the BM general purpose input signal GPIO 13 and writes will have no effect. 0: BM GPIO 13 state is low 1: BM GPIO 13 state is high | RO |
| 6 | BM GPIO 14: This bit reflects the state of the BM general purpose input signal GPIO 14 and writes will have no effect. 0: BM GPIO 14 state is low 1: BM GPIO 14 state is high | RO |
| 7 | BM GPIO 15: This bit reflects the state of the BM general purpose input signal GPIO 15 and writes will have no effect. 0: BM GPIO 15 state is low 1: BM GPIO 15 state is high | RO |

Register Address : **SPI Base + 06h**

Register Name : **DSP GPI (07-00 Low Byte) Register**

Default Value: ----

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | DSP GPIO 00: This bit reflects the state of the DSP general purpose input signal GPIO 00 and writes will have no effect. 0: DSP GPIO 00 state is low 1: DSP GPIO 00 state is high | RO |
| 1 | DSP GPIO 01: This bit reflects the state of the DSP general purpose input signal GPIO 01 and writes will have no effect. 0: DSP GPIO 01 state is low 1: DSP GPIO 01 state is high | RO |
| 2 | DSP GPIO 02: This bit reflects the state of the DSP general purpose input signal GPIO 02 and writes will have no effect. 0: DSP GPIO 02 state is low 1: DSP GPIO 02 state is high | RO |
| 3 | DSP GPIO 03: This bit reflects the state of the DSP general purpose input signal GPIO 03 and writes will have no effect. 0: DSP GPIO 03 state is low 1: DSP GPIO 03 state is high | RO |
| 4 | DSP GPIO 04: This bit reflects the state of the DSP general purpose input signal GPIO 04 and writes will have no effect. 0: DSP GPIO 04 state is low 1: DSP GPIO 04 state is high | RO |
| 5 | DSP GPIO 05: This bit reflects the state of the DSP general purpose input signal GPIO 05 and writes will have no effect. 0: DSP GPIO 05 state is low 1: DSP GPIO 05 state is high | RO |

| | | |
|---|---|----|
| 6 | DSP GPIO 06: This bit reflects the state of the DSP general purpose input signal GPIO 06 and writes will have no effect. 0: DSP GPIO 06 state is low 1: DSP GPIO 06 state is high | RO |
| 7 | DSP GPIO 07: This bit reflects the state of the DSP general purpose input signal GPIO 07 and writes will have no effect. 0: DSP GPIO 07 state is low 1: DSP GPIO 07 state is high | RO |

Register Address : **SPI Base + 07h**

Register Name : **DSP GPI (15-08 High Byte) Status Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | DSP GPIO 08: This bit reflects the state of the DSP general purpose input signal GPIO 08 and writes will have no effect. 0: DSP GPIO 08 state is low 1: DSP GPIO 08 state is high | RO |
| 1 | DSP GPIO 09: This bit reflects the state of the DSP general purpose input signal GPIO 09 and writes will have no effect. 0: DSP GPIO 09 state is low 1: DSP GPIO 09 state is high | RO |
| 2 | DSP GPIO 10: This bit reflects the state of the DSP general purpose input signal GPIO 10 and writes will have no effect. 0: DSP GPIO 10 state is low 1: DSP GPIO 10 state is high | RO |
| 3 | DSP GPIO 11: This bit reflects the state of the DSP general purpose input signal GPIO 11 and writes will have no effect. 0: DSP GPIO 11 state is low 1: DSP GPIO 11 state is high | RO |
| 4 | DSP GPIO 12: This bit reflects the state of the DSP general purpose input signal GPIO 12 and writes will have no effect. 0: DSP GPIO 12 state is low 1: DSP GPIO 12 state is high | RO |
| 5 | DSP GPIO 13: This bit reflects the state of the DSP general purpose input signal GPIO 13 and writes will have no effect. 0: DSP GPIO 13 state is low 1: DSP GPIO 13 state is high | RO |
| 6 | DSP GPIO 14: This bit reflects the state of the DSP general purpose input signal GPIO 14 and writes will have no effect. 0: DSP GPIO 14 state is low 1: DSP GPIO 14 state is high | RO |
| 7 | DSP GPIO 15: This bit reflects the state of the DSP general purpose input signal GPIO 15 and writes will have no effect. 0: DSP GPIO 15 state is low 1: DSP GPIO 15 state is high | RO |

Register Address : **SPI Base + 08h**
 Register Name : **Debug LED Register**
 Default Value: 00h
 Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 0 | DEBUG_LED 1: This bit can be updated by the DSP software to drive a high or low value on the debug LED 0 pin. 0: DEBUG_LED 1 drives low 1: DEBUG_LED 1 drives high | R/W |
| 1 | DEBUG_LED 2: This bit can be updated by the DSP software to drive a high or low value on the debug LED 1 pin. 0: DEBUG_LED 2 drives low 1: DEBUG_LED 2 drives high | R/W |
| 2 | DEBUG_LED 3: This bit can be updated by the DSP software to drive a high or low value on the debug LED 2 pin 0: DEBUG_LED 3 drives low 1: DEBUG_LED 3 drives high | R/W |
| 3 | DEBUG_LED 4: This bit can be updated by the DSP software to drive a high or low value on the debug LED 3 pin 0: DEBUG_LED 4 drives low 1: DEBUG_LED 4 drives high | R/W |
| 7-4 | Reserved | RO |

Register Address : **SPI Base + 09h**
 Register Name : **MMC Control Register**
 Default Value: ----
 Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | MMC_DETECT#: This bit reflects the MMC_DETECT# state and it is used by the MMC to indicate the AMC chassis insertion status. 0: MMC_DETECT# state is low to indicate that the EVM is inserted into the AMC chassis. 1: MMC_DETECT# state is high to indicate that the EVM is not inserted into the AMC chassis. | RO |
| 1 | MMC_RESETSTAT#: This bit reflects the DSP RESETSTAT# state and the FPGA will drive the same logic value on the MMC_RESETSTAT# pin (to MMC). 0: DSP RESETSTAT# state is low and the FPGA drives MMC_RESETSTAT# low to MMC 1: DSP RESETSTAT# state is high and the FPGA drives MMC_RESETSTAT# high to MMC | RO |
| 2 | MMC_POR_IN_AMC#: This bit reflects the MMC_POR_IN_AMC# state and it is used by the MMC to trigger a Power-on sequence & reset event. 0: MMC_POR_IN_AMC# state is low to trigger a Power-on sequence & reset event. 1: MMC_POR_IN_AMC# state is high and the FPGA stays in | RO |

| | | |
|-----|---|----|
| | current state. | |
| 3 | MMC_WR_AMC#: This bit reflects the MMC_WR_AMC# state and it is used by the MMC to trigger a warm reset event. 0: MMC_WR_AMC# state is low to trigger a warm reset event. 1: MMC_WR_AMC# state is high and the FPGA stays in current state | RO |
| 4 | MMC_BOOTCOMPLETE: This bit reflects the DSP_BOOTCOMPLETE state and the FPGA will drive the same logic value on the MMC_BOOTCOMPLETE pin (to MMC). 0: DSP_BOOTCOMPLETE state is low and the FPGA drives MMC_BOOTCOMPLETE low to MMC 1: DSP_BOOTCOMPLETE state is high and the FPGA drives MMC_BOOTCOMPLETE high to MMC | RO |
| 7-5 | Reserved | RO |

Register Address : **SPI Base + 0Ah**

Register Name : **PHY Control Register**

Default Value: 03h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | PHY_INT#: This bit reflects the PHY_INT# state. 0: PHY_INT# state is low. 1: PHY_INT# state is high. | RO |
| 1 | PHY_RST#: This bit can be updated by the DSP software to drive a high or low value on the PHY_RST# pin 0: PHY_RST# drives low 1: PHY_RST# drives high | R/W |
| 7-3 | Reserved | RO |

Register Address : **SPI Base + 0Bh**

Register Name : **Reset Button Status Register**

Default Value: ----

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | FULL_RESET button status: This bit reflects the FULL_RESET button state. This button is used to request a power full reset sequence to DSP. A logic Low to High transition on this button signal will complete the FPGA FULL_RESET sequence with a specified delay time. 0: FULL_RESET button state is low 1: FULL_RESET button state is high | RO |
| 1 | WARM_RESET button status (RFU): This bit reflects the WARM_RESET button state. This button is used to request a warm reset sequence to DSP. A logic Low to High transition on this button signal will complete the FPGA WARM_RESET sequence with a specified delay time. 0: WARM_RESET button state is low | RO |

| | | |
|---|---|----|
| | 1: WARM_RESET button state is high | |
| 2 | COLD_RESET button status (RFU): This bit reflects the COLD_RESET button state. This button is used to request a hard reset sequence to DSP. A logic Low to High transition on this button signal will complete the FPGA HARD_RESET sequence with a specified delay time. 0: COLD_RESET button state is low 1: COLD_RESET button state is high | RO |
| 3 | Reserved | RO |
| 4 | DSP_RESETSTAT#: This bit reflects the DSP_RESETSTAT# state. 0: DSP_RESETSTAT# state is low 1: DSP_RESETSTAT# state is high | RO |
| 5 | TRGRSTZ: This bit reflects the TRGRSTZ state. 0: TRGRSTZ state is low 1: TRGRSTZ state is high | RO |
| 6 | PCIESSEN: This bit reflects the PCIESSEN switch state. 0: PCIESSEN state is low 1: PCIESSEN state is high | RO |
| 7 | User Defined Switch: This bit reflects the User_Define_Switch state. 0: User Defined Switch state is low 1: User Defined Switch state is high | RO |

Register Address : **SPI Base + 0Ch**

Register Name : **Miscellaneous - 1 Register**

Default Value: 1Ch

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 1-0 | Reserved | R/W |
| 2 | NAND_WP#: This bit can be updated by the DSP software to drive a high or low value on the NAND_WP# pin (RFU) 0: NAND_WP# drives low 1: NAND_WP# drives high | R/W |
| 3 | XDS560_IL Enable Control : 0: XDS560 mezzanine card is disabled. 1: XDS560 mezzanine card is enabled. | R/W |
| 4 | NOR_WP#: This bit can be updated by the DSP software to drive a high or low value on the NOR_WP# pin (RFU) 0: NOR_WP# drives low 1: NOR_WP# drives high | R/W |
| 5 | EEPROM_WP: This bit can be updated by the DSP software to drive a high or low value on the EEPROM_WP pin (RFU) 0: EEPROM_WP drives low 1: EEPROM_WP drives high | R/W |
| 6 | PCA9306_EN: This bit can be updated by the DSP software to drive a high or low value on the PCA9306_EN pin (RFU) 0: PCA9306_EN drives low | R/W |

| | | |
|---|---------------------------|----|
| | 1: PCA9306_EN drives high | |
| 7 | Reserved | RO |

Register Address : **SPI Base + 0Dh**

Register Name : Miscellaneous - 2 Register

Default Value: ----

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 0 | FPGA FW Update SPI Interface Enable Status: This bit reflects the FPGA FW Update SPI Interface Enable status. The FPGA FW Update SPI interface could be enabled/disabled through the offset 0Eh register. 0: FPGA FW update SPI interface is disabled. 1: FPGA FW update SPI interface is enabled. The DSP_GPIO[12] is mapped to FPGA_FW_SPI_CLK. The DSP_GPIO[13] is mapped to FPGA_FW_SPI_CS#. The DSP_GPIO[14] is mapped to FPGA_FW_SPI_MOSI. The DSP_GPIO[15] is mapped to FPGA_FW_SPI_MISO. | RO |
| 2 | DSP_HOUT status: This bit reflects the DSP_HOUT signal state. 0: DSP_HOUT state is low 1: DSP_HOUT state is high | RO |
| 3 | DSP_SYSCLKOUT status: This bit reflects the DSP_SYSCLKOUT signal state. 0: DSP_SYSCLKOUT state is low 1: DSP_SYSCLKOUT state is high | RO |
| 7-4 | Reserved | RO |

Register Address : **SPI Base + 0Eh**

Register Name : **FPGA FW Update SPI Interface Control Register**

Default Value: Default Value: ----

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | FPGA FW Update SPI Interface Enable Control: These bits are used to enable/disable the FPGA FW Update SPI Interface. If the value of this register be set to 68h, the FPGA FW Update SPI interface would be enabled. All the other values set to this register would disable the FPGA FW Update SPI interface. 68h: FPGA FW update SPI interface is enabled. Others: FPGA FW update SPI interface is disabled. The DSP_GPIO[12] is mapped to FPGA_FW_SPI_CLK. The DSP_GPIO[13] is mapped to FPGA_FW_SPI_CS#. The DSP_GPIO[14] is mapped to FPGA_FW_SPI_MOSI. The DSP_GPIO[15] is mapped to FPGA_FW_SPI_MISO. | R/W |

Register Address : **SPI Base + 0Fh**

Register Name : **Scratch Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--------------|------------|
| 7-0 | Scratch Data | R/W |

Register Address : **SPI Base + 10h**

Register Name : **CLK-GEN 2 Control Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 0 | Initiate a data transfer via the SPI bus to update the SPI command to CDCE62005 Clock Generator #2 0: Idle state 1: Write 1 to perform the SPI command update process. | R/W |
| 1 | The BUSY status indication for the CDCE62005 Clock Generator #2 SPI bus 0: The SPI bus for the CDCE62005 Clock Generator #2 is idle. 1: The SPI bus for the CDCE62005 Clock Generator #2 is busy and a SPI command is processing.. | RO |
| 7-2 | Reserved | RO |

Register Address : **SPI Base + 11h**

Register Name : **CLK-GEN 2 Interface Clock Setting Register**

Default Value: 03h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register is a clock divider setting to adjust the interface clock for the CDCE62005 Clock Generator #2 SPI bus. 00: CDCE62005 #2 SPI Clock = 12MHz (= 48 / 4) 01: CDCE62005 #2 SPI Clock = 12MHz (= 48 / 4) 02: CDCE62005 #2 SPI Clock = 8 MHz (= 48 / 6) 03: CDCE62005 #2 SPI Clock = 6 MHz (= 48 / 8) 04: CDCE62005 #2 SPI Clock = 4.8 MHz (= 48 /10) 05: CDCE62005 #2 SPI Clock = 4 MHz (= 48 /12) 06: CDCE62005 #2 SPI Clock = 3.42 MHz (= 48 / 14) X: CDCE62005 #2 SPI Clock = 48 MHz /((X+1)*2) if X != 0 | R/W |

Register Address : **SPI Base + 12h ~ 13h**

Register Name : **Reserved**

Register Address : **SPI Base + 14h**

Register Name : **CLK-GEN 2 Command Byte 0 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 0 to the CDCE62005 Clock Generator #2 | R/W |

| | | |
|--|---|--|
| | 3-0: SPI command address field bit 3 to bit 0 7-4: SPI command data field bit 3 to bit 0 | |
|--|---|--|

Register Address : **SPI Base + 15h**
Register Name : **CLK-GEN 2 Command Byte 1 Register**
Default Value: 00h
Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 1 to the CDCE62005 Clock Generator #2 7-0: SPI command data field bit 11 to bit 4 | R/W |

Register Address : **SPI Base + 16h**
Register Name : **CLK-GEN 2 Command Byte 2 Register**
Default Value: 00h
Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 2 to the CDCE62005 Clock Generator #2 7-0: SPI command data field bit 19 to bit12 | R/W |

Register Address : **SPI Base + 17h**
Register Name : **CLK-GEN 2 Command Byte 3 Register**
Default Value: 00h
Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 3 to the CDCE62005 Clock Generator #2 7-0: SPI command data field bit 27 to bit 20 | R/W |

Register Address : **SPI Base + 18h**
Register Name : **CLK-GEN 2 Read Data Byte 0 Register**
Default Value: 00h
Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 0 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4: The SPI read back data bit 3 to bit 0 for a SPI Read Command. | RO |

Register Address : **SPI Base + 19h**
Register Name : **CLK-GEN 2 Read Data Byte 1 Register**
Default Value: 00h
Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 11 to bit 4 for a SPI Read Command. | RO |

Register Address : **SPI Base + 1Ah**

Register Name : **CLK-GEN 2 Read Data Byte 2 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 19 to bit 12 for a SPI Read Command. | RO |

Register Address : **SPI Base + 1Bh**

Register Name : **CLK-GEN 2 Read Data Byte 3 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 27 to bit 20 for a SPI Read Command. | RO |

Register Address : **SPI Base + 1Ch ~ 1Fh**

Register Name : **Reserved**

Register Address : **SPI Base + 20h**

Register Name : **CLK-GEN 3 Control Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | Initiate a data transfer via the SPI bus to update the SPI command to CDCE62005 Clock Generator #3 0: Idle state 1: Write 1 to perform the SPI command update process. | R/W |
| 1 | The BUSY status indication for the CDCE62005 Clock Generator #3 SPI bus 0: The SPI bus for the CDCE62005 Clock Generator #3 is idle. 1: The SPI bus for the CDCE62005 Clock Generator #3 is busy and a SPI command is processing. | RO |
| 7-2 | Reserved | RO |

Register Address : **SPI Base + 21h**
 Register Name : **CLK-GEN 3 Interface Clock Setting Register**
 Default Value: 00h
 Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register is a clock divider setting to adjust the interface clock for the CDCE62005 Clock Generator #3 SPI bus. 00: CDCE62005 #3 SPI Clock = 12MHz (= 48 / 4) 01: CDCE62005 #3 SPI Clock = 12MHz (= 48 / 4) 02: CDCE62005 #3 SPI Clock = 8 MHz (= 48 / 6) 03: CDCE62005 #3 SPI Clock = 6 MHz (= 48 / 8) 04: CDCE62005 #3 SPI Clock = 4.8 MHz (= 48 /10) 05: CDCE62005 #3 SPI Clock = 4 MHz (= 48 /12) 06: CDCE62005 #3 SPI Clock = 3.42 MHz (= 48 / 14) X: CDCE62005 #3 SPI Clock = 48 MHz /((X+1)*2) if X != 0 | R/W |

Register Address : **SPI Base + 22h ~ 23h**
 Register Name : **Reserved**

Register Address : **SPI Base + 24h**
 Register Name : **CLK-GEN 3 Command Byte 0 Register**
 Default Value: 00h
 Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 0 to the CDCE62005 Clock Generator #3 3-0: SPI command address field bit 3 to bit 0 7-4: SPI command data field bit 3 to bit 0 | R/W |

Register Address : **SPI Base + 25h**
 Register Name : **CLK-GEN 3 Command Byte 1 Register**
 Default Value: 00h
 Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 1 to the CDCE62005 Clock Generator #3 7-0: SPI command data field bit 11 to bit 4 | R/W |

Register Address : **SPI Base + 26h**
 Register Name : **CLK-GEN 3 Command Byte 2 Register**
 Default Value: 00h
 Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 2 to the CDCE62005 Clock Generator #3 | R/W |

| | | |
|--|--|--|
| | 7-0: SPI command data field bit 19 to bit 12 | |
|--|--|--|

Register Address : **SPI Base + 27h**

Register Name : **CLK-GEN 3 Command Byte 3 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 3 to the CDCE62005 Clock Generator #3 7-0: SPI command data field bit 27 to bit 20 | R/W |

Register Address : **SPI Base + 28h**

Register Name : **CLK-GEN 3 Read Data Byte 0 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register reflects the read back data byte 0 from the CDCE62005 Clock Generator #3 for responding to a host SPI Read Command. 3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4: The SPI read back data bit 3 to bit 0 for a SPI Read Command. | RO |

Register Address : **SPI Base + 29h**

Register Name : **CLK-GEN 3 Read Data Byte 1 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #3 for responding to a host SPI Read Command. 7-0: The SPI read back data bit 11 to bit 4 for a SPI Read Command. | RO |

Register Address : **SPI Base + 2Ah**

Register Name : **CLK-GEN 3 Read Data Byte 2 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #3 for responding to a host SPI Read Command. 7-0: The SPI read back data bit 19 to bit 12 for a SPI Read Command. | RO |

Register Address : **SPI Base + 2Bh**

Register Name : **CLK-GEN 3 Read Data Byte 3 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #3 for responding to a host SPI Read Command. 7-0: The SPI read back data bit 27 to bit 20 for a SPI Read Command. | RO |

Register Address : **SPI Base + 2Ch ~ 2Fh**

Register Name : **Reserved**

Register Address : **SPI Base + 30h ~ 3Fh(RFU)**

Register Name : **PM Bus Control Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|-------------|------------|
| 7-0 | RFU | R/W |

Register Address : **SPI Base + 40h**

Register Name : **CLK-GEN 1 Control Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 0 | Initiate a data transfer via the SPI bus to update the SPI command to CDCE62002 Clock Generator #1 0: Idle state 1: Write 1 to perform the SPI command update process. | R/W |
| 1 | The BUSY status indication for the CDCE62002 Clock Generator #1 SPI bus 0: The SPI bus for the CDCE62002 Clock Generator #1 is idle. 1: The SPI bus for the CDCE62002 Clock Generator #1 is busy and a SPI command is processing.. | RO |
| 7-2 | Reserved | RO |

Register Address : **SPI Base + 41h**

Register Name : **CLK-GEN 1 Interface Clock Setting Register**

Default Value: 03h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register is a clock divider setting to adjust the interface clock for the CDCE62002 Clock Generator #1 SPI bus. 00: CDCE62002 SPI Clock = 12MHz (= 48 / 4) 01: CDCE62002 SPI Clock = 12MHz (= 48 / 4) 02: CDCE62002 SPI Clock = 8 MHz (= 48 / 6) 03: CDCE62002 SPI Clock = 6 MHz (= 48 / 8) | R/W |

| | | |
|--|--|--|
| | 04: CDCE62002 SPI Clock = 4.8 MHz (= 48 /10) 05: CDCE62002 SPI Clock = 4 MHz (= 48 /12) 06: CDCE62002 SPI Clock = 3.42 MHz (= 48 / 14) X: CDCE62002 SPI Clock = 48 MHz /((X+1)*2) if X != 0 | |
|--|--|--|

Register Address : **SPI Base + 42h ~ 43h**

Register Name : **Reserved**

Register Address : **SPI Base + 44h**

Register Name : **CLK-GEN 1 Command Byte 0 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 0 to the CDCE62002 Clock Generator #1 3-0: SPI command address field bit 3 to bit 0 7-4: SPI command data field bit 3 to bit 0 | R/W |

Register Address : **SPI Base + 45h**

Register Name : **CLK-GEN 1 Command Byte 1 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register specifies the update SPI command byte 1 to the CDCE62002 Clock Generator #1 7-0: SPI command data field bit 11 to bit 4 | R/W |

Register Address : **SPI Base + 46h**

Register Name : **CLK-GEN 1 Command Byte 2 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 2 to the CDCE62002 Clock Generator #1 7-0: SPI command data field bit 19 to bit 12 | R/W |

Register Address : **SPI Base + 47h**

Register Name : **CLK-GEN 1 Command Byte 3 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register specifies the update SPI command byte 3 to the CDCE62002 Clock Generator #1 7-0: SPI command data field bit 27 to bit 20 | R/W |

Register Address : **SPI Base + 48h**

Register Name : **CLK-GEN 1 Read Data Byte 0 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 0 from the CDCE62002 Clock Generator #1 for responding a host SPI Read Command. 3-0: The SPI read back register address [3-0] for a SPI Read Command 7-4: The SPI read back data bit 3 to bit 0 for a SPI Read Command. | RO |

Register Address : **SPI Base + 49h**

Register Name : **CLK-GEN 1 Read Data Byte 1 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|---|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62002 Clock Generator #1 for responding a host SPI Read Command. 7-0: The SPI read back data bit 11 to bit 4 for a SPI Read Command. | RO |

Register Address : **SPI Base + 4Ah**

Register Name : **CLK-GEN 1 Read Data Byte 2 Register**

Default Value: 00h

Attribute: Read Only

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62002 Clock Generator #1 for responding a host SPI Read Command. 7-0: The SPI read back data bit 19 to bit 12 for a SPI Read Command. | RO |

Register Address : **SPI Base + 4Bh**

Register Name : **CLK-GEN 1 Read Data Byte 3 Register**

Default Value: 00h

Attribute: Read/Write

| Bit | Description | Read/Write |
|-----|--|------------|
| 7-0 | This register reflects the read back data byte 1 from the CDCE62002 Clock Generator #1 for responding a host SPI Read Command. 7-0: The SPI read back data bit 27 to bit 20 for a SPI Read Command. | RO |

Register Address : **SPI Base + 4Ch ~ 4Fh**

Register Name : **Reserved**

Register Address : **SPI Base + 50h**

Register Name : **ICS 557 Clock Selection Control Register**

Default Value: 00h

Attribute : Read/Write

| Bit | Description | Read/Write |
|-----|---|------------|
| 0 | FPGA_ICS557_SEL : This bit can be updated by the DSP software to drive a high or low value on the FPGA_ICS557_SEL pin. 0 : FPGA_ICS557_SEL drives low 1 : FPGA_ICS557_SEL drives high | R/W |

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